# Overview of the ALPIDE Pixel Sensor Features

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All credits for illustrations and reference material: **ALICE ITS Project Team**

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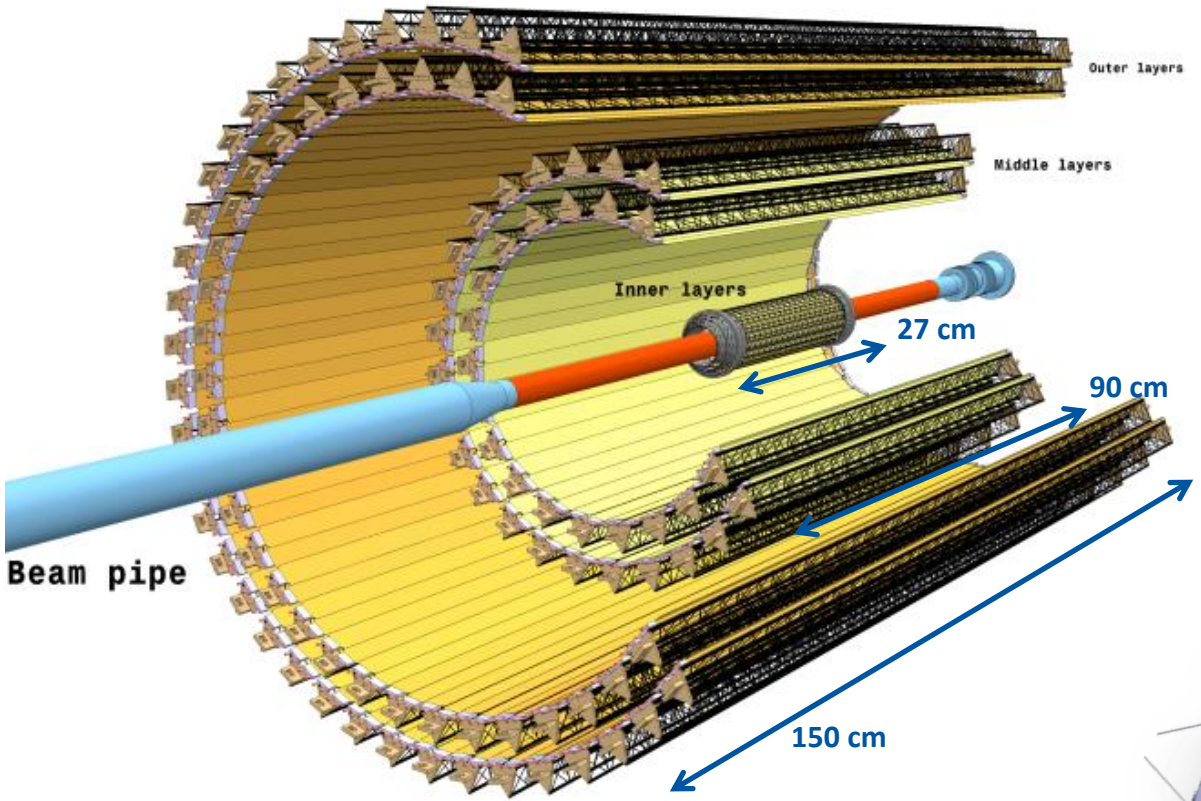
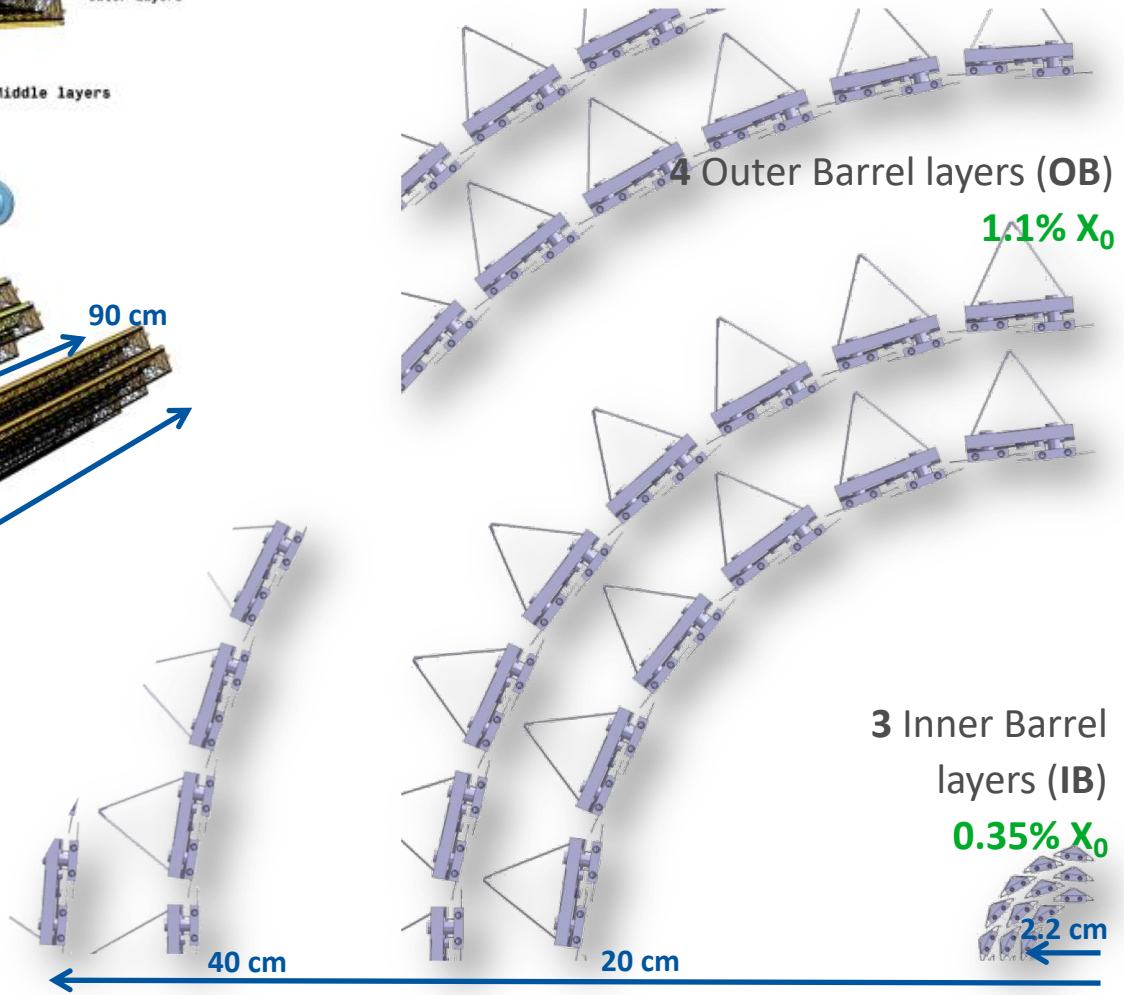
# Outline

1. ALPIDE Chip Description
2. Performance Figures, Timing and Readout capabilities
3. Integration of ALPIDE in ITS modules

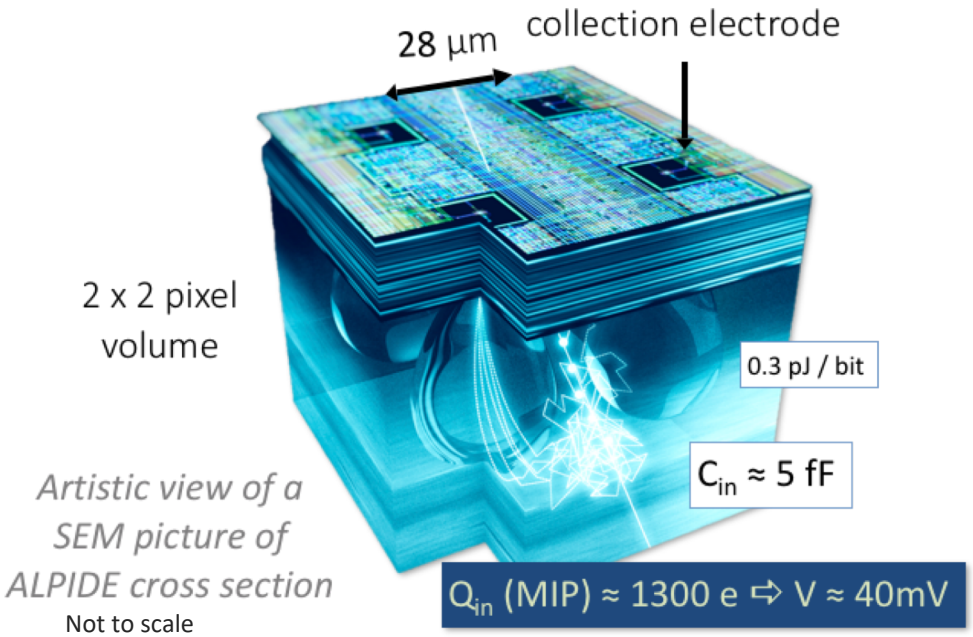
# ALICE ITS Upgrade Layout



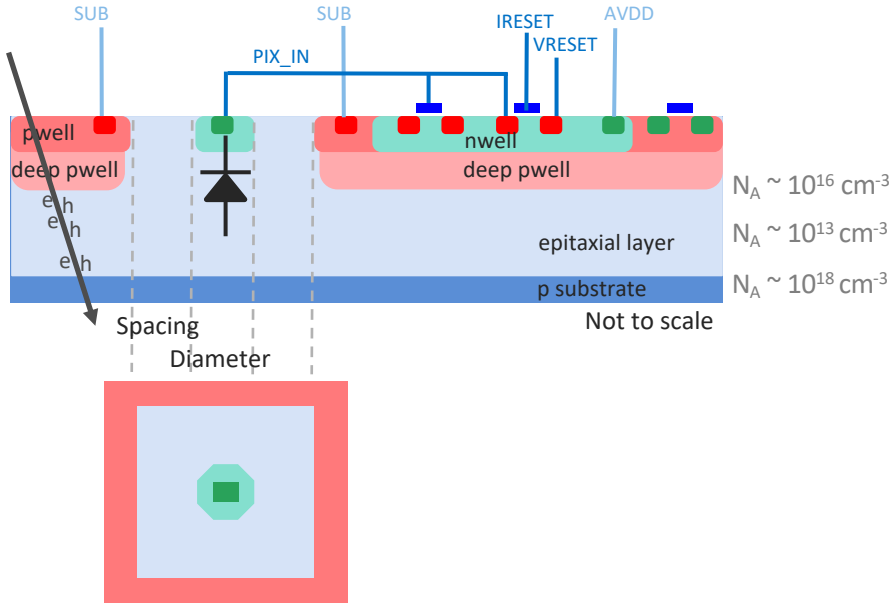

**10 m²** sensitive area
**24120** CMOS Pixel Sensors
**~12.5** Gpixels



# ALPIDE Technology




Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)



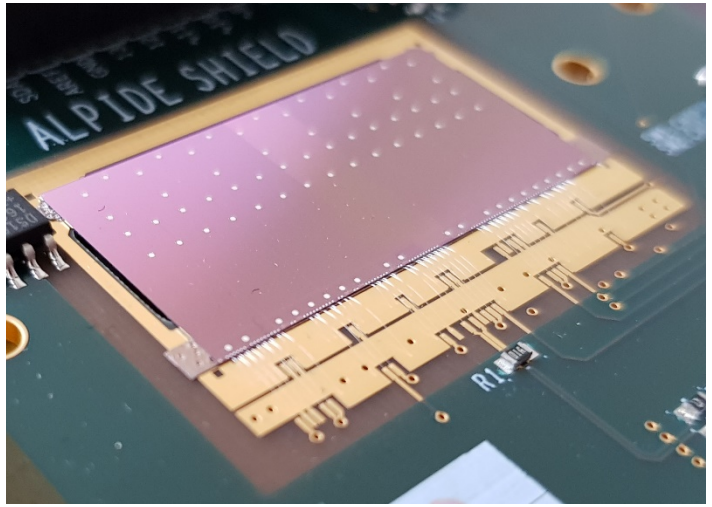

High-resistivity (> 1kΩ cm) p-type epitaxial layer (~25 µm) on p-type substrate

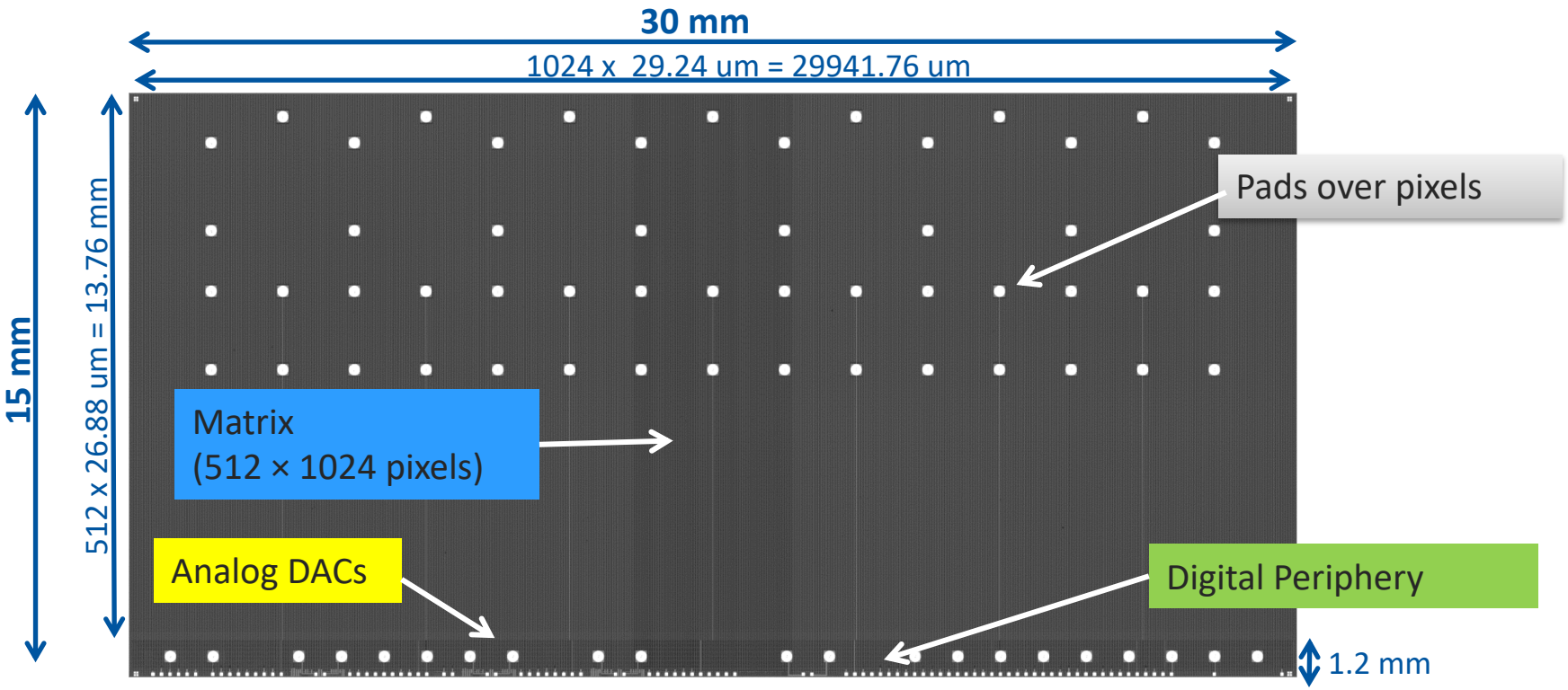
Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)

Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance => large S/N

Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode

# ALPIDE Chip




CCNU,
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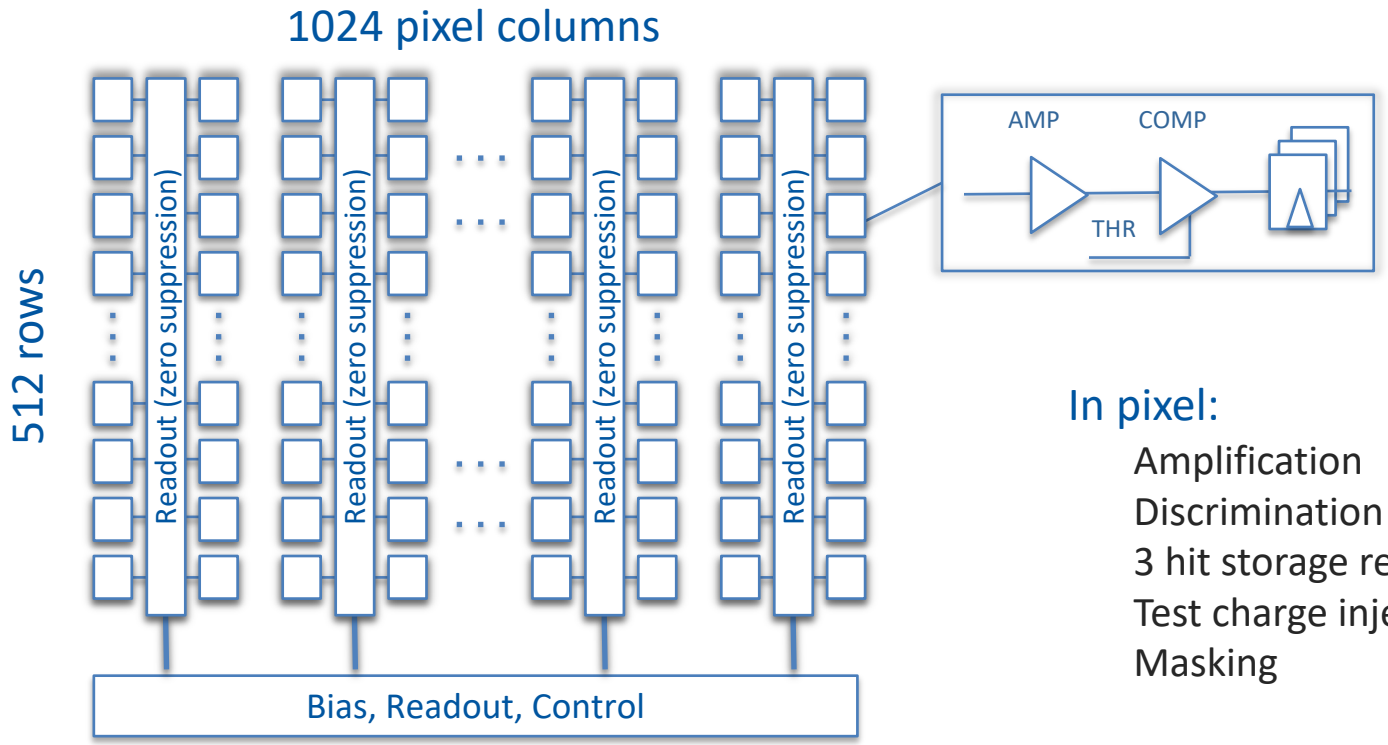
INFN (Torino, Cagliari),
IPHC,
IRFU,
NIKHEF,
YONSEI

# ALPIDE Architecture




In pixel:

- Amplification
- Discrimination
- 3 hit storage registers (MEB)
- Test charge injection
- Masking

29 μm x 27 μm pixel pitch

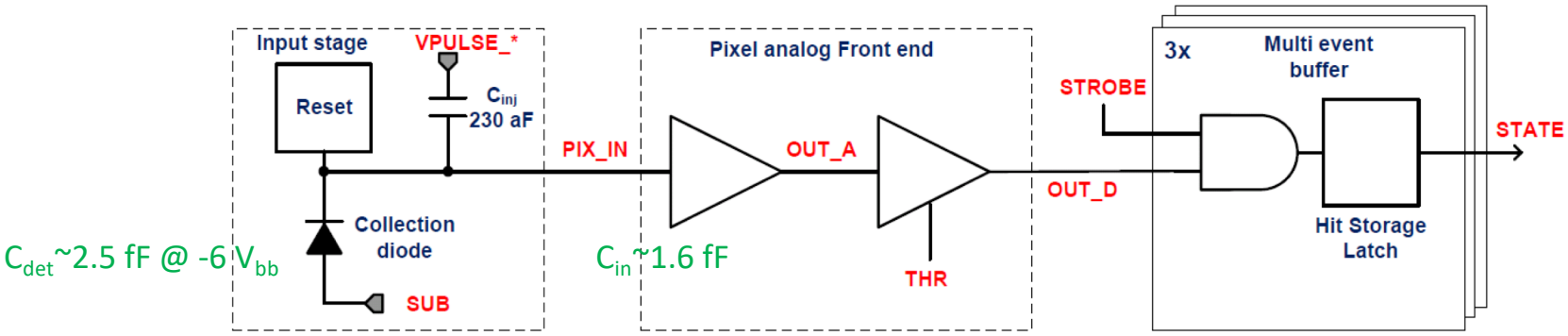
Continuously active front-end

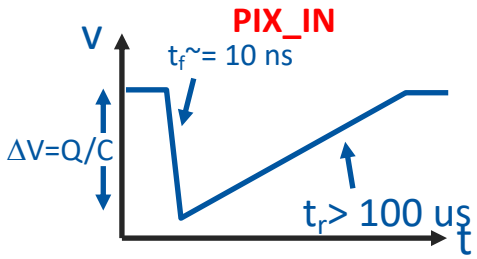
Global shutter (*STROBE signal*)

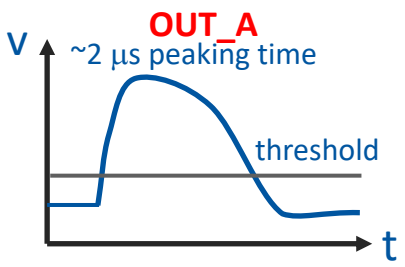
Zero-suppressed matrix readout

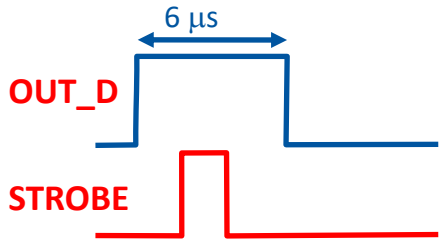
Triggered or continuous readout modes

# Pixel




## Analog front-end and discriminator continuously active

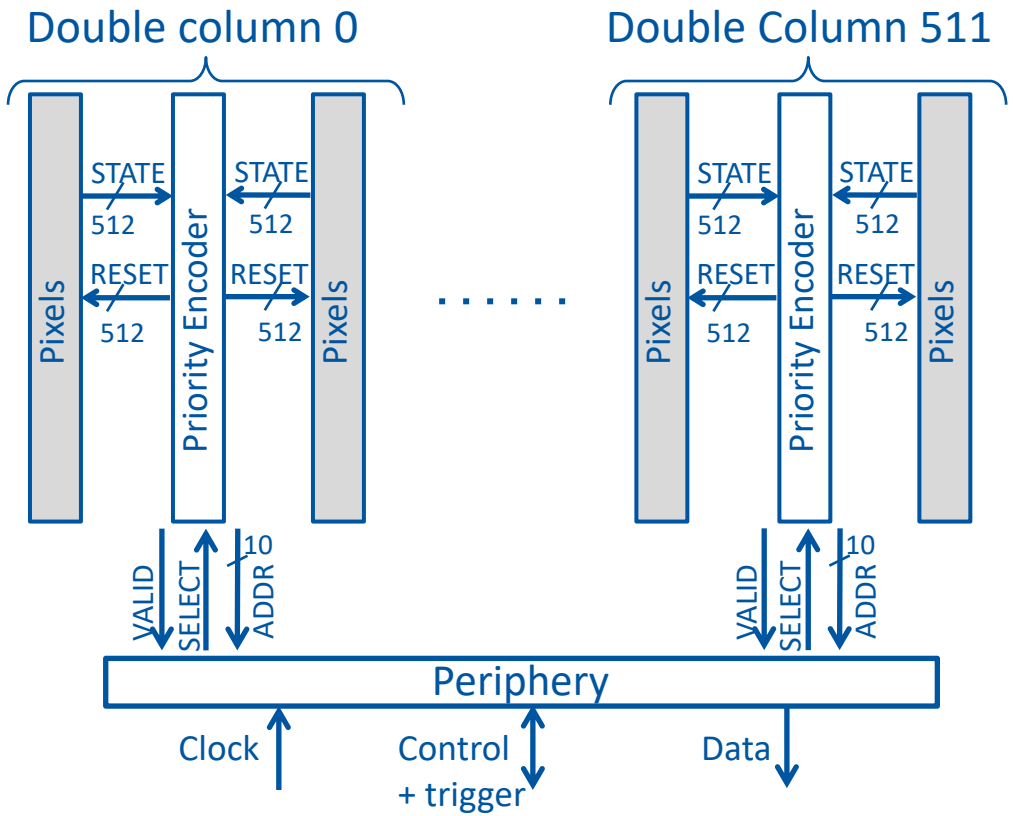
- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

## Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

| Front End Characteristics (simulated) | |
|---|---|
| Gain (small signal) [mV/e] | 4 |
| ENC [e] | 3.9 |
| Threshold [e] | 92 ± 2 |

# Matrix Readout




The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

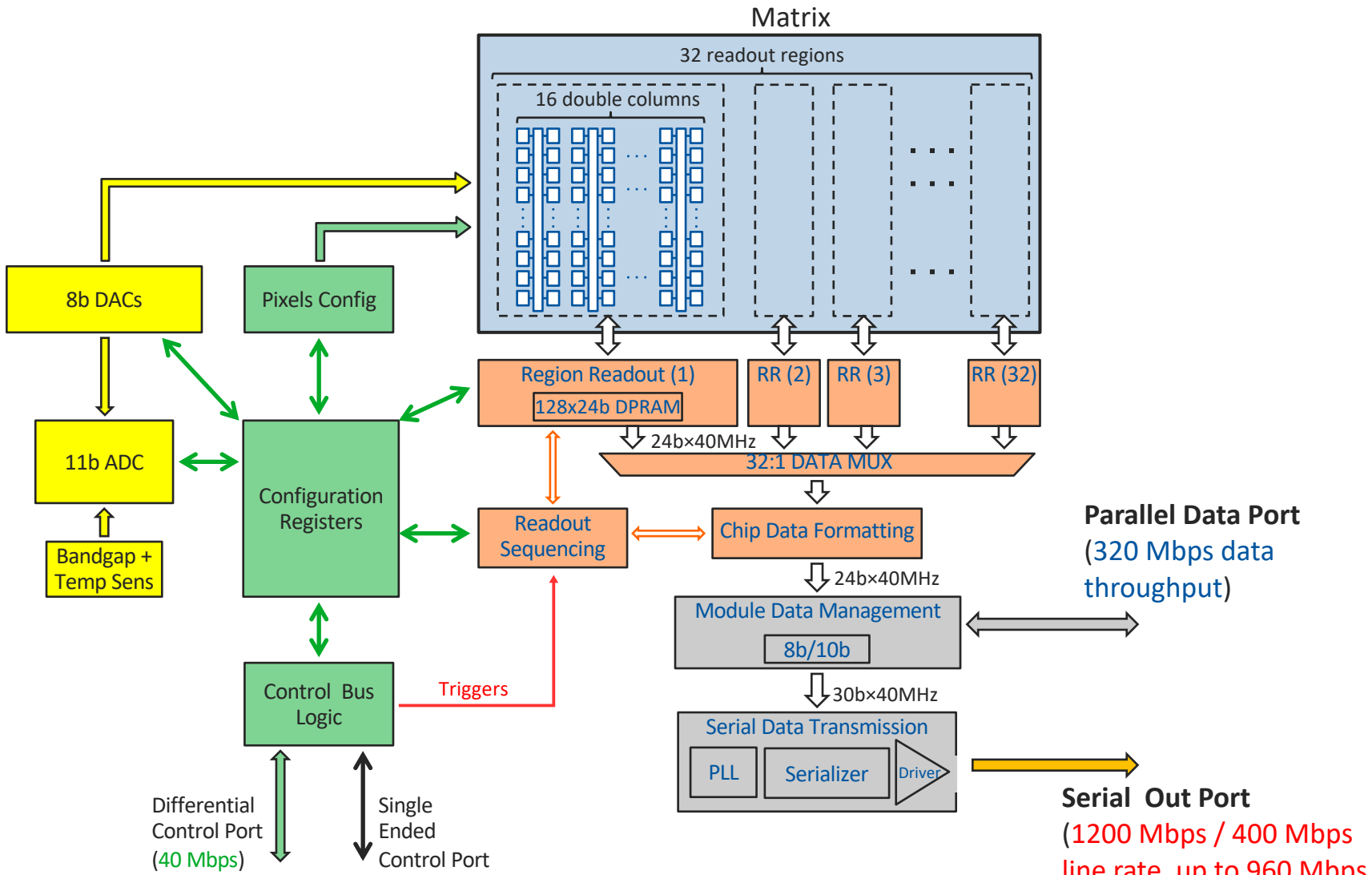
Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame

No free running clock over matrix. No activity if there are no hits

Energy per hit: $E_h$ ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate

Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

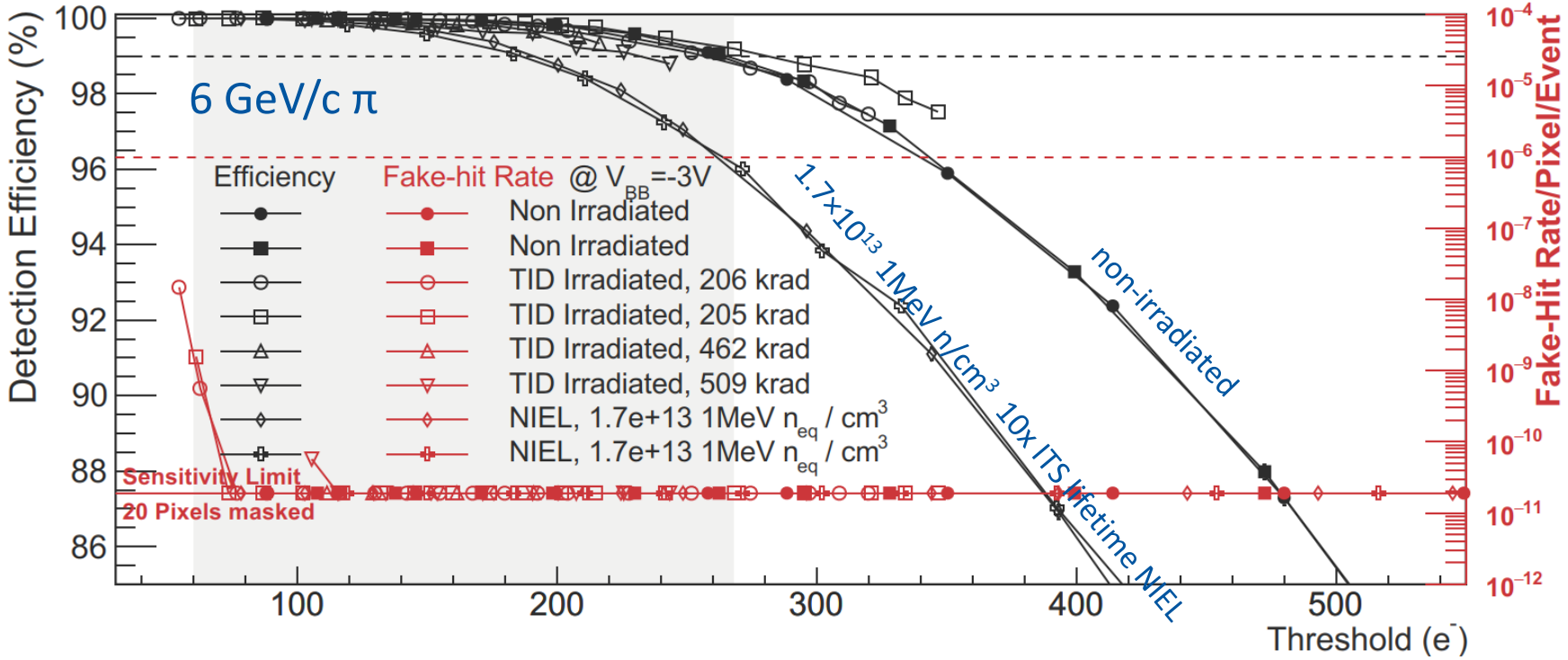
# ALPIDE Block Diagram



# PERFORMANCE FIGURES
# TIMING AND READOUT CAPABILITIES

# Detection Efficiency and Fake Hit Rate

## Test Beam Measurements

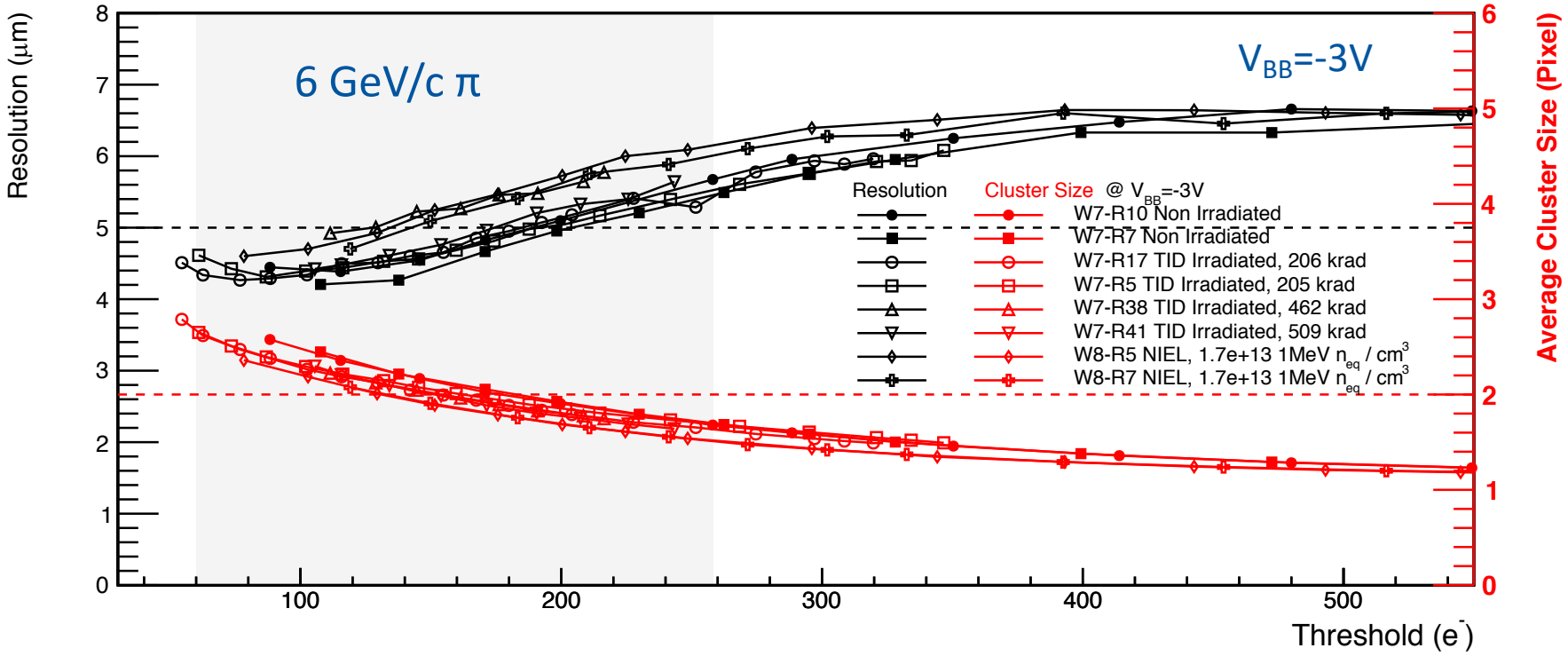



Large operational margin with O(10) masked pixels (0.002%)

Fake hit rate < $2*10^{-11}$ pixel hits/event

# Resolution and Cluster Size

## Test Beam Measurements




Resolution of 5 μm at a threshold of 200 electrons

Typ. cluster size 2 at a threshold of 200 electrons (normal incidence)

# Pixel Timing

Typical duration of discriminated pulse: **~6 us**

Max latency for STROBE assertion (max trigger latency in triggered mode)

~2.6 us constrained by clipping for *large (>5 ke)* input signals

Minimum setting of STROBE duration

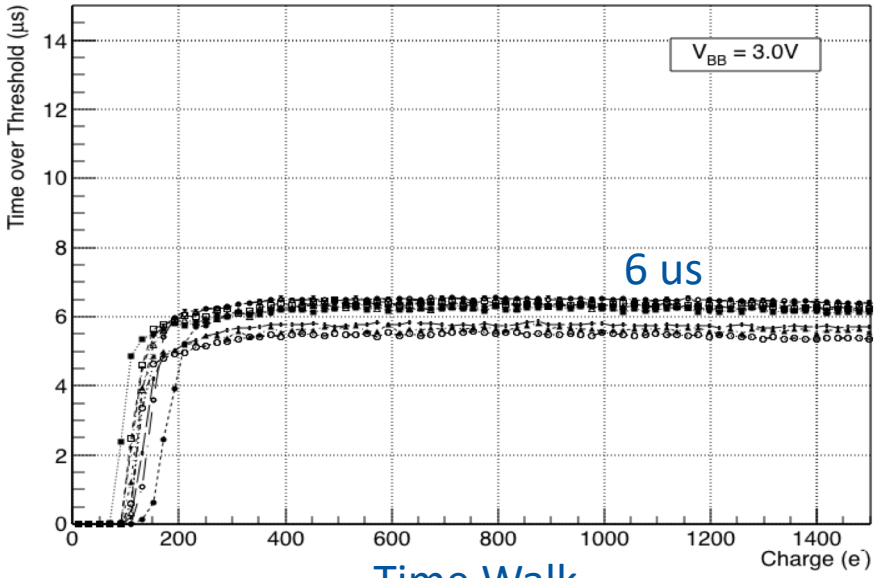
O(500 ns) determined by time walk for *small* input charge

Event time resolution is ultimately limited by *time walk*

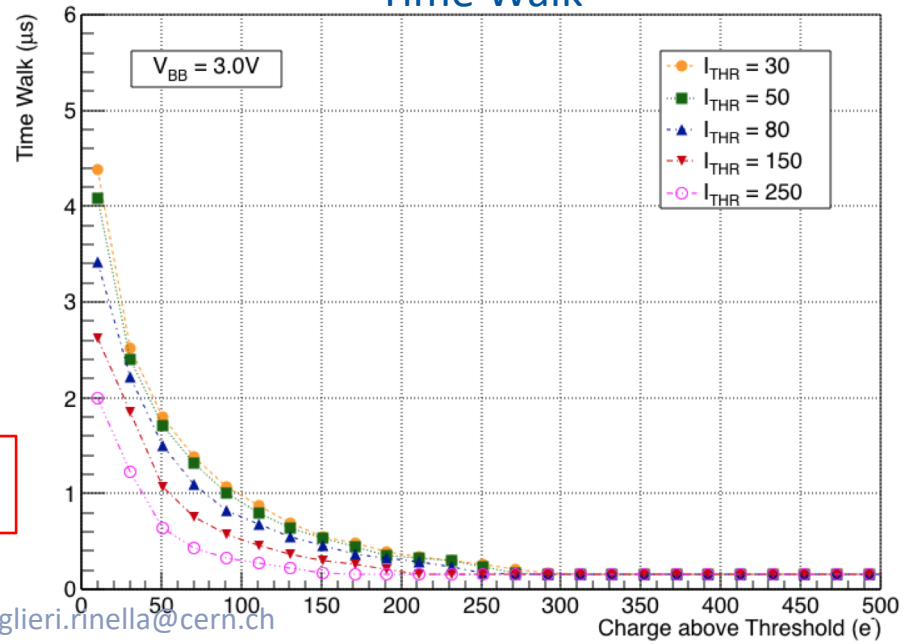
Depends on threshold (100e typ.)

Slide source: ALPIDE PRR

Time Over Threshold vs Injected Charge




Time Walk

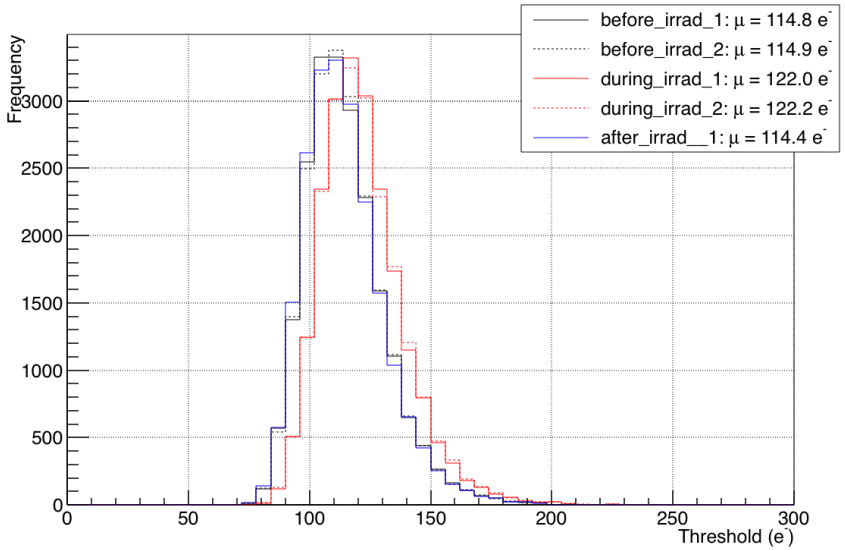


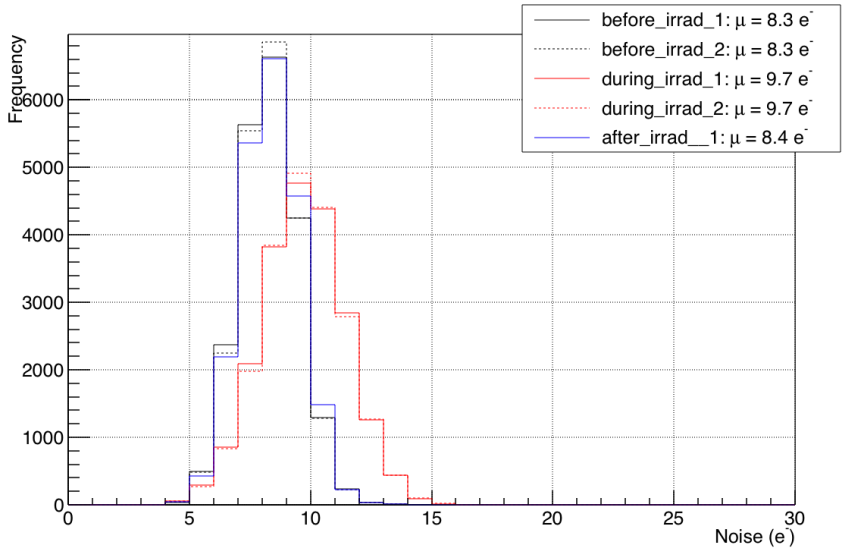
# Single-Pixel Pile-Up

Slide source: ALPIDE PRR

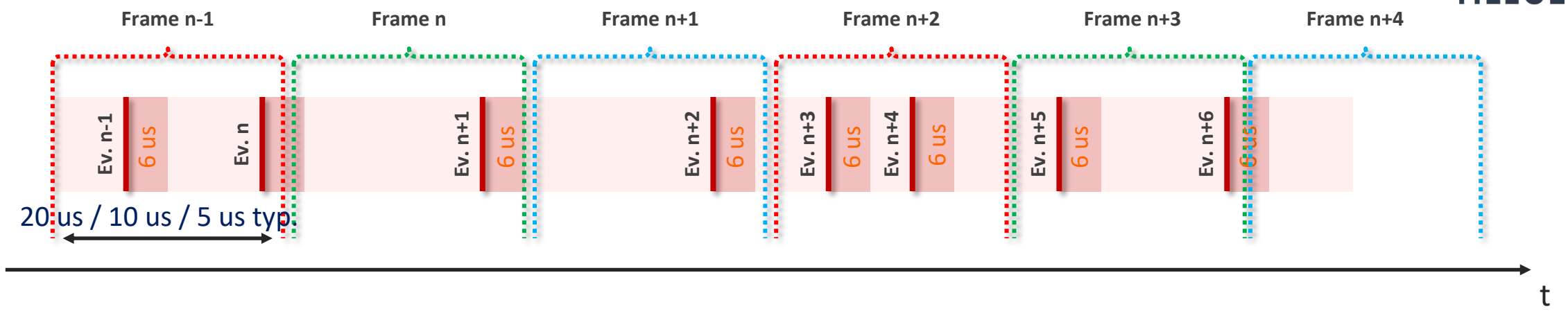
## Effect of Pile-Up in Single Pixel

- Perform threshold scan with simultaneous illumination with X-rays, compare results before / during / after illumination
- Modest increase of threshold and noise: +6% (17%) for an average single-pixel hit rate of 465 Hz (59 MHz/cm$^2$)
- Effect consistent with slight shift of operation point in single pixel



# Continuous Readout Mode (*free-running*)




Internal strobe has programmable duration

- Periodic frames can be synchronized externally or generated internally (full camera mode)

For every frame *start*, ALPIDE produces a data packet with time stamp and (optional) payload with hits in coincidence with frame strobe

- Hit data repetition can happen because of the duration of the discriminated pixel output
  - Event (n) and (n+6) in the sample diagram have hits repeated in two consecutive chip data packets (can be accounted for)

Decreasing frame duration *increases data throughput*

- Increases hit data volume because of double sampling pixel hits
- Increases overhead of chip data packet headers and trailers

# Hit Rates and Data Rates

## ALPIDE *particle* rate max. capabilities

Assuming 2.5 average cluster size

Matrix to Periphery hit data transfer: ~ 50 MHz/cm$^2$

At slow frame rates. Reduces with faster frame rate

Chip output link max capacity: ~ 6 MHz/cm$^2$ (with on-chip data reduction), ~ 4 MHz/cm$^2$ (raw)

Table source: ALPIDE PRR

## Operation in ALICE for Pb-Pb 100 kHz interaction rate

Combined Physics Simulation and SystemC model of ALPIDE

**~1.5 MHz cm$^{-2}$**
(Avg. Cluster size 3.7)

~1.9 MHz cm$^{-2}$
(This sustainable also with 5 us periodic frame)

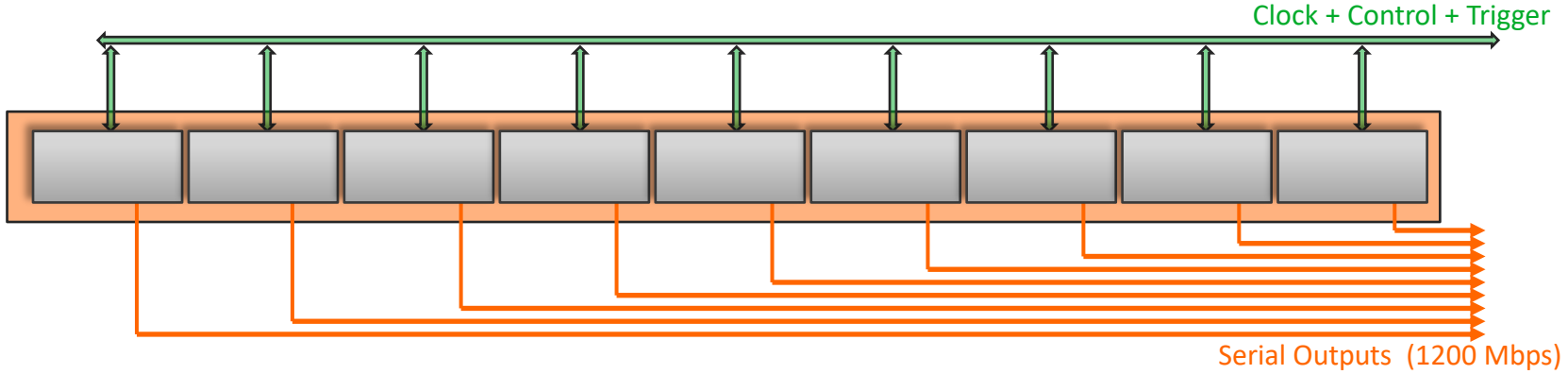
Needs dedicated HS Link per chip

| | | Layer 0 | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|---|---|
| Average fired pixels per event per sensor | **Total** (η = 0°) | **253.7** (326) | **152.7** (192.6) | **102.9** (127.2) | **4.8** (5.8) | **3.3** (4.1) | **1.9** (2.3) | **1.6** (1.8) |
| | Physics (η = 0°) | 152.6 (224.1) | 101.1 (141.0) | 71.0 (95.3) | 3.0 (4.0) | 2.7 (3.5) | 1.4 (1.8) | 1.1 (1.3) |
| | QED | 100.6 | 51.0 | 31.4 | 0.3 | 0.1 | 0.0 | 0.0 |
| | Noise | 0.53 | 0.52 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| Average data rate per master [Mbit/s] | Avg | **299.4** | **191.3** | **135.6** | **71.8** | **56.8** | **41.7** | **38.6** |
| | (η = 0°) | 362.5 | 223.3 | 154.2 | 79.7 | 60.7 | 45.8 | 41.2 |

# ALPIDE IN ITS MODULES

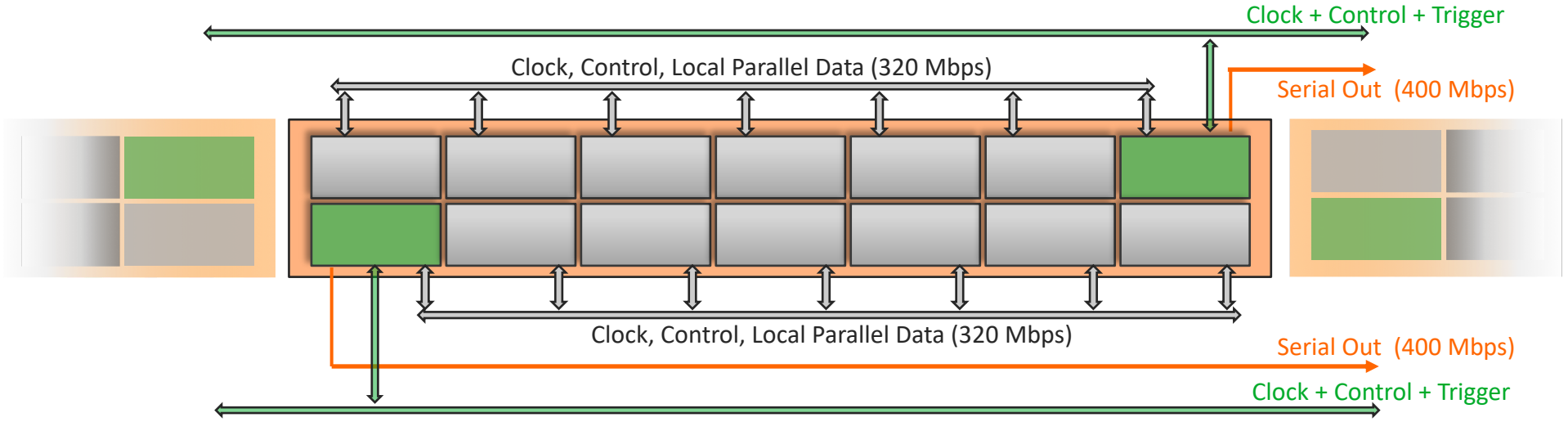
# Detector Modules with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, *shared* clock (40 MHz) and control (40 Mbps), individual data readout lines

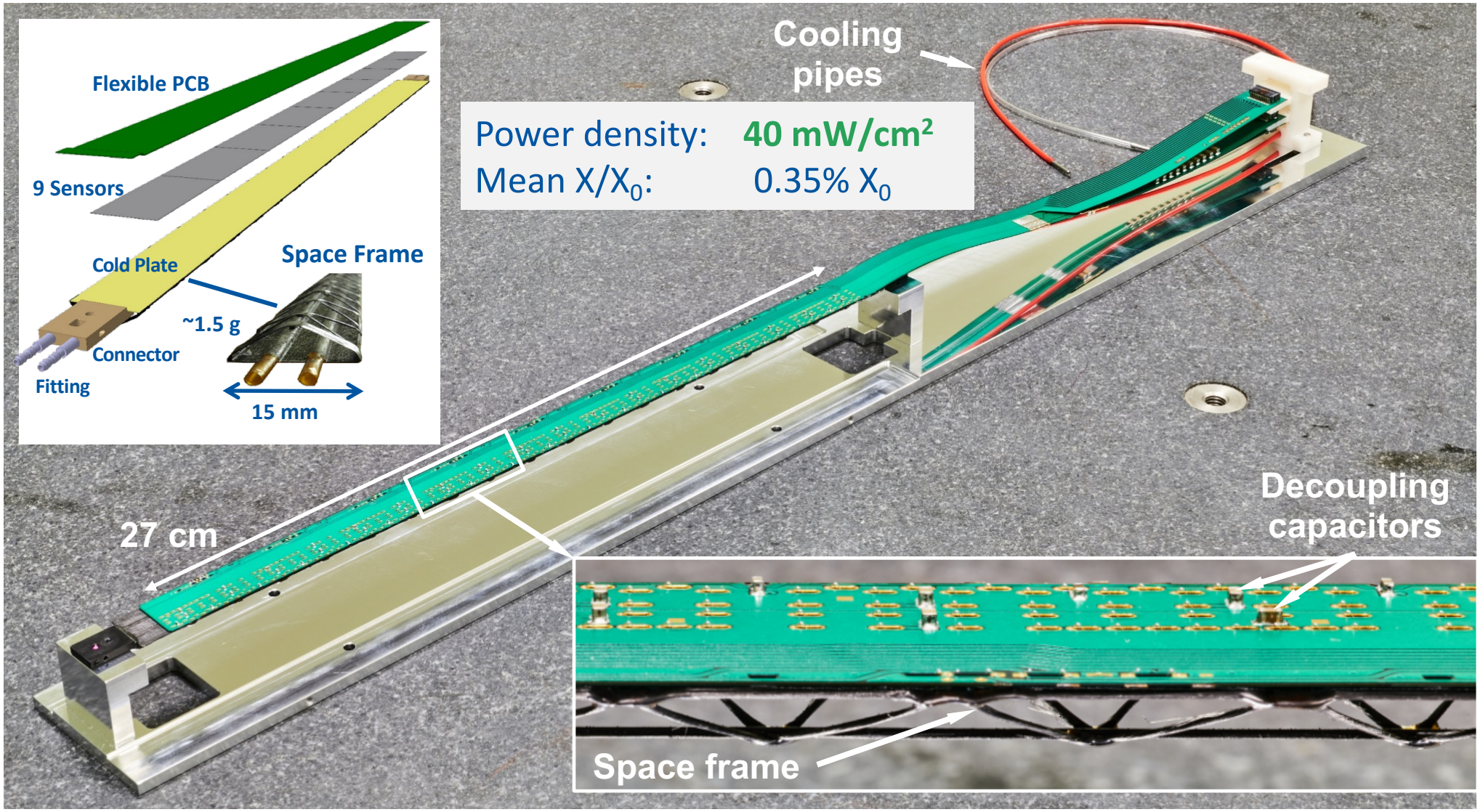



ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

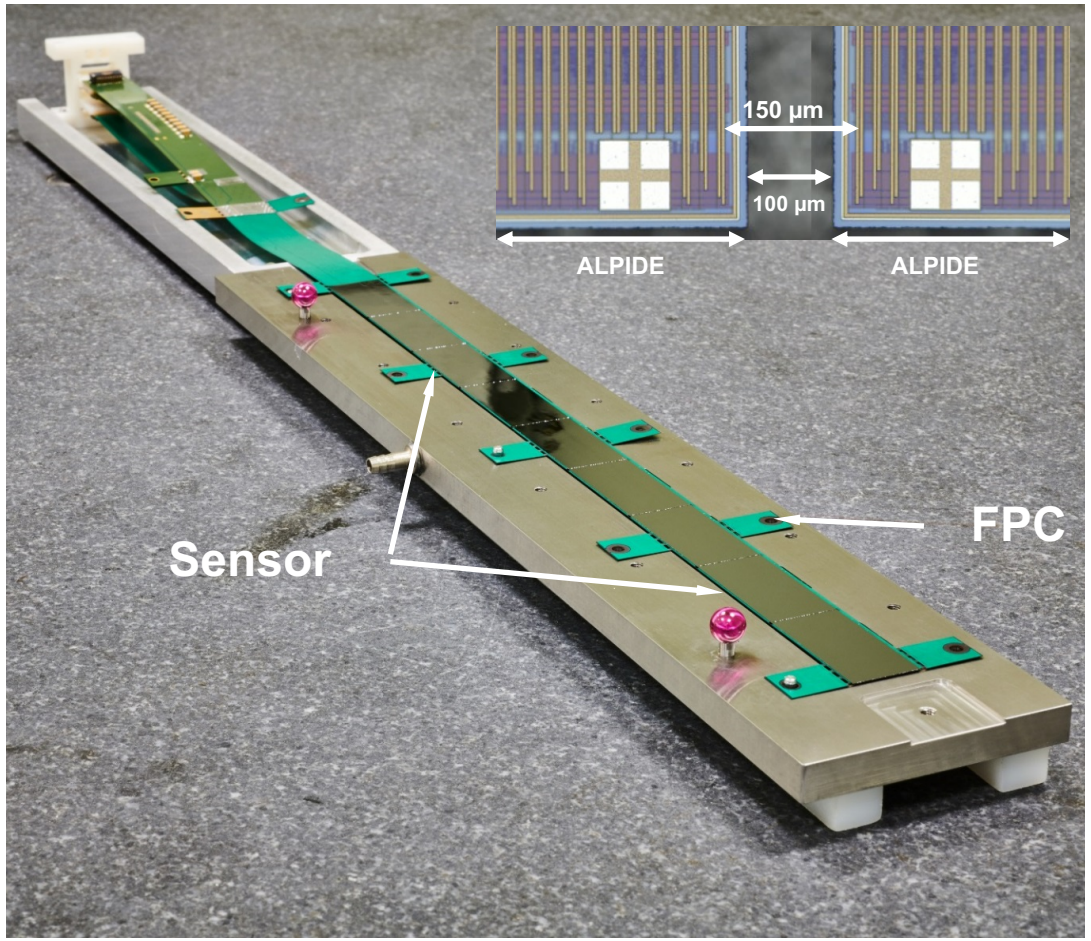
Only the Master interfaces to the external world and bridges control and data transfer

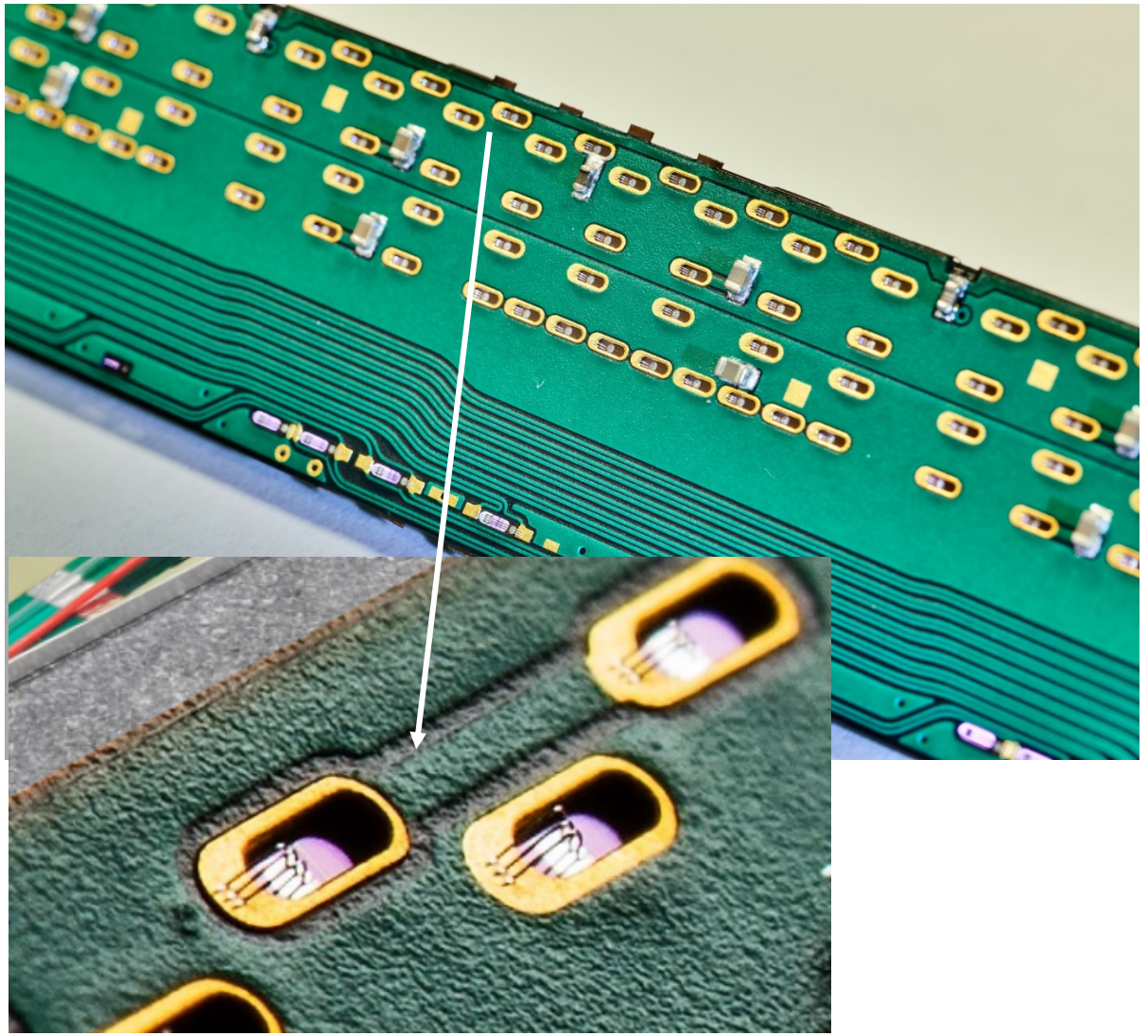


# Inner Barrel Stave



# Bonding through vias



# Material budget and thinning

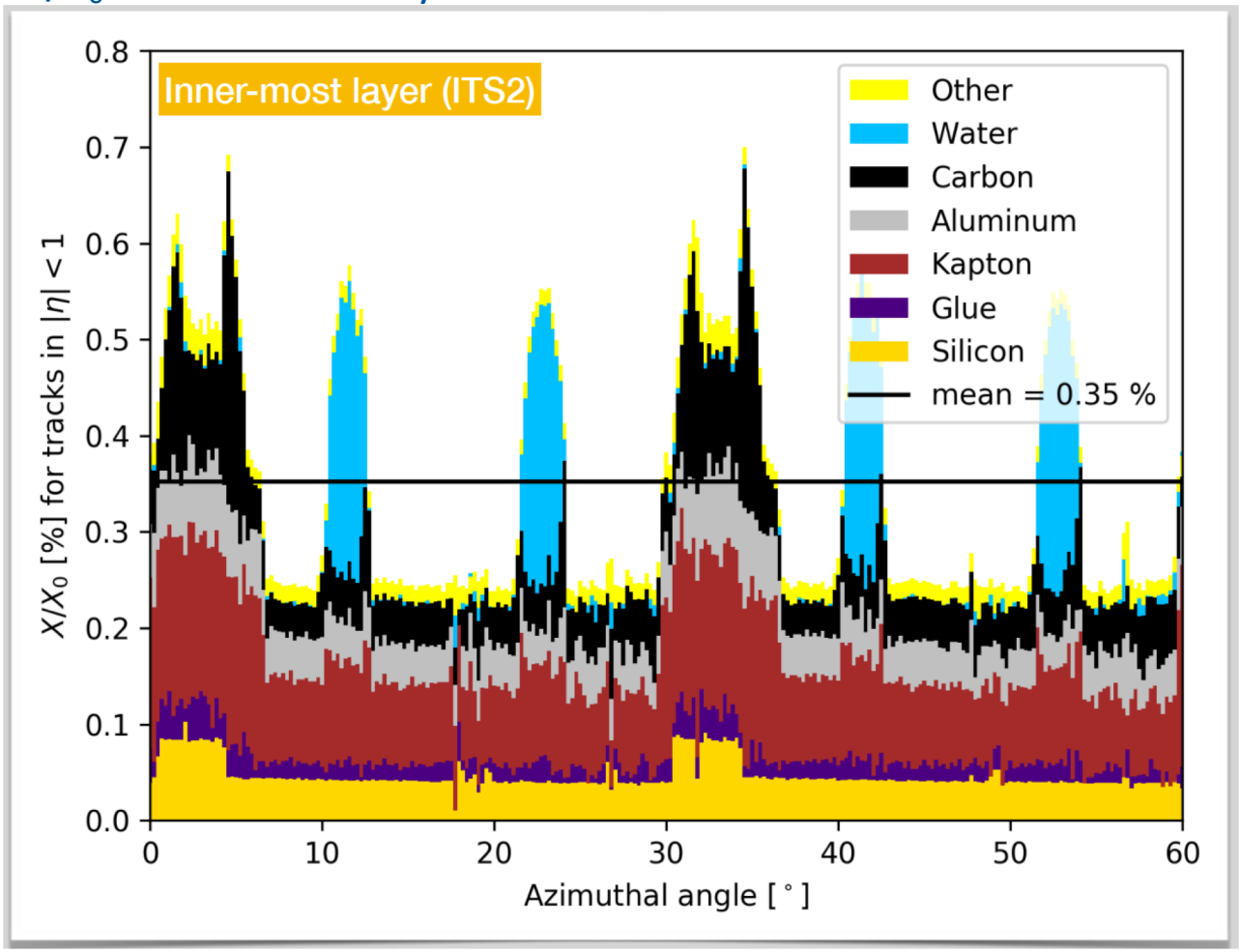
Wafer *thinning* after CMOS processing

Inner layers: 50 um

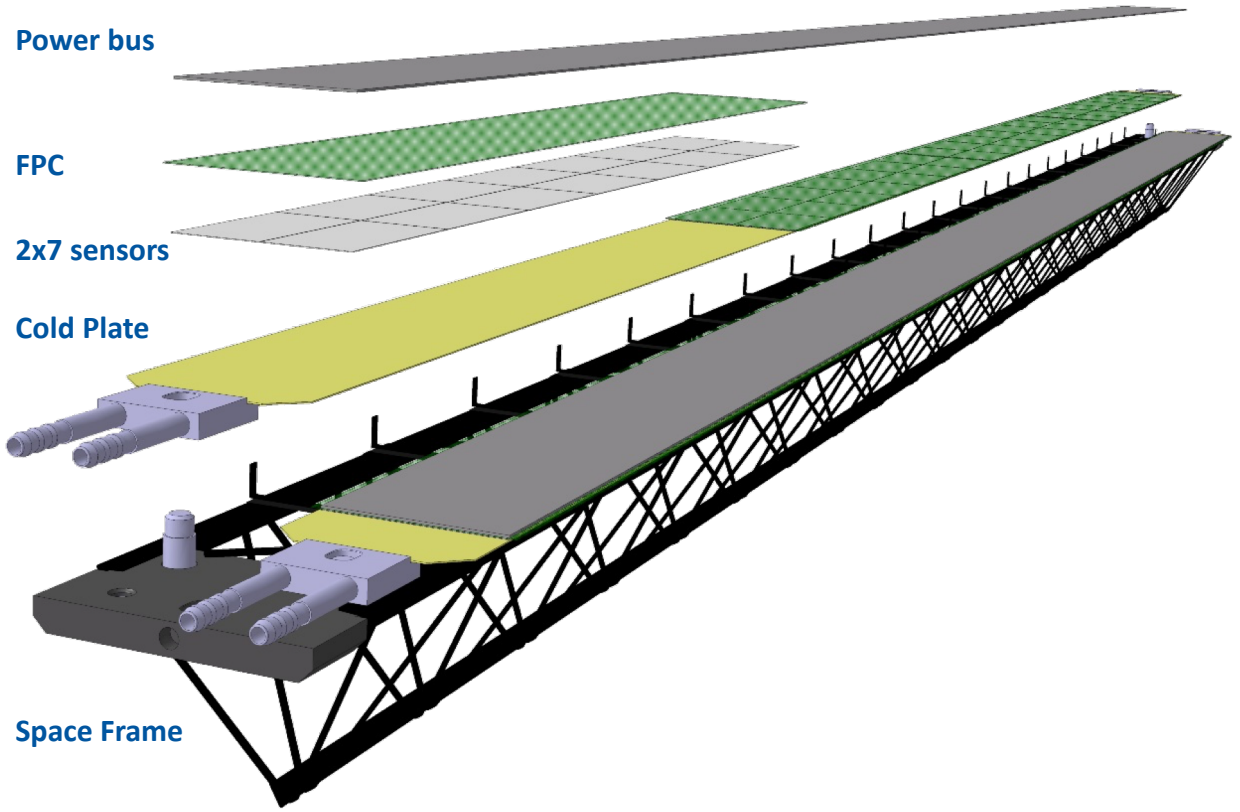
Outer layers: 100 um

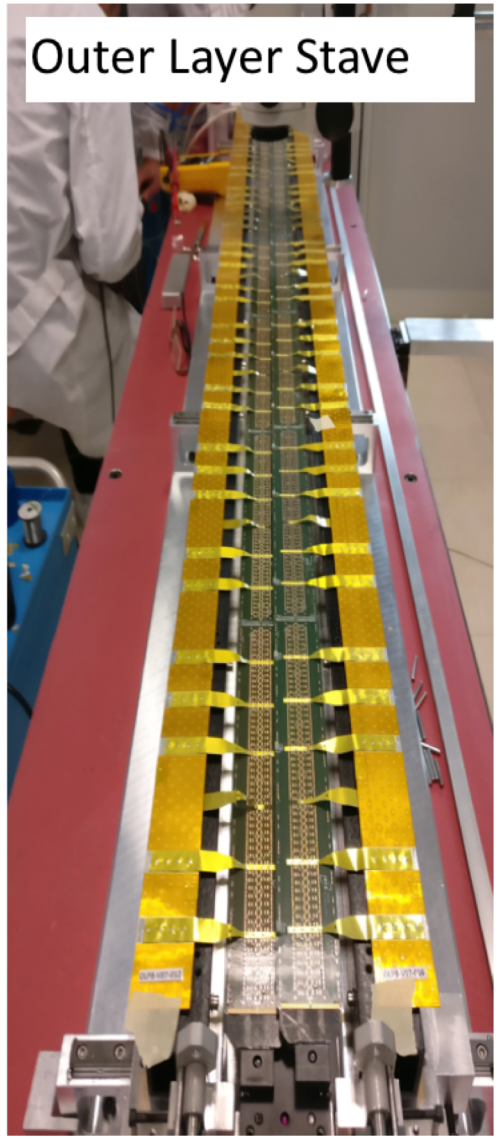
X/X0 /layer (ITS innermost three layers): 0.35%

$X/X_0$ for innermost layers

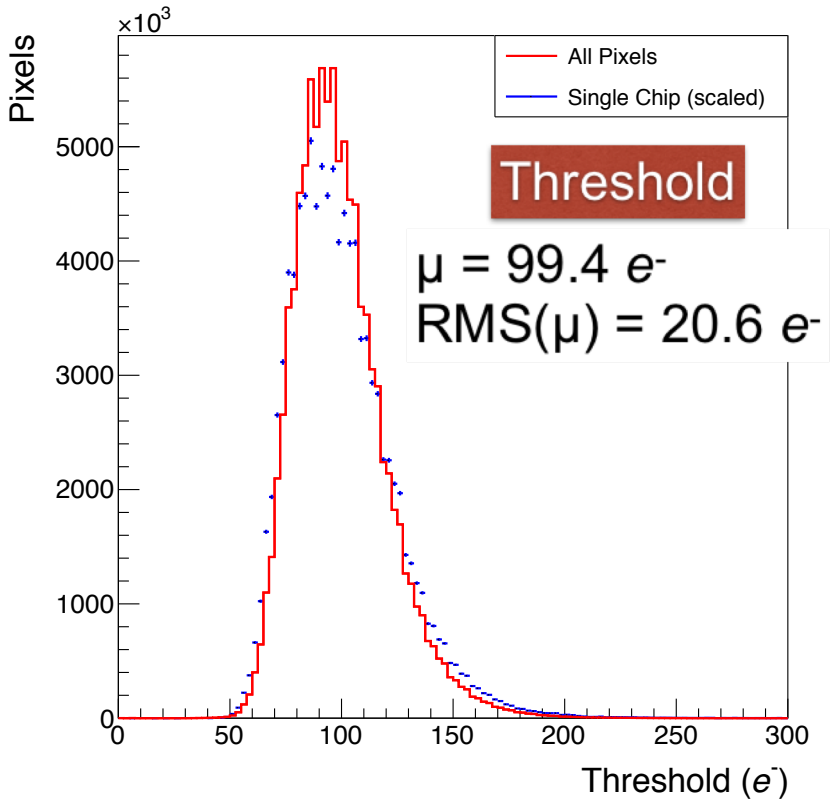


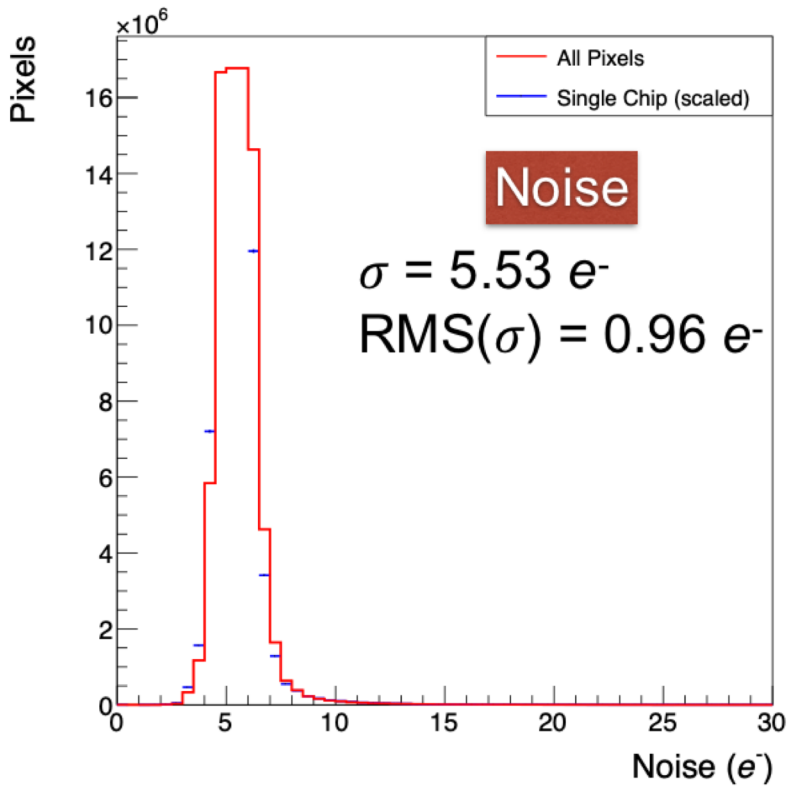
# Outer Barrel Stave

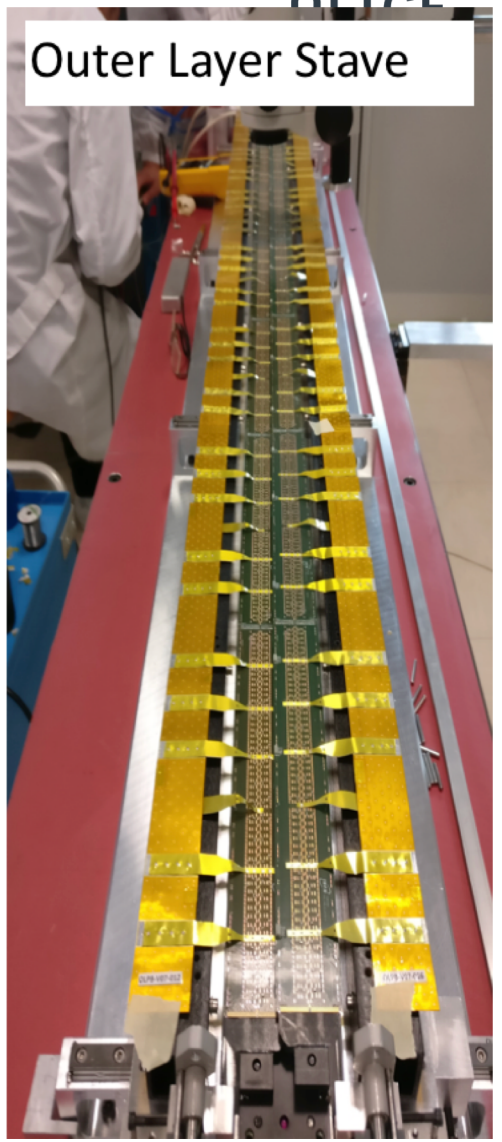


# ITS Outer Layer Stave – Thresholds and Noise

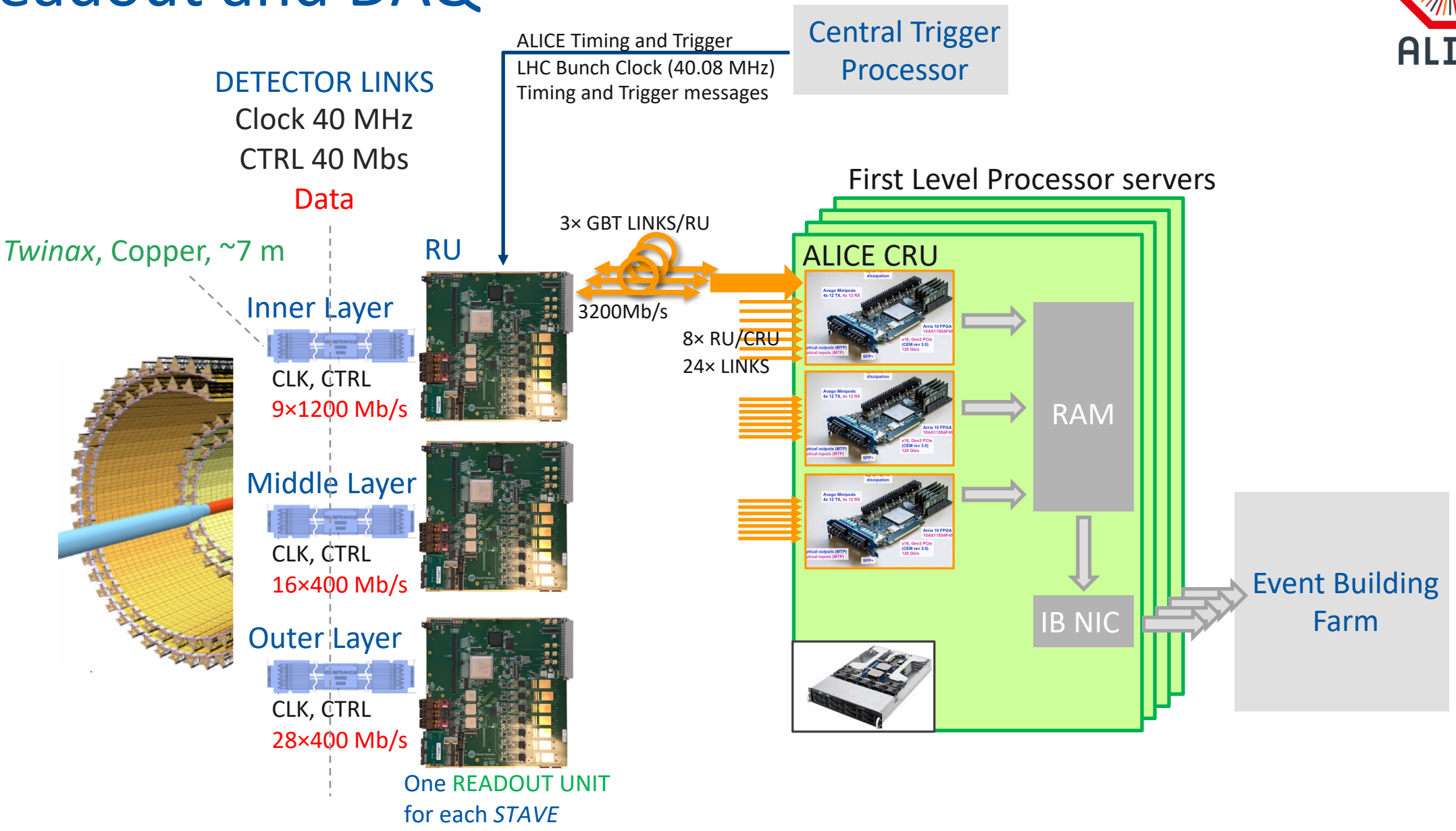


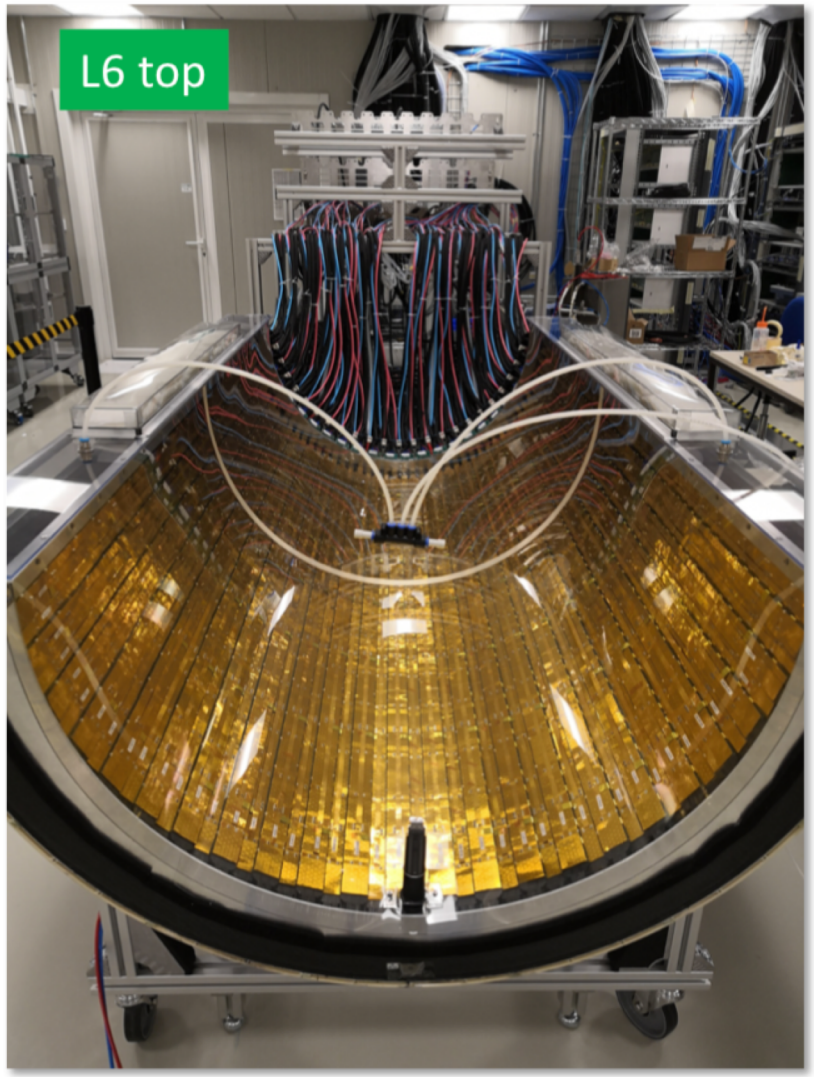



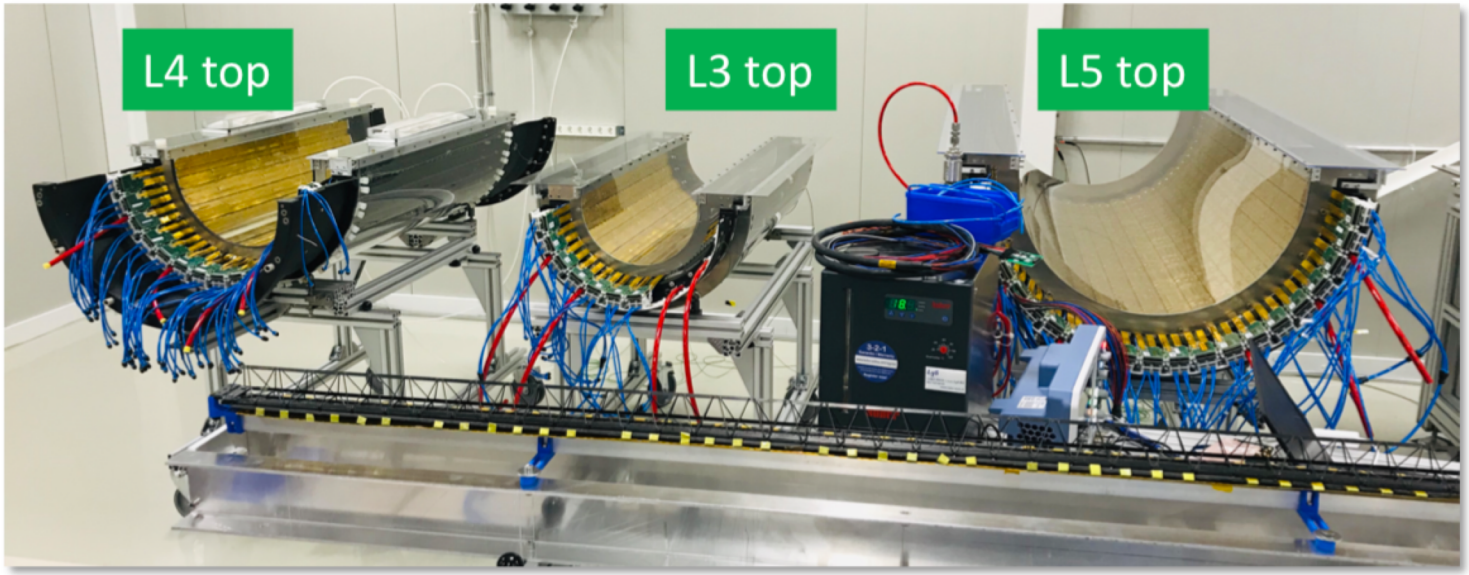

Middle Layer staves 84 cm long, 114 chips in 8 modules, 59 Mpixels
Outer Layer staves: 150 cm long, 196 chips in 14 modules, 103 Mpixels
Excellent noise and threshold uniformity maintained across the full stave (after chip-to-chip tuning)

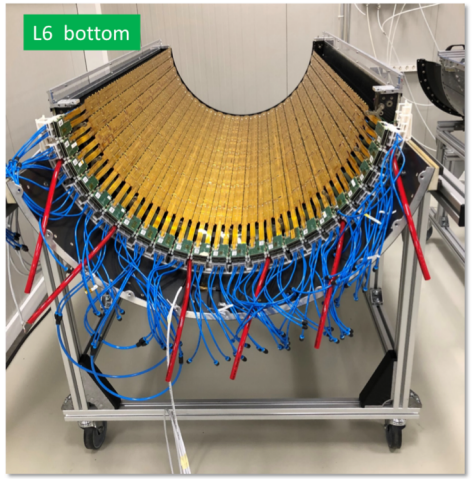
# Readout and DAQ



# Outer Barrel Half Layers




ITS and its Supply and Readout Systems are **completed** at date

Undergoing **commissioning** (in the clean room)

Transfer to the cavern over June, July and August 2020

# Summary

## ALPIDE Chip description

Technology, Architecture

Pixel characteristics, timing and readout features, Data rates

Power Consumption

## Key ALPIDE performance figures

## ALPIDE in ALICE ITS Modules

## Tried to target questions on sustainable flux and time resolution

Expected max muon flux of $5*10^5$ $cm^{-2}s^{-1}$ is 25% of peak flux in ITS

OK with 10 us strobe and 100 kHz frame rate

I think also OK in continuous mode with 5 us strobe duration and 200 kHz frame rate

Would give dual and triple sampling of hits, need dedicated links per chips and data filtering off-detector

# FURTHER REFERENCE

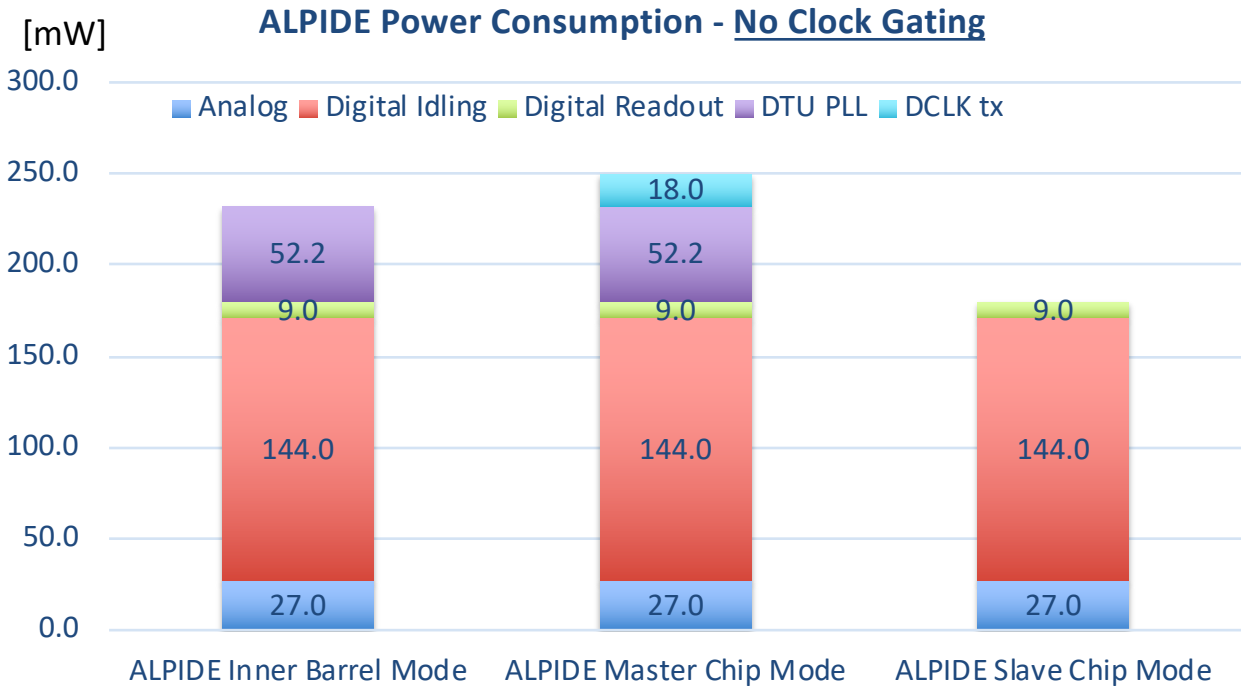
# ITS Chip General Requirements

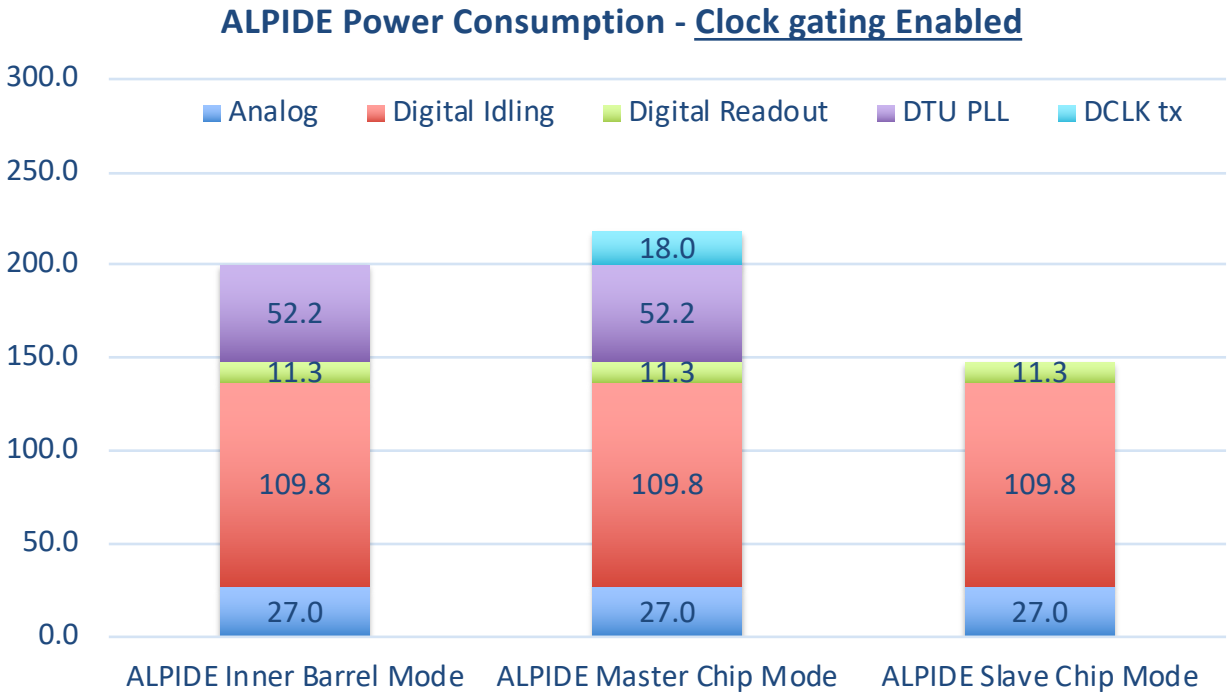
| Parameter | Inner Barrel | Outer Barrel |
|---|---|---|
| Chip size (mm x mm) | 15 x 30 | |
| Chip thickness (μm) | 50 | 100 |
| Spatial resolution (μm) | 5 | 10 (5) |
| Detection efficiency | > 99% | |
| Fake hit rate | $< 10^{-5}$ evt$^{-1}$ pixel$^{-1}$ (ALPIDE $<< 10^{-5}$) | |
| Integration time (μs) | < 30 (< 10) | |
| Power density (mW/cm$^2$) | < 300 (~35) | < 100 (~20) |
| TID radiation hardness (krad) (**) | 2700 | 100 |
| NIEL radiation hardness (1 MeV $n_{eq}$/cm$^2$) (**) | 1.7 x $10^{13}$ | 1.7 x $10^{12}$ |
| Readout rate, Pb-Pb interactions (kHz) | 100 | |
| Hit Density, Pb-Pb interactions (cm$^{-2}$) | 18.6 | 2.8 |

(*) In color: ALPIDE performance figure where above requirements

(**) 10x radiation load integrated over approved program (~ 6 years of operation)

# Typical Power Consumption Figures




Clock Gating OFF

Inner Barrel Mode: 51 mW/cm$^2$
Outer Barrel Average: 42 mW/cm2

Clock Gating ON

Inner Barrel Mode: 44 mW/cm$^2$
Outer Barrel Average: 35 mW/cm2

# Priority Encoder

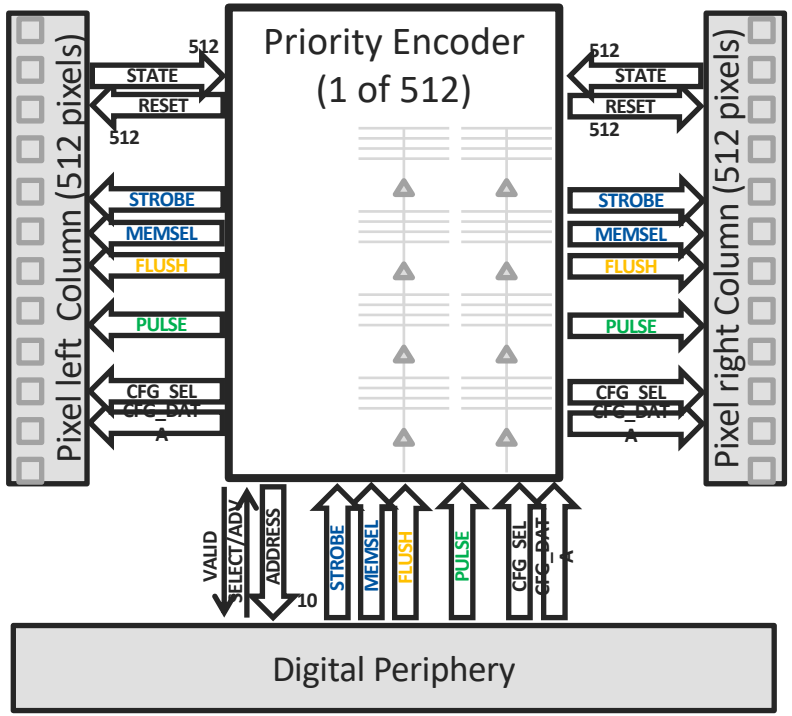
Encodes **ADDRESS** of first hit pixel of input **STATE** vector

Forwards **RESET** to hit pixel

Buffers global signals

**STROBEs, MEMSELs, FLUSHs, PULSEs**

Buffers **pixel configuration** signals



# Triggered and Continuous Readout Modes

## Triggered Mode

Randomly distributed STROBE pulses of short duration Θ(100 ns)

Scenario: external trigger commands derived from trigger system

*Busy violation* trigger commands still acknowledged with Chip Empty Frame response, e.g. once MEB is full

## Continuous Mode

Periodic and repeating STROBE intervals, duration 1 – 5 us

*Flush* oldest event when MEB is becoming full and start new strobe interval. (Priority to latest framing interval)

## Generation of STROBE

Duration programmable 50 ns -> 1.6 ms *(both modes)*

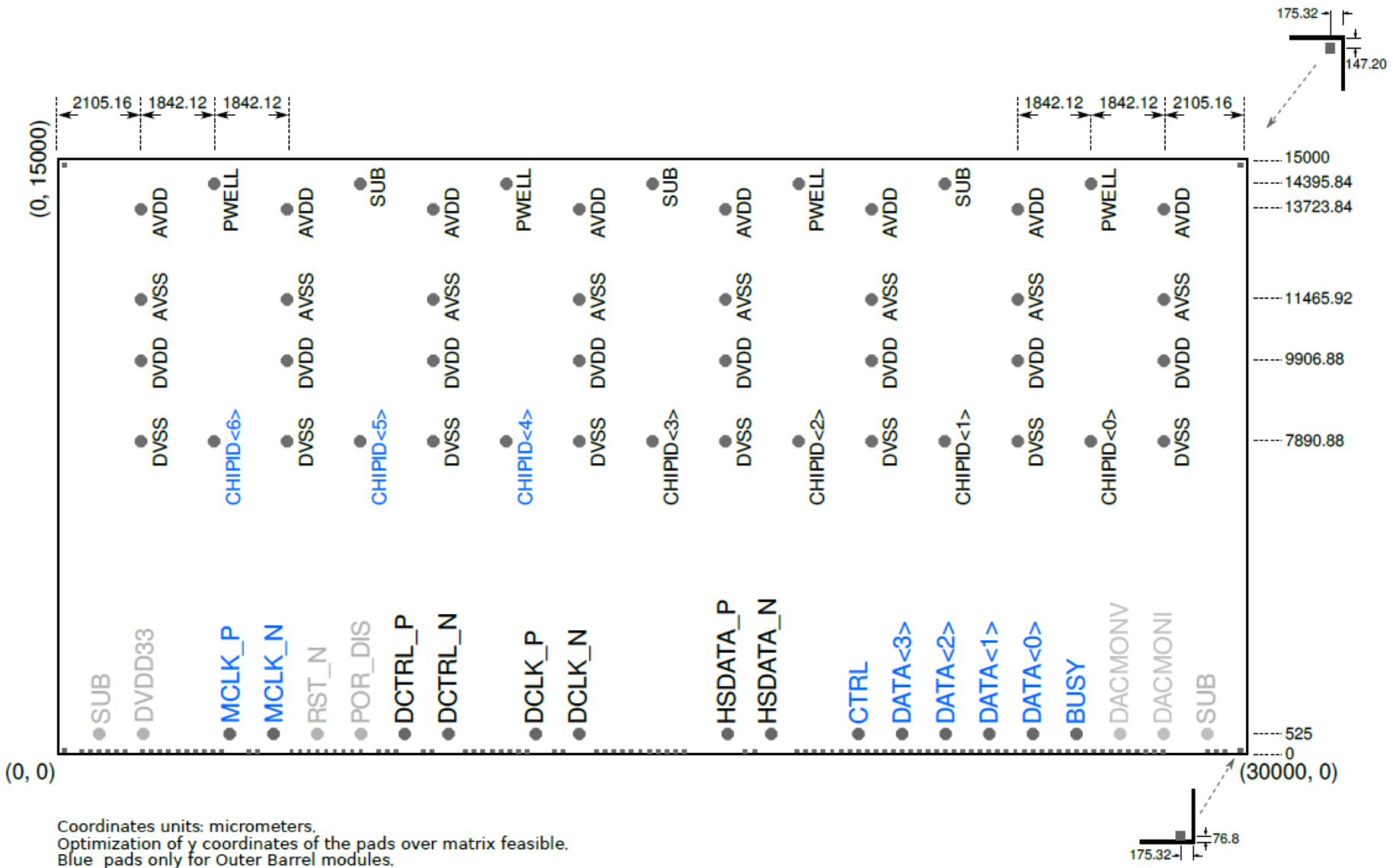
Start on external commands or internal sequencer *(both modes)*

## BUSY status

Triggered mode: *MEBs full* or *periphery FIFOs almost full*

Continuous mode: *MEBs almost full* or *periphery FIFOs almost full*

# ALPIDE Pinout




Coordinates units: micrometers.
Optimization of y coordinates of the pads over matrix feasible.
Blue pads only for Outer Barrel modules.
Light gray pads can be left unconnected and could disappear from the chip.