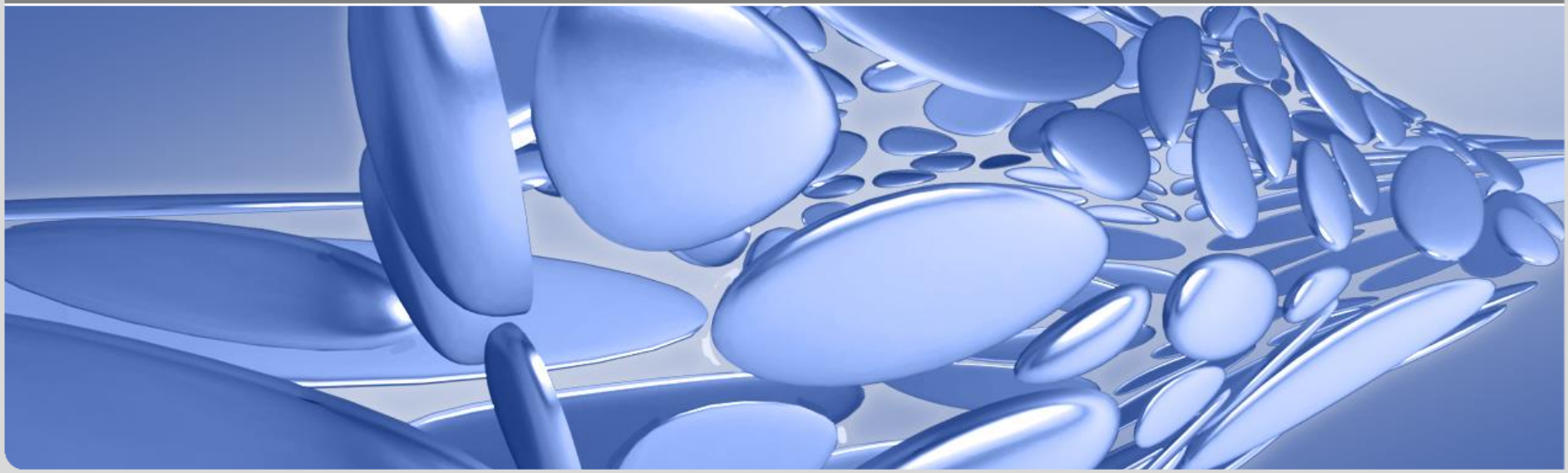
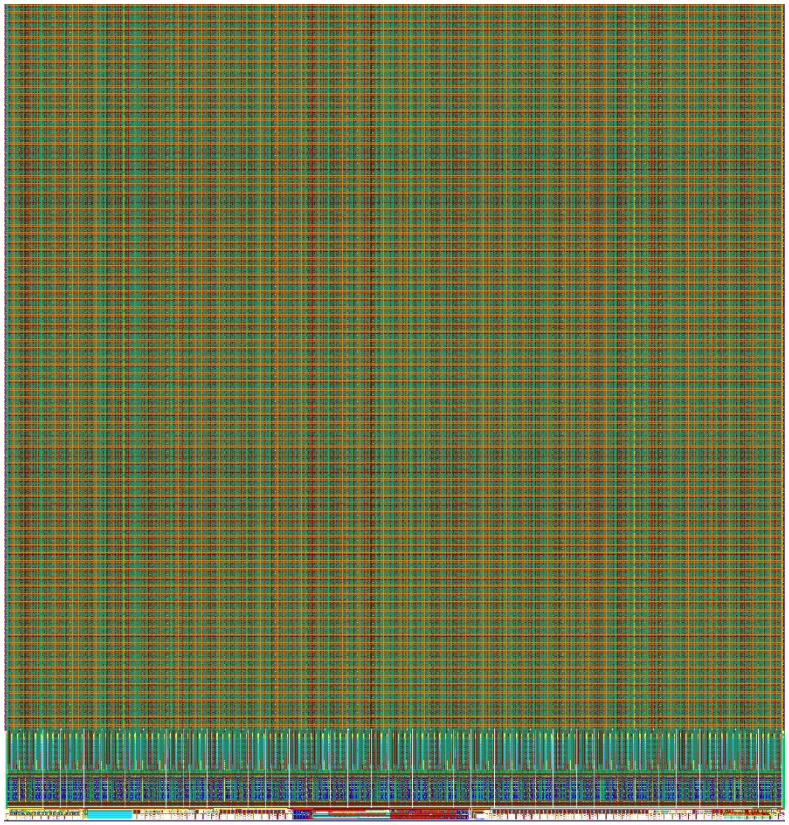
Two reticle size monolithic pixel detectors ATLASPIX3 and MuPix10

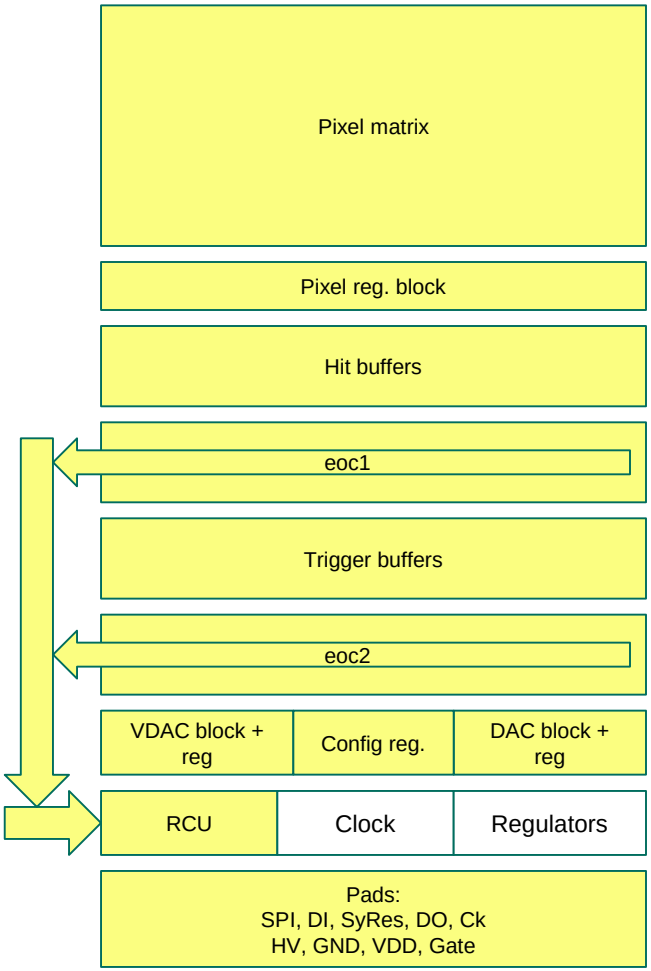
Ivan Peric



- ATALSPIX3
- HVCMOS sensor
- The chip has been implemented in 180nm HVCMOS technology of TSI. 200Ωcm wafers have been used.
- Received in September 2019
- Triggered and triggerless readout possible via two concurrent readout structures
- Several configuration methods for different wire count constraints (serial, SPI, single line)
- Data interface similar as RD53
- **Triggered readout can be used as continuous readout with hit sorting**
- Interface:
- Input CMD line (used for clock generation, L1 triggering with trigger tag, configuring and readback of configuration), like RD53
- Supports serial powering
- Size: 20.2mm x 21mm
- Radiation hard design with SEU tolerant memory



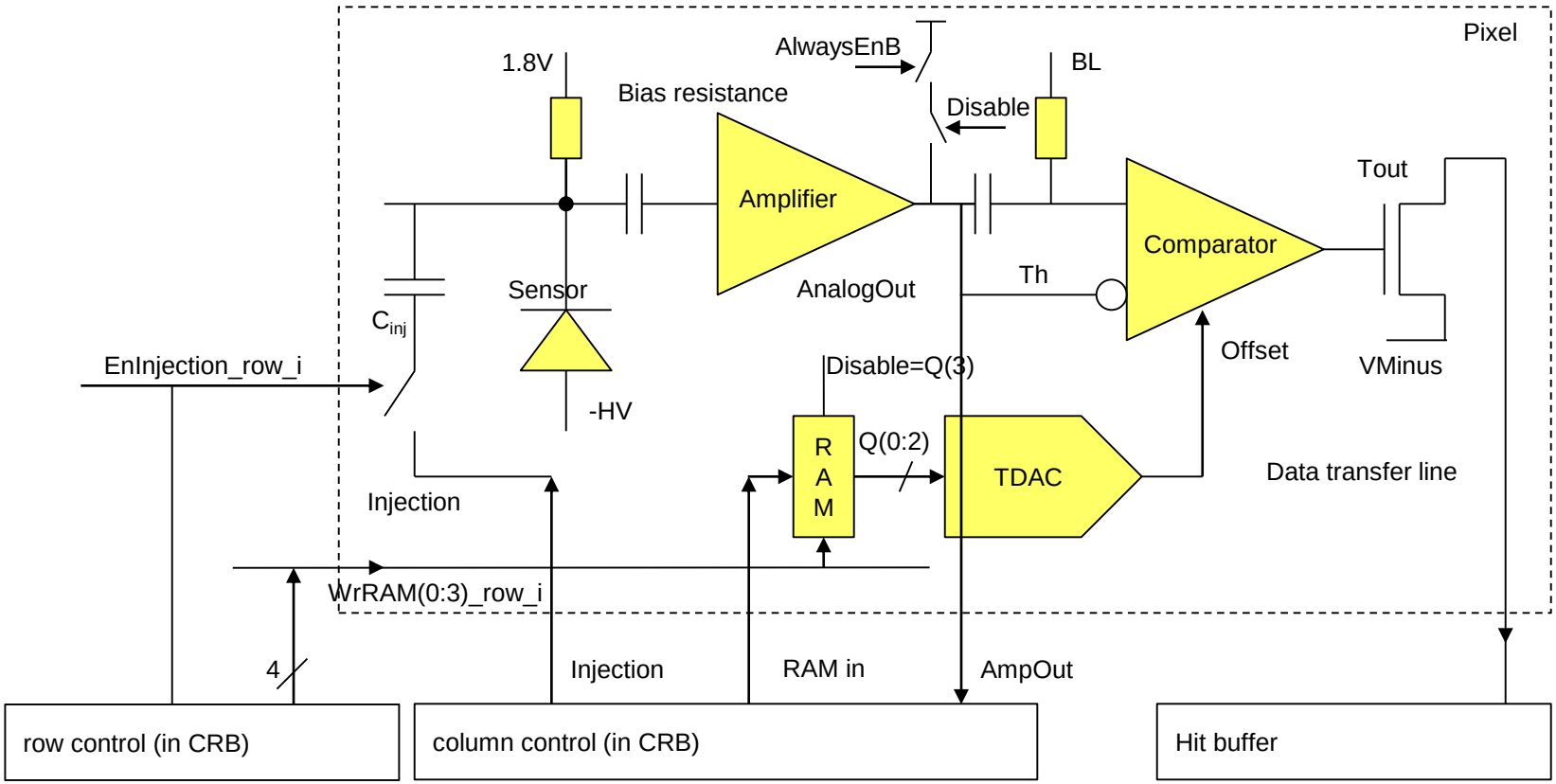
- ATLASPIX3 has a pixel matrix with 132 columns and 372 rows. Pixel size is x = 150µm, y = 50µm. The chip size is x = 20.2mm, y = 21mm.
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two end of column (EoC) blocks. EoC1 is attached to hit buffers and EoC2 to trigger buffers.



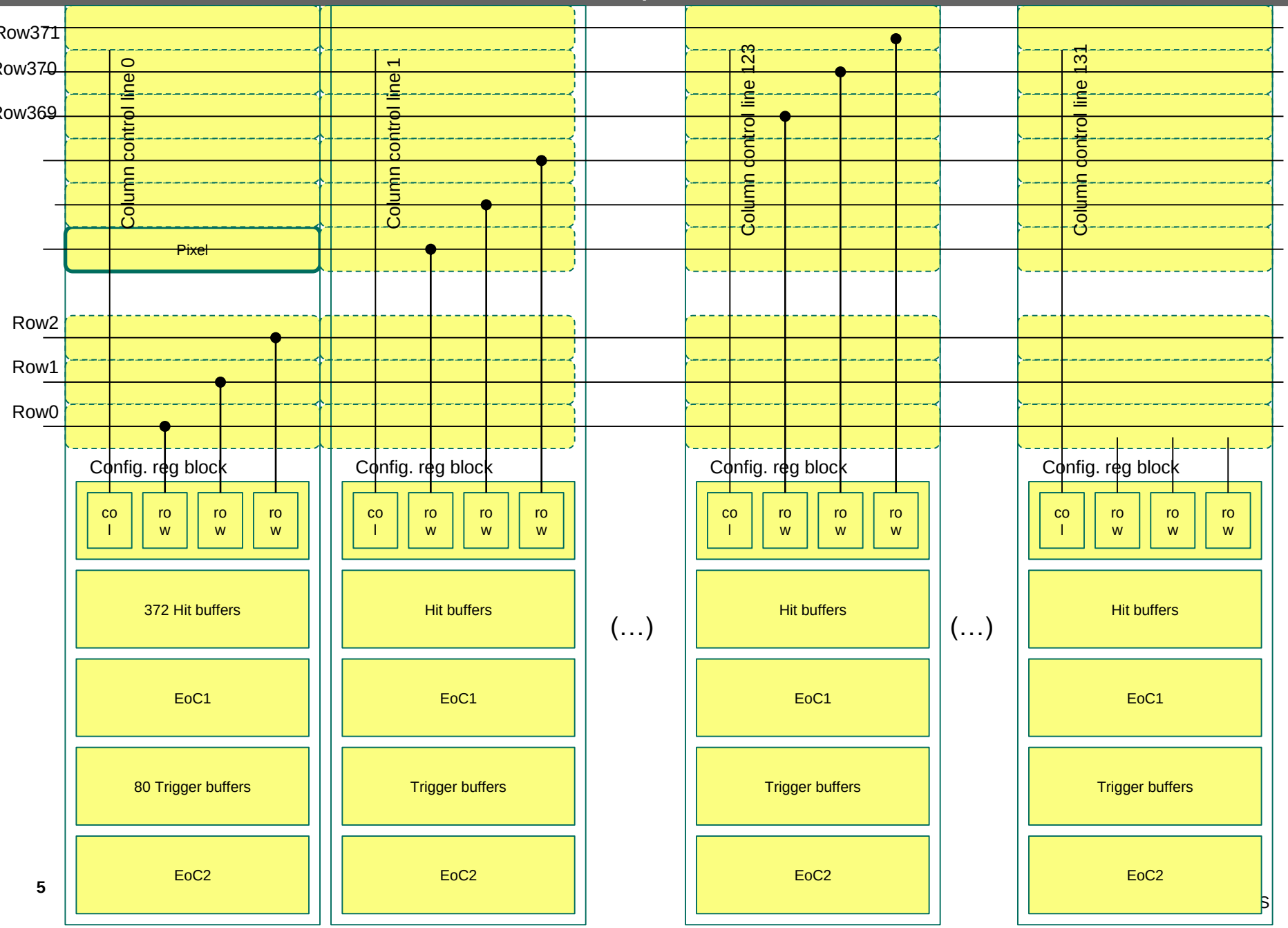
Pixel size (x, y): 150µm x 50µm
Matrix size: 132 x 372

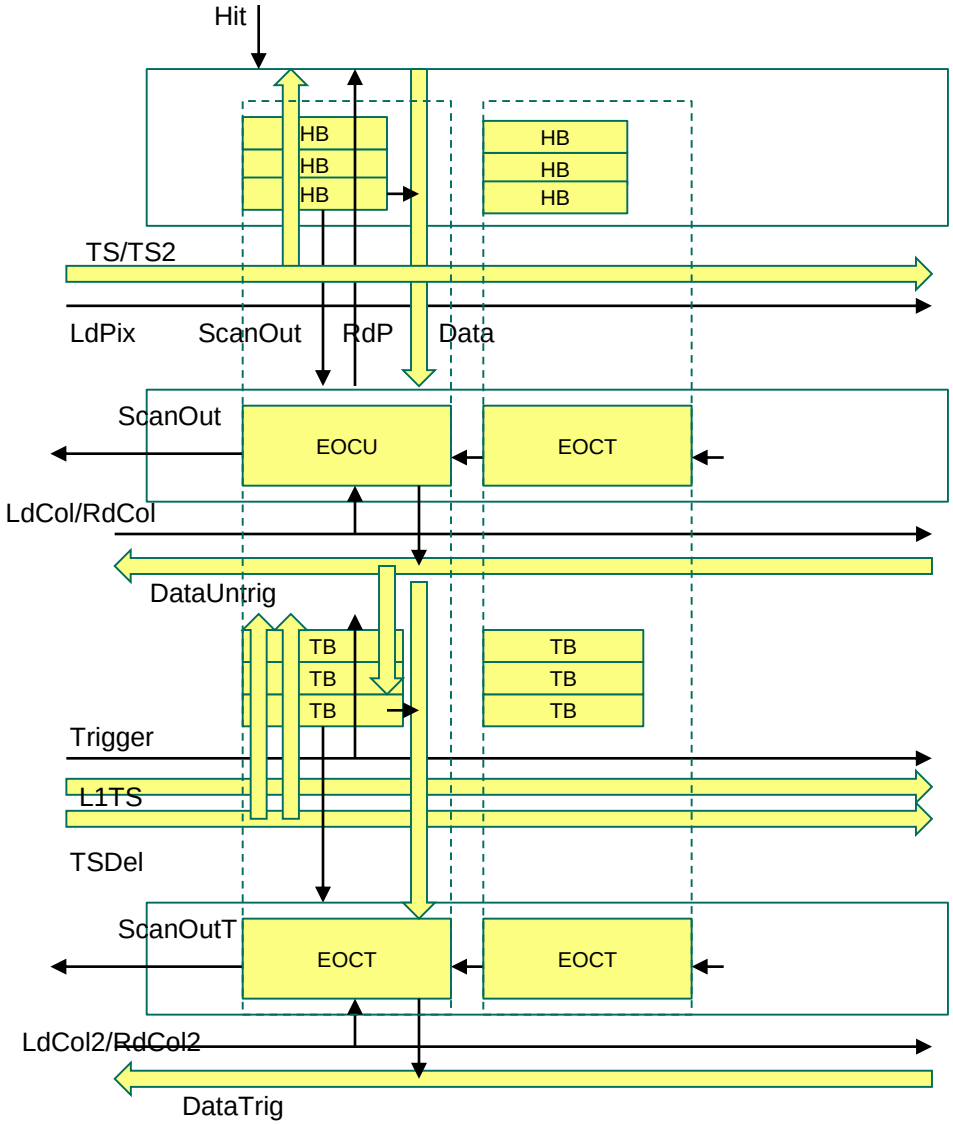
Time stamp: 10 bits, ToT time stamp: 7 bits
Programmable TS. frequency: up 160MHz (untriggered), 40MHz (triggered)
Output:
Triggered: Aurora 66/64 (Max rate 40MHits/s)
Untriggered: 8b10b (Max rate 20MHits/s)

- The pixel contains a deep n-well and the electronics that is inside the n-well. N-well to p-substrate diode is used as sensor.
- Pixel contains sensor diode, charge sensitive amplifier, comparator, threshold tune DAC, RAM for tune bits (3) and disable bit and output driver
- The outputs of the pixels are transmitted to the column periphery (long metal lines)

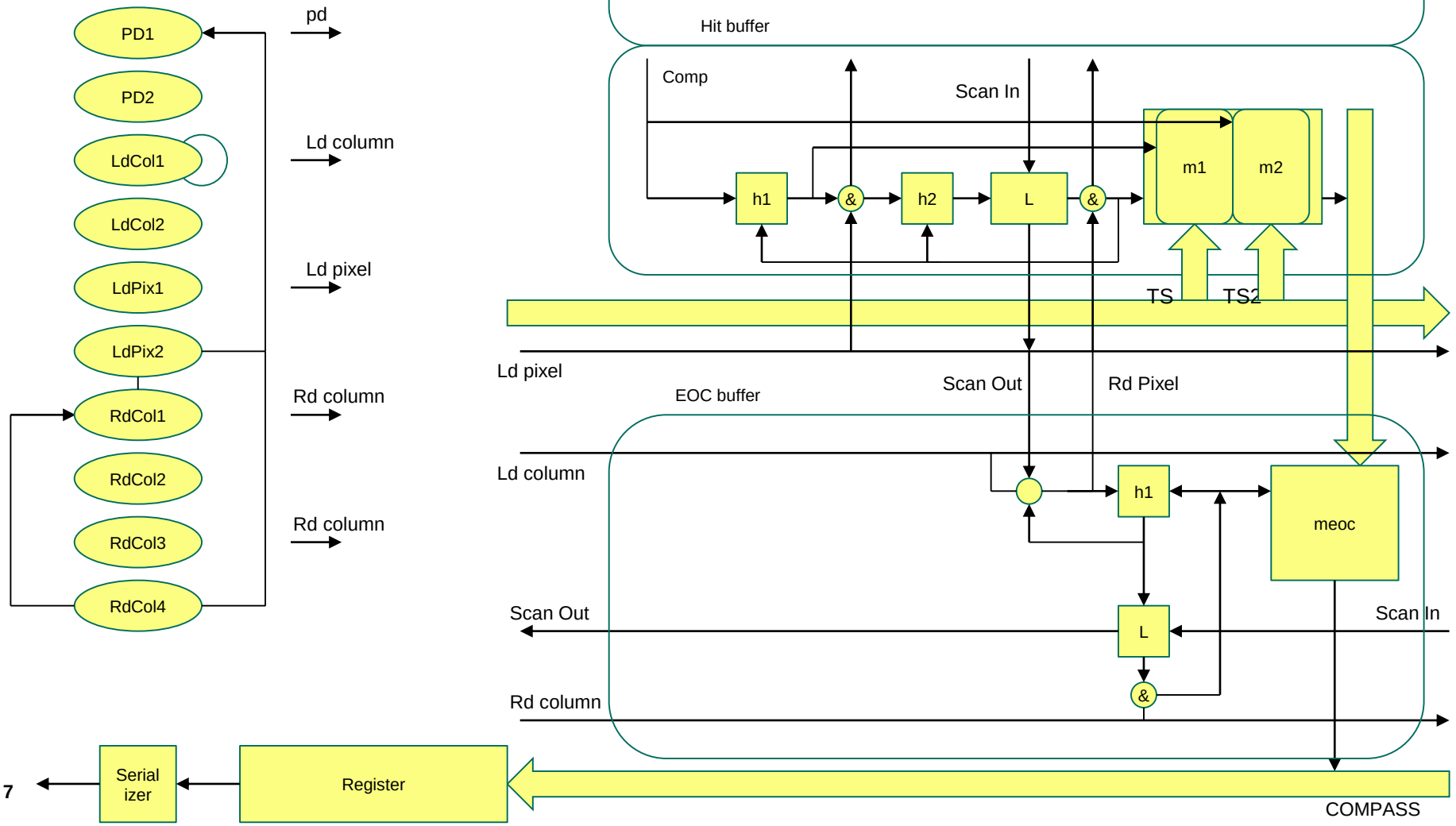


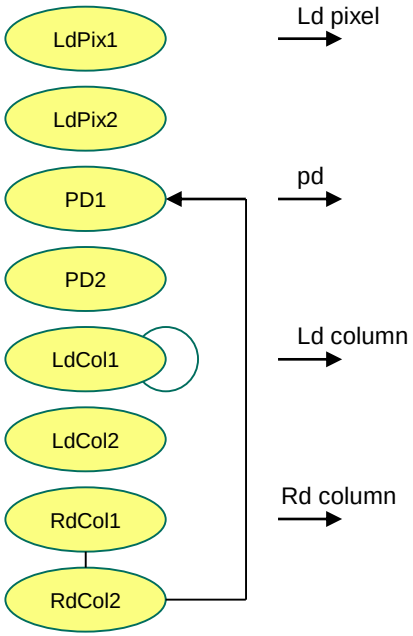
Chip architecture

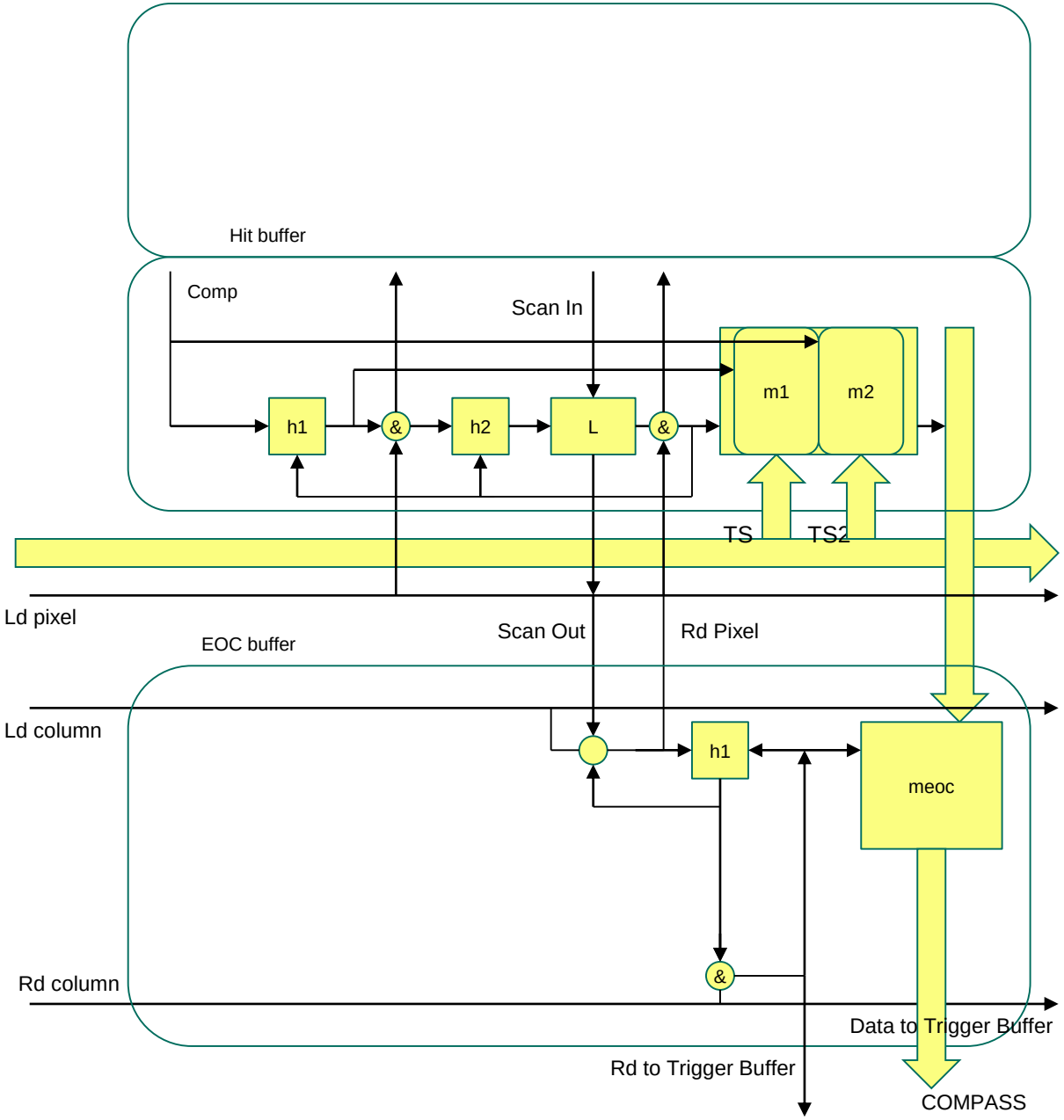


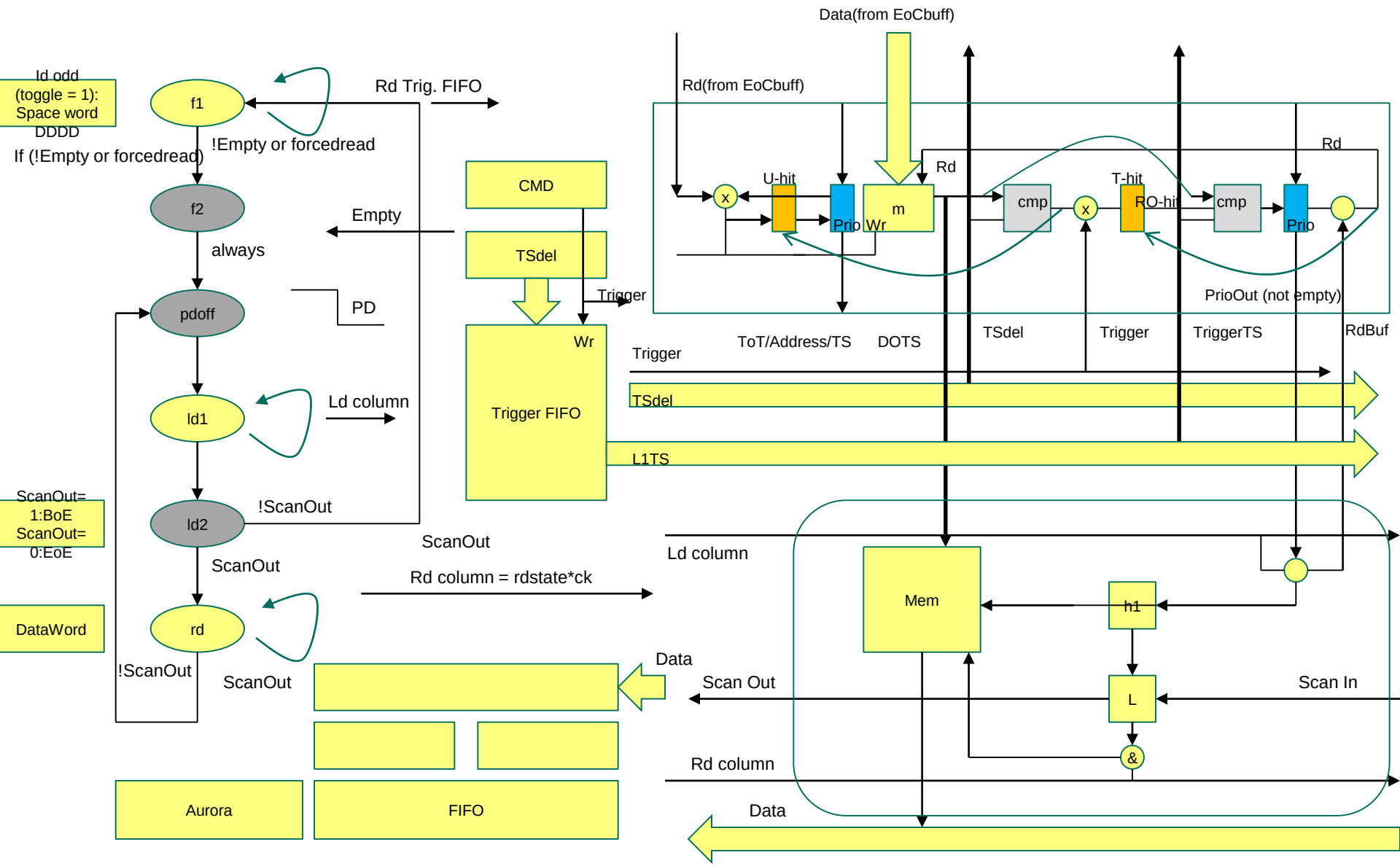

Hit
HB
HB
HB
HB
HB
HB
TS/TS2
LdPix
ScanOut
RdP
Data
ScanOut
EOCU
EOCT
LdCol/RdCol
DataUntrig
TB
TB
TB
TB
TB
TB
Trigger
L1TS
TSDel
ScanOutT
EOCT
EOCT
LdCol2/RdCol2
DataTrig

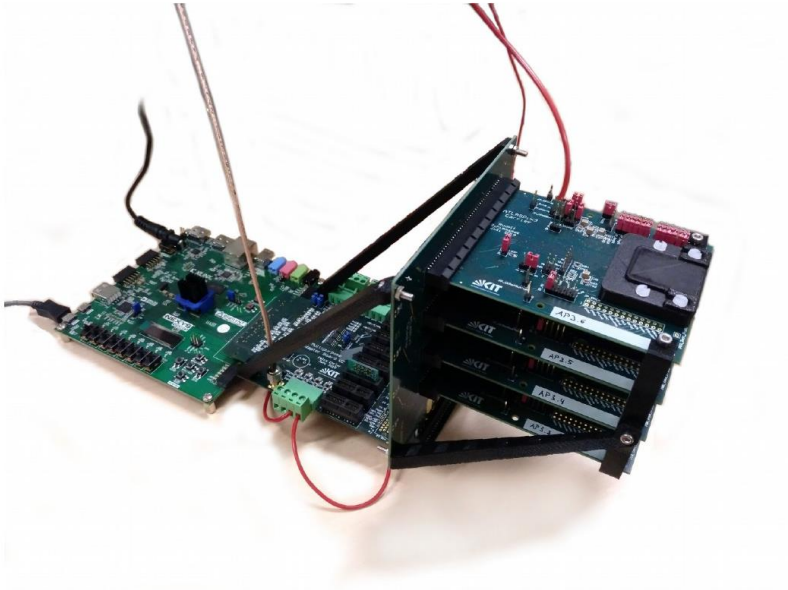
- …

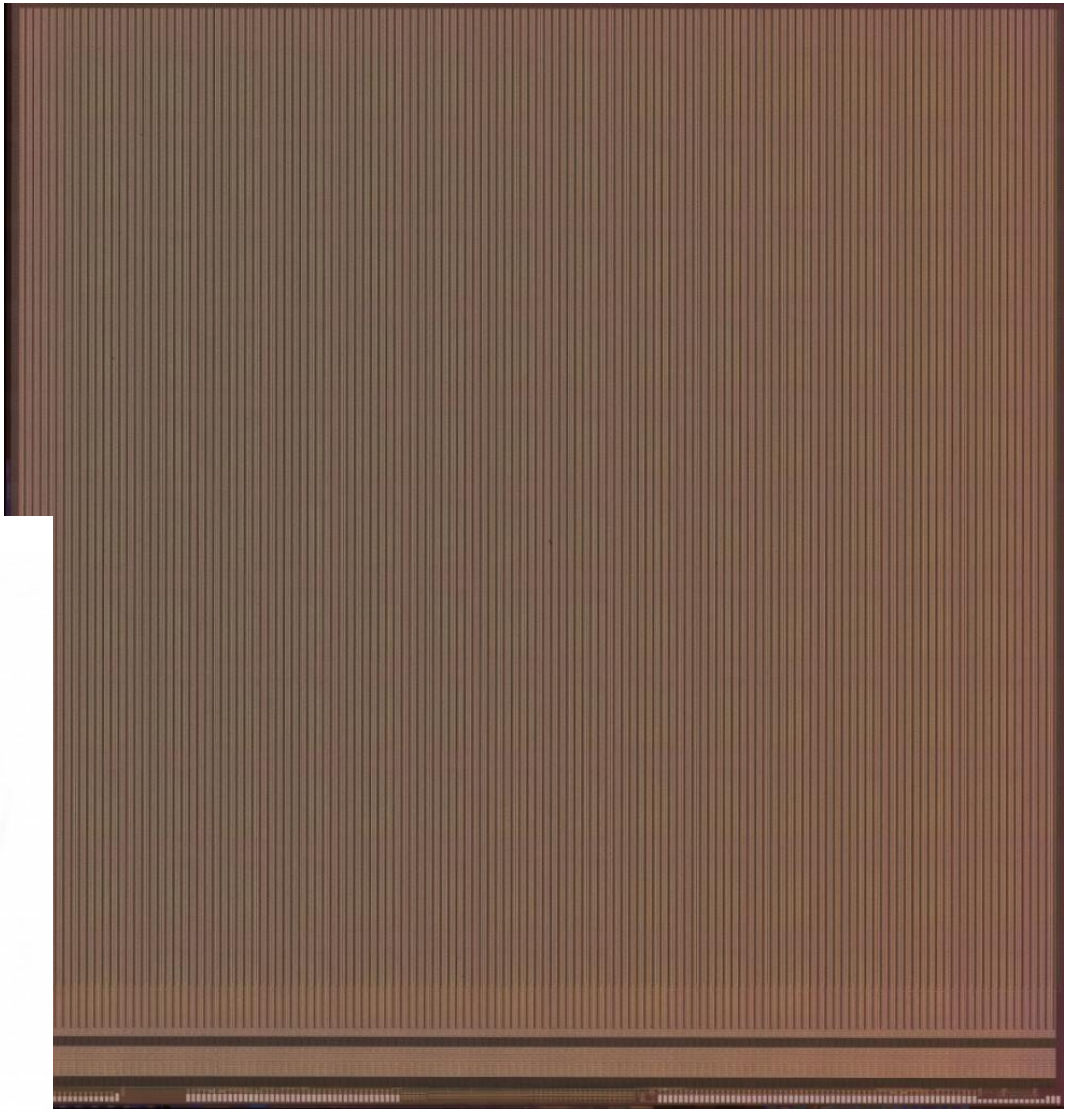

PD1
PD2
LdCol1
LdCol2
LdPix1
LdPix2
RdCol1
RdCol2
RdCol3
RdCol4
pd
Ld column
Ld pixel
Rd column
Rd column
Hit buffer
Comp
Scan In
h1
&
h2
L
&
m1
m2
TS
TS2
Ld pixel
Scan Out
Rd Pixel
EOC buffer
Ld column
h1
meoc
Scan Out
L
Scan In
&
Rd column
Serial izer
Register
COMPASS

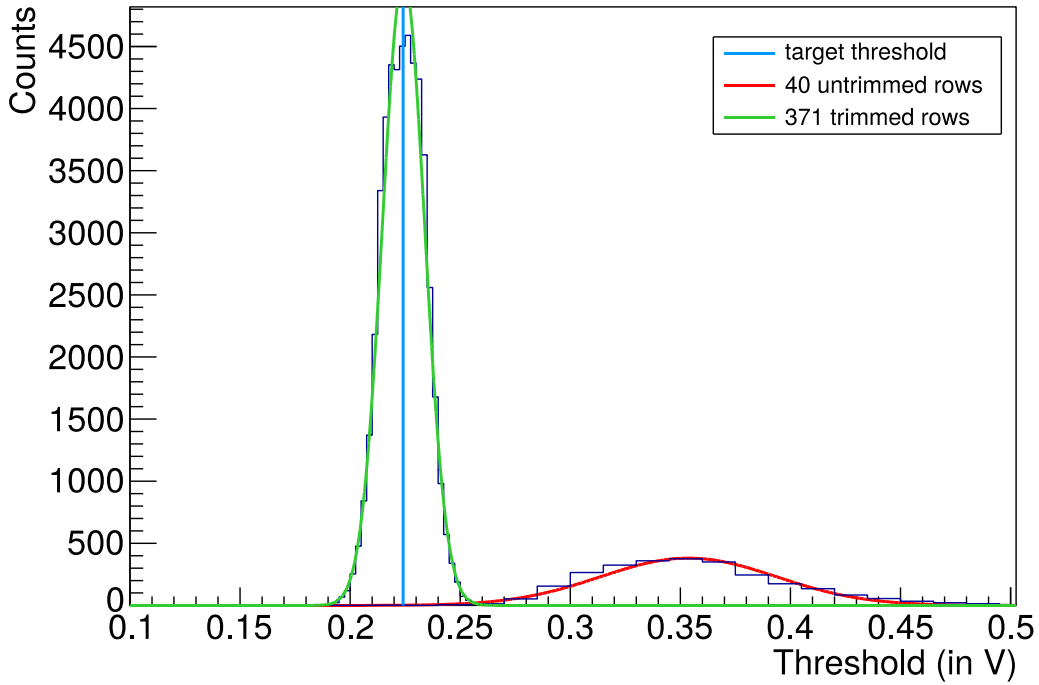

LdPix1
LdPix2
PD1
PD2
LdCol1
LdCol2
RdCol1
RdCol2
Ld pixel
pd
Ld column
Rd column


Hit buffer
Comp
Scan In
h1
&
h2
L
&
m1
m2
TS
TS2
Ld pixel
Scan Out
Rd Pixel
EOC buffer
Ld column
h1
meoc
&
Rd column
Data to Trigger Buffer
Rd to Trigger Buffer
COMPASS

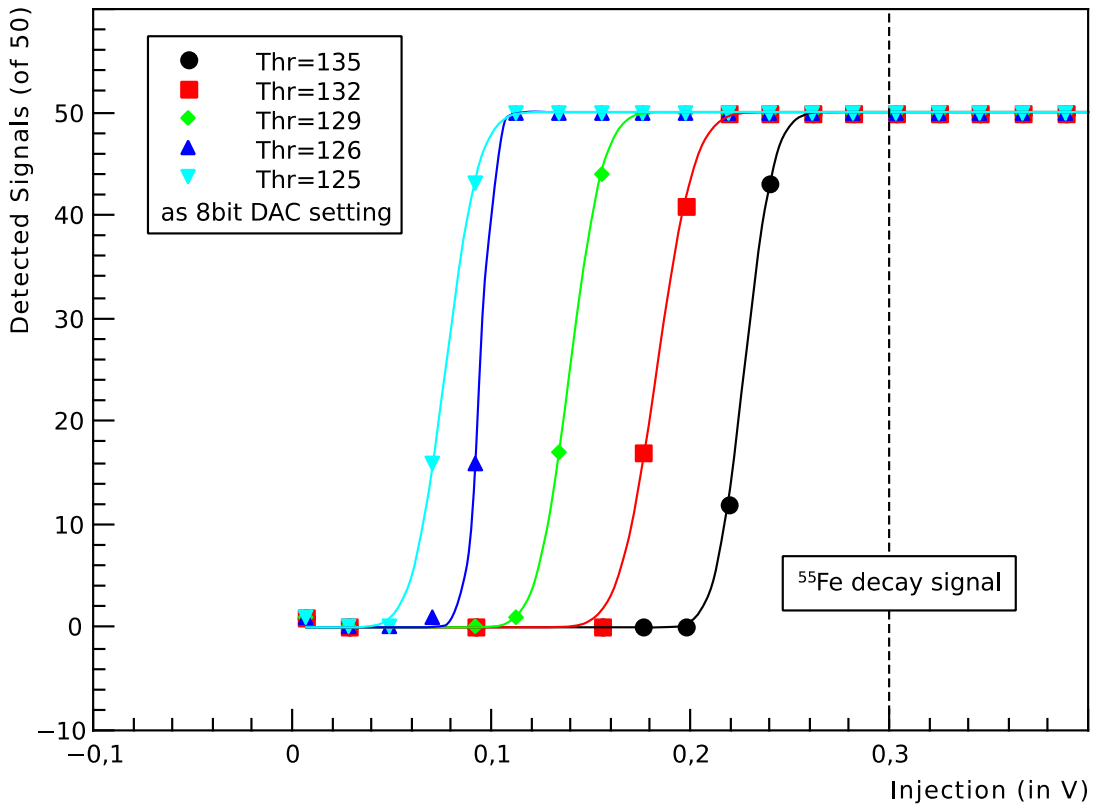

Id odd
(toggle = 1):
Space word
DDDD
If (!Empty or forcedread)
f1
Rd Trig. FIFO
!Empty or forcedread
f2
always
Empty
CMD
TSdel
Trigger
PD
pdoff
Wr
Trigger FIFO
Ld column
ld1
ScanOut=
1:BoE
ScanOut=
0:EoE
!ScanOut
ld2
ScanOut
ScanOut
Rd column = rdstate*ck
DataWord
rd
!ScanOut
ScanOut
Aurora
FIFO
Data(from EoCbuff)
Rd(from EoCbuff)
Rd
U-hit
Prio
Wr
m
T-hit
RO-hit
cmp
Prio
PrioOut (not empty)
ToT/Address/TS
DOTS
TSdel
Trigger
TriggerTS
RdBuf
Trigger
TSdel
L1TS
Ld column
Mem
h1
Data
Scan Out
L
Scan In
&
Rd column
Data

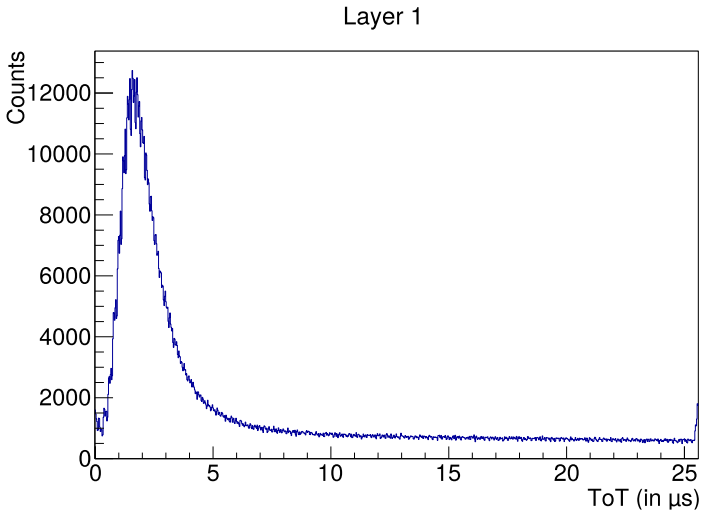


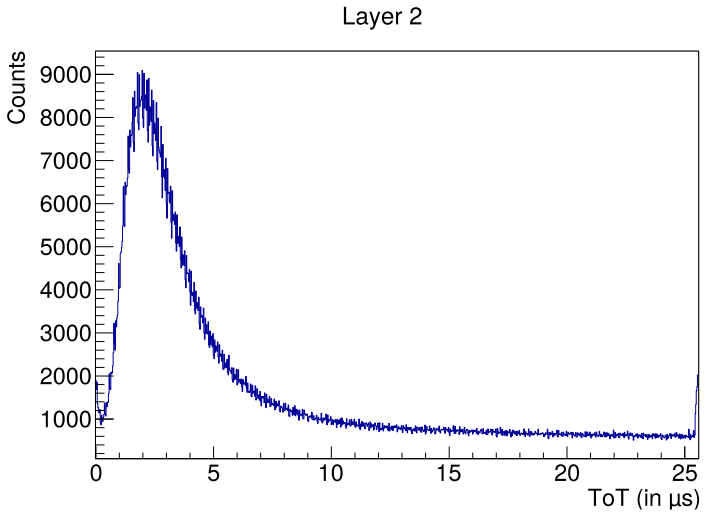


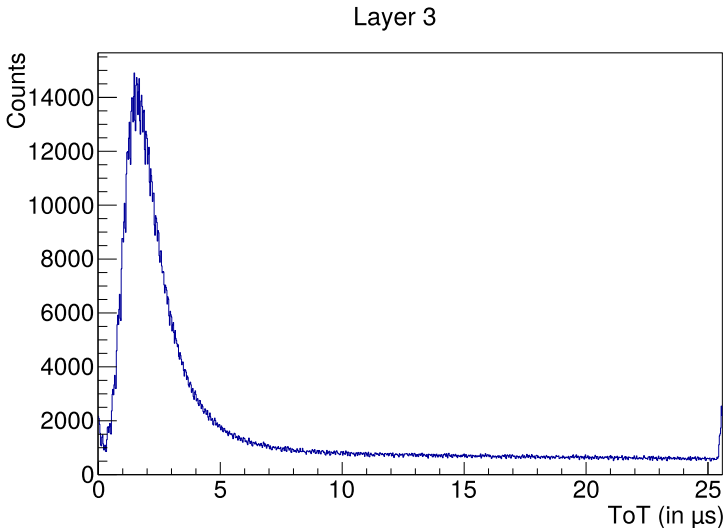


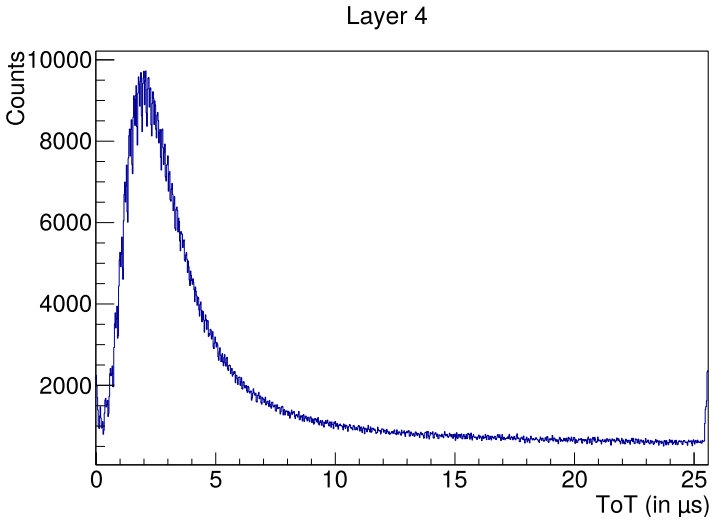
Sigma dispersion: 52e- (9.6mV) @ 1200e- threshold (inj. Voltage 220mV)


Detected Signals (of 50)
50
40
30
20
10
0
−10
−0,1
0
0,1
0,2
0,3
Injection (in V)
Thr=135
Thr=132
Thr=129
Thr=126
Thr=125
as 8bit DAC setting
55Fe decay signal

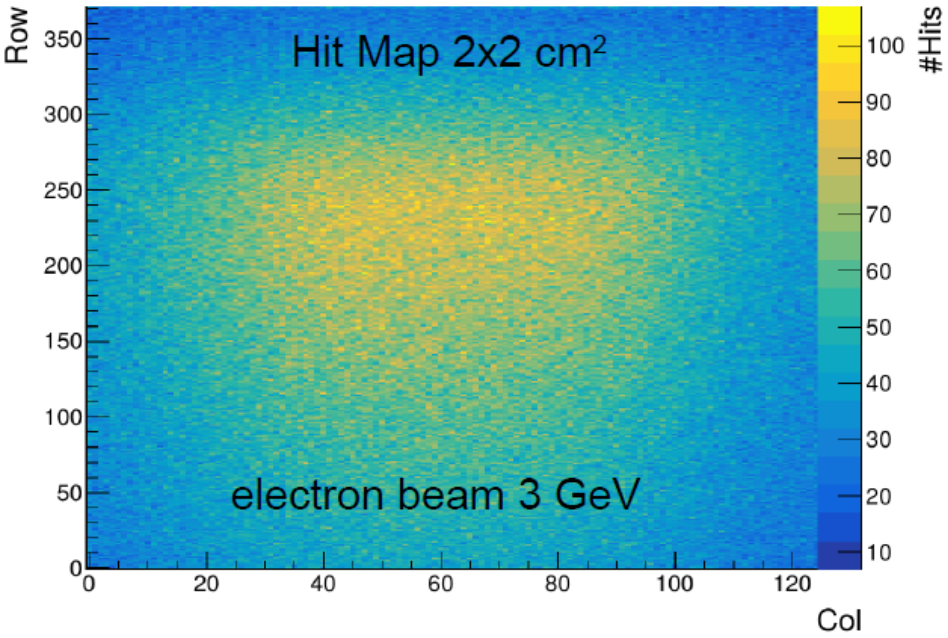

Layer 1
Counts
ToT (in µs)

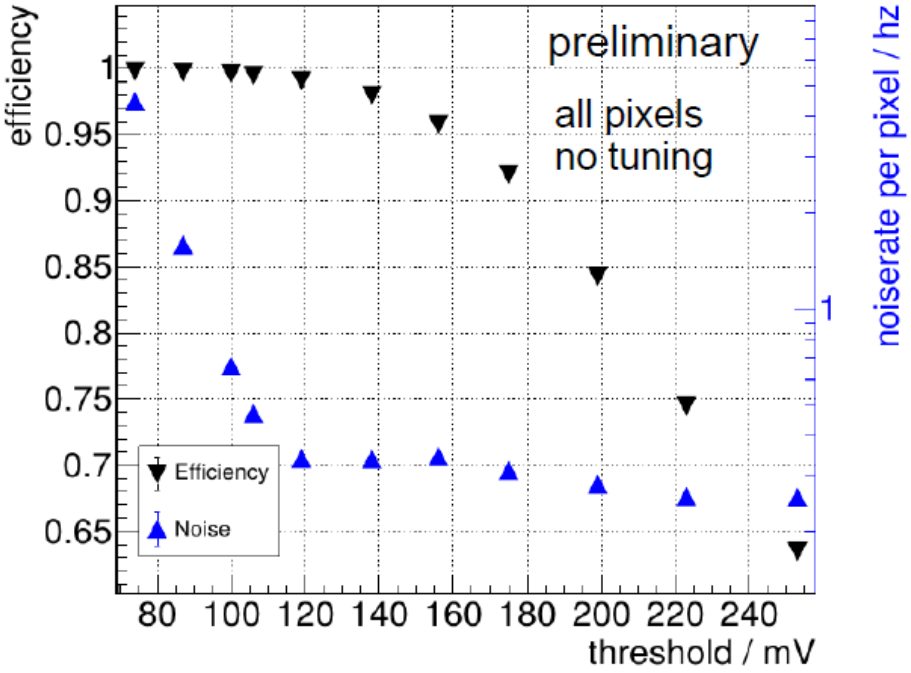

Layer 2
Counts
ToT (in µs)


Layer 3
Counts
ToT (in µs)


Layer 4
Counts
ToT (in µs)

- Excellent efficiency





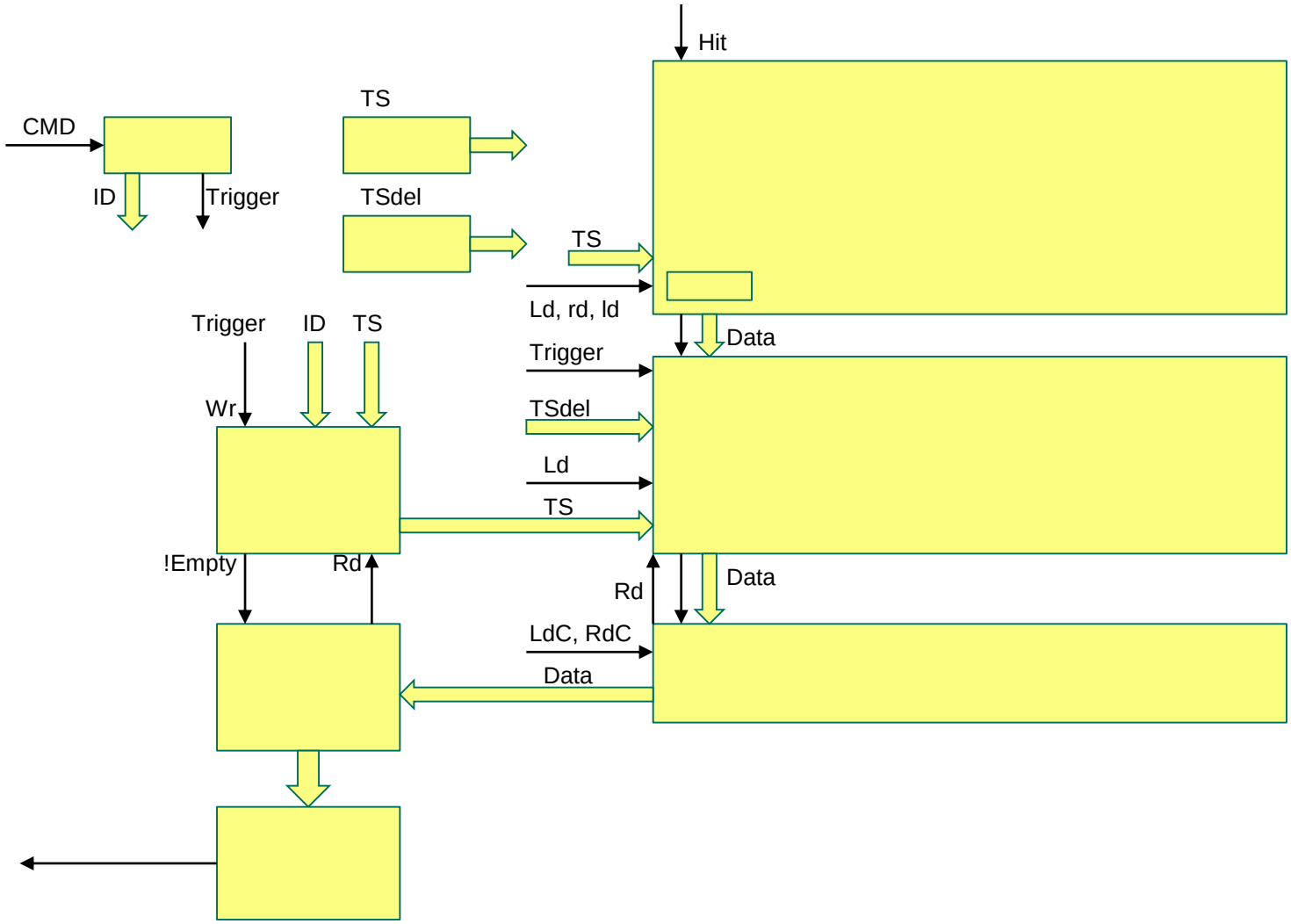
- ATLASPix3 is a full reticle, single matrix detector
- The detector is working and has a high yield
- Trimming is possible to compensate for threshold and timing differencies
- A four layer beam telescope was developed and is operational
- Excellent efficiency in test beam

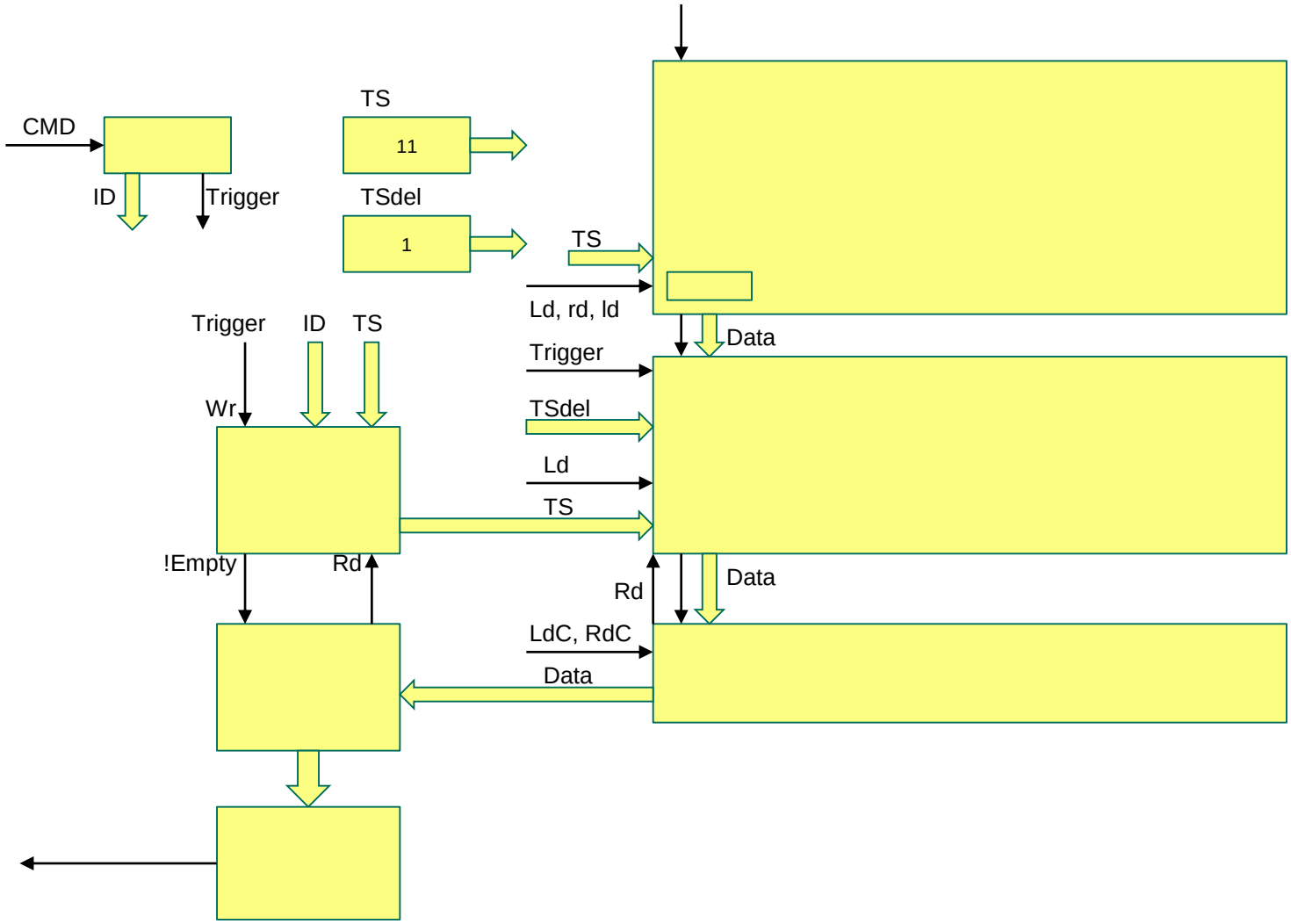
- MuPix10 is a full reticle, single matrix detector
- The chip design was submitted to TSI in December 2019, the wafers are ready to be shipped, tests will start in March 2020
- Advantage versus ATLASPIX3 – 3 data outputs, 3x higher data rate

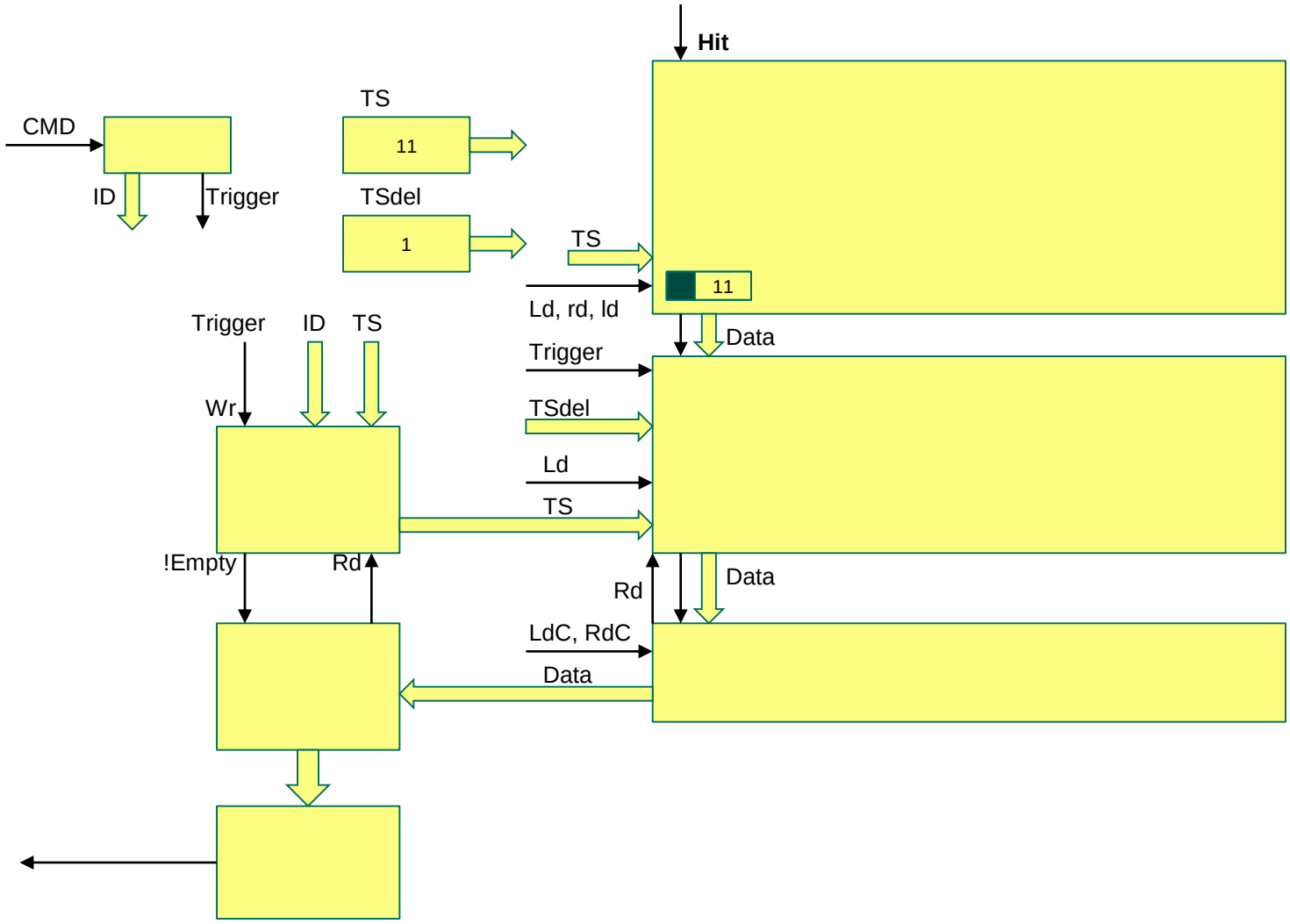
- The chip has a size of 20.66×23.18mm and contains 256 columns each with 250 pixels
- Each pixel has a size of 80 × 80 μm^2
- The pixel electronics contains of a charge sensitive PMOS amplifier, its feedback and the output driver
- The output driver of the pixel is connected to a long line to the readout buffer placed in the chip periphery
- The output of the pixels is a voltage signal, the output driver is realized with a source follower.
- The readout buffer contains different circuits for the following purposes: time measurement, amplitude measurement, address signal generation, temporary storage of the hit information (11 bit time stamp and 5 bit second time stamp for time over threshold calculation), priority ordered readout and hit bus signal generation.
- There are two different modes of the readout buffer
  - The two comparators are used with different threshold voltages. The output of the comparator with the smaller threshold is used for storing the timestamp. By this, the timewalk can be reduced. The hits are confirmed using the comparator with the higher threshold.
  - The other possibility is to turn one of the comparators off to allow a power saving modus and doing just a time over threshold (ToT) measurement.
- The threshold can be set for each comparators individually. The TDAC is extended so that every comparator has a 3-bit DAC and RAM cells
- Matrix is divided into 3 segments
- The RCU receives the signals of the corresponding matrix segment. The state machine generates the signals LdPix, Pull Down, LdCol and RdCol. RCU receives the hit data containing the two timestamps, the row address and the column address. The output of the RCU are 3+1 parallel data words
- Current mode DACs are 6-bit DACs made with current sources. These DACs produce currents. To bias a current source in a pixel, there is a diode connected transistor near the DAC. The DAC current generates voltage when it flows through the diode connected device. The voltage is distributed in the pixels and connected to the gates of the current sources.
- Voltage mode DAC uses a resistor ladder structure
- There are six independent shift registers. Bias, Config and VDAC are responsible for the global chip configuration. Col, TDAC and Test are responsible for the configuration of the chips test infrastructure (injection, ampout, hitbus), as well as the pixel tuning.

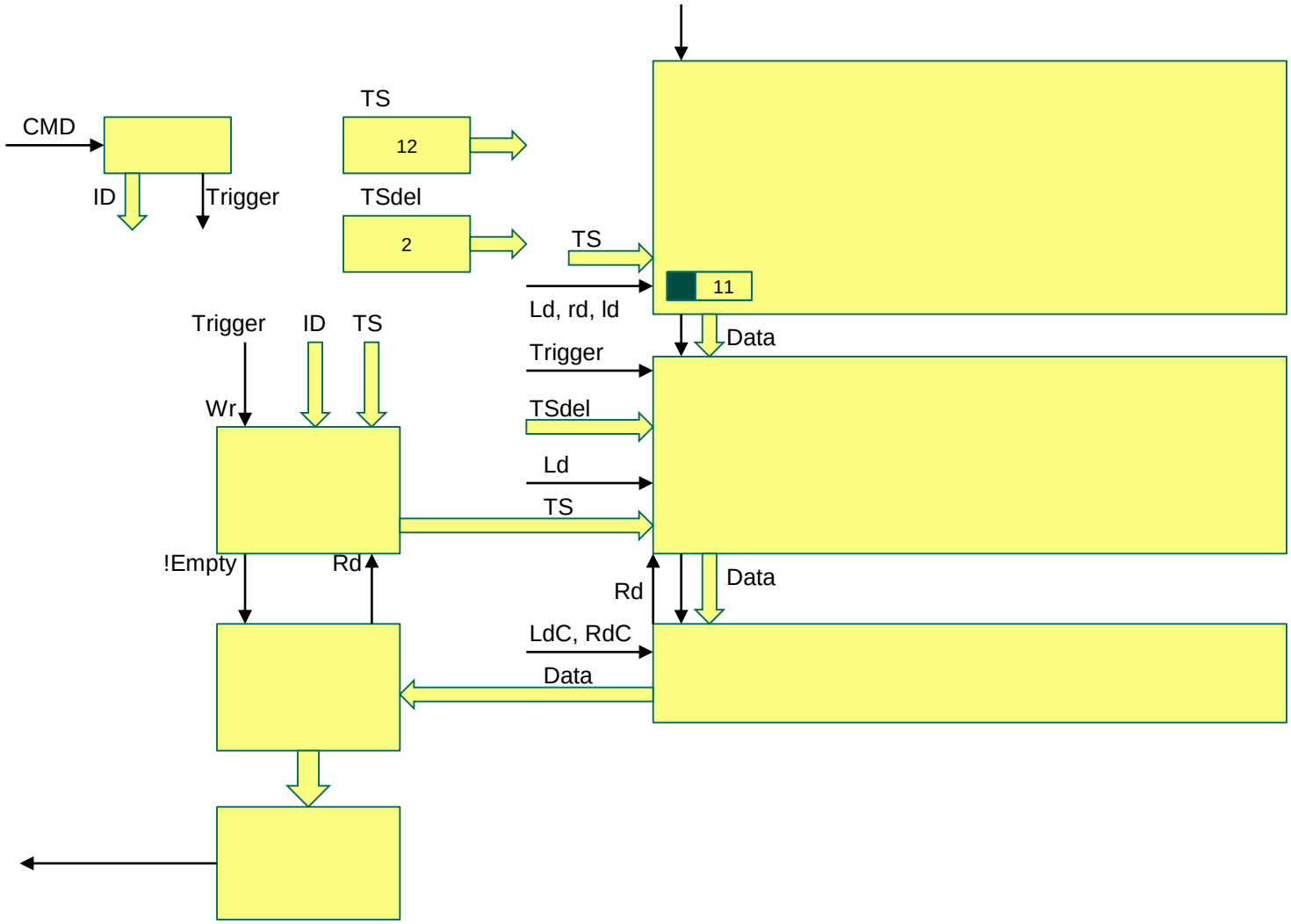
- Thank you

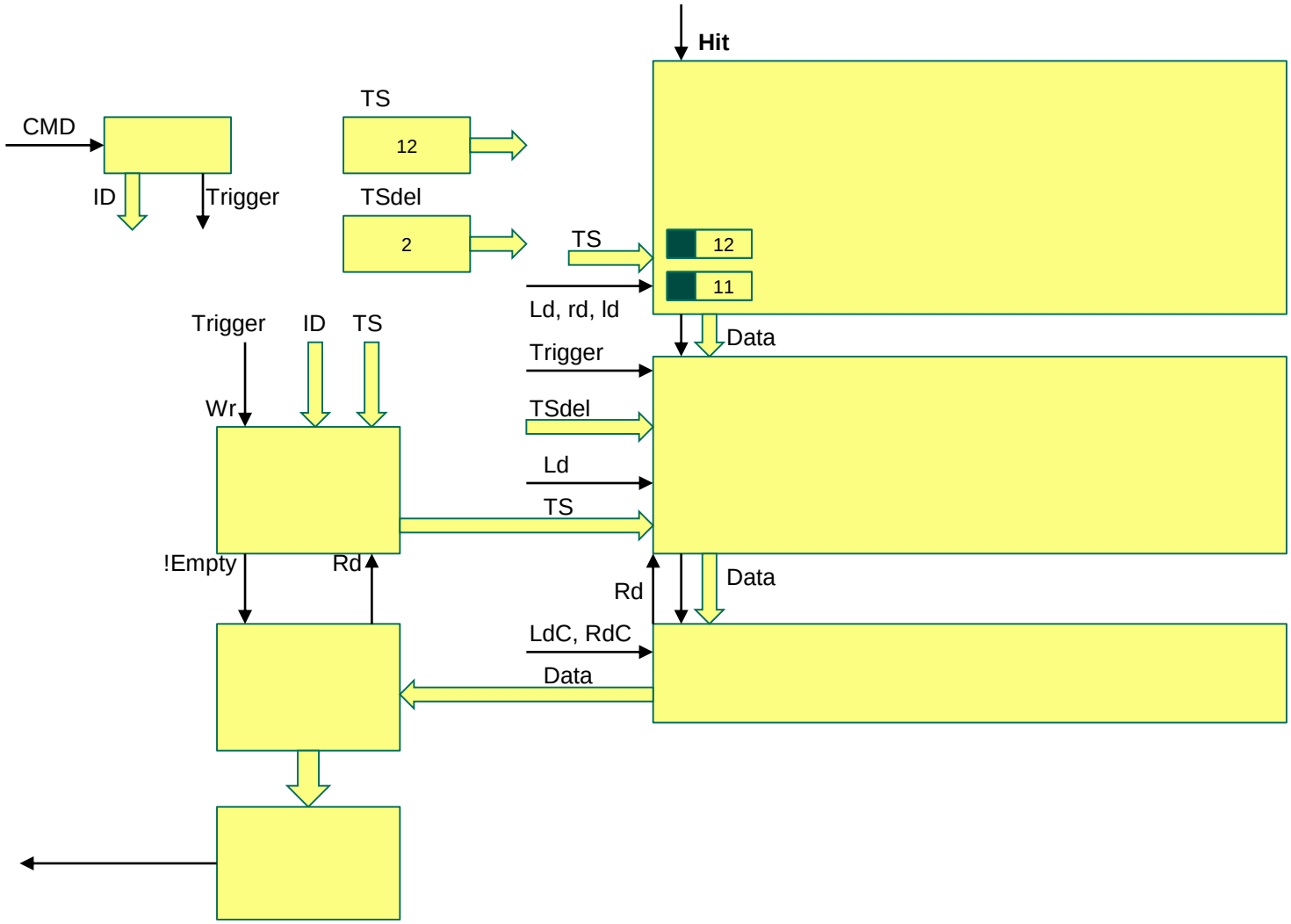
- Triggered readout animation

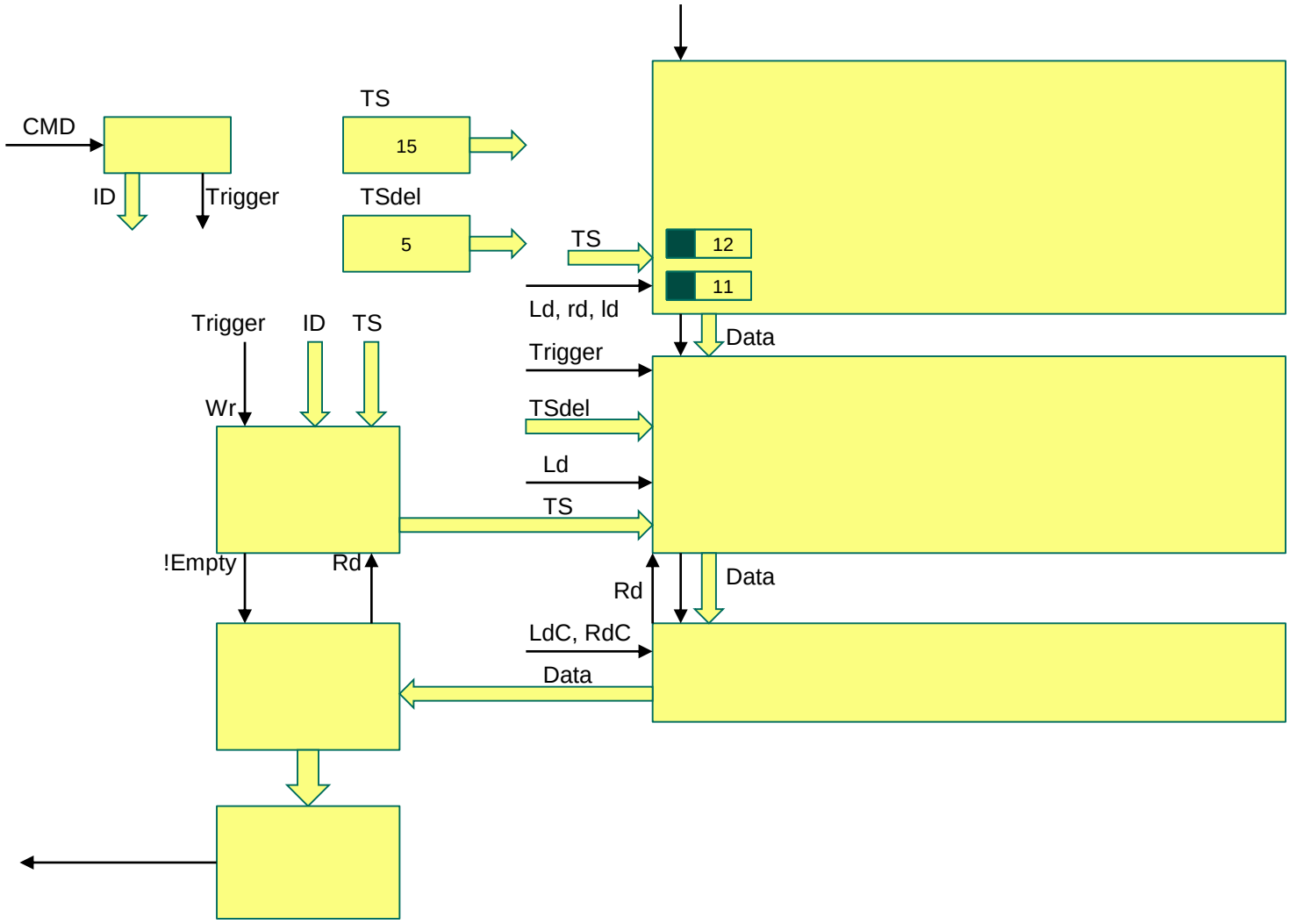

Hit
TS
CMD
ID
Trigger
TSdel
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

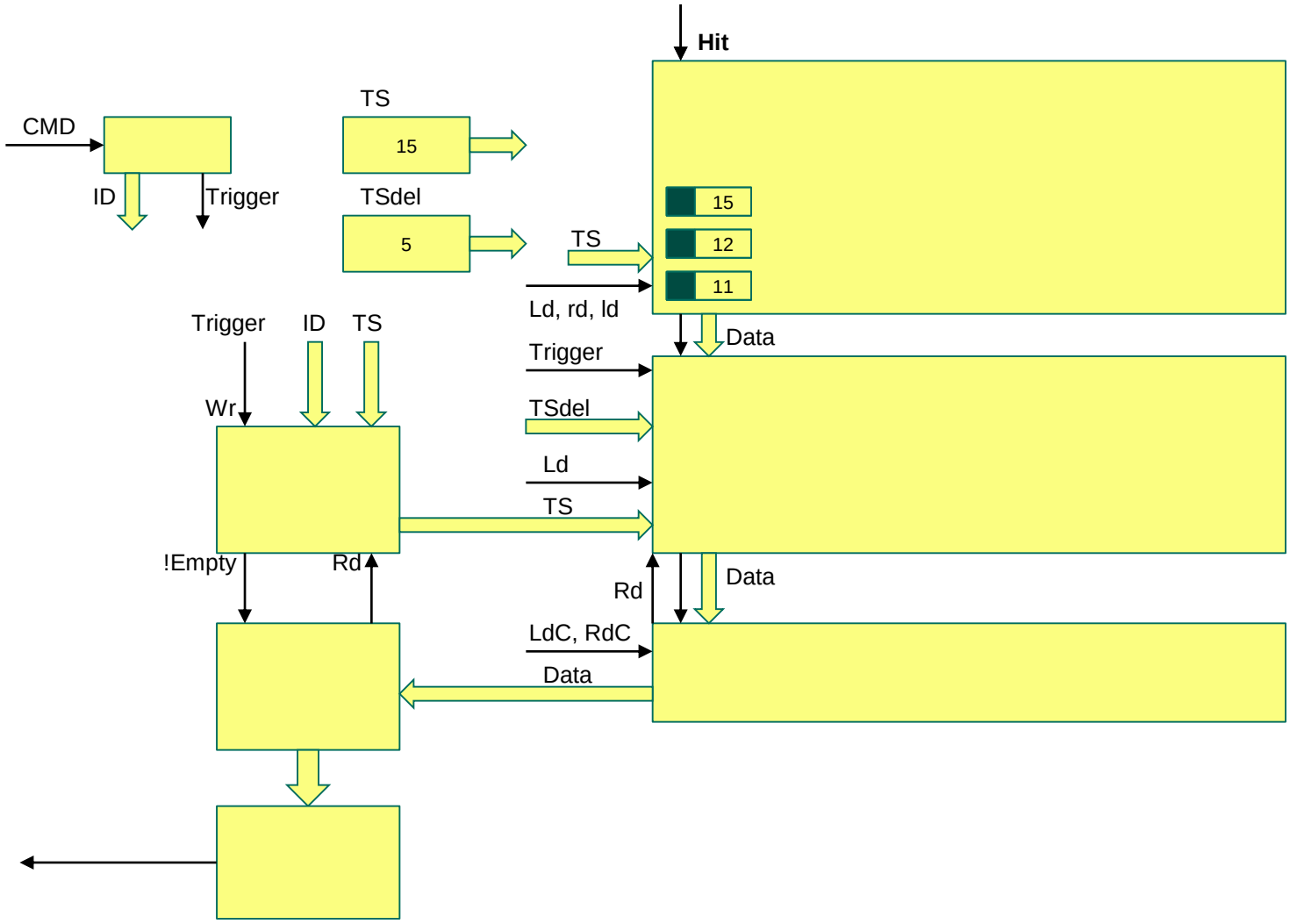

CMD
ID
Trigger
TS
11
TSdel
1
TS
Ld, rd, ld
Data
Trigger
TSdel
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd

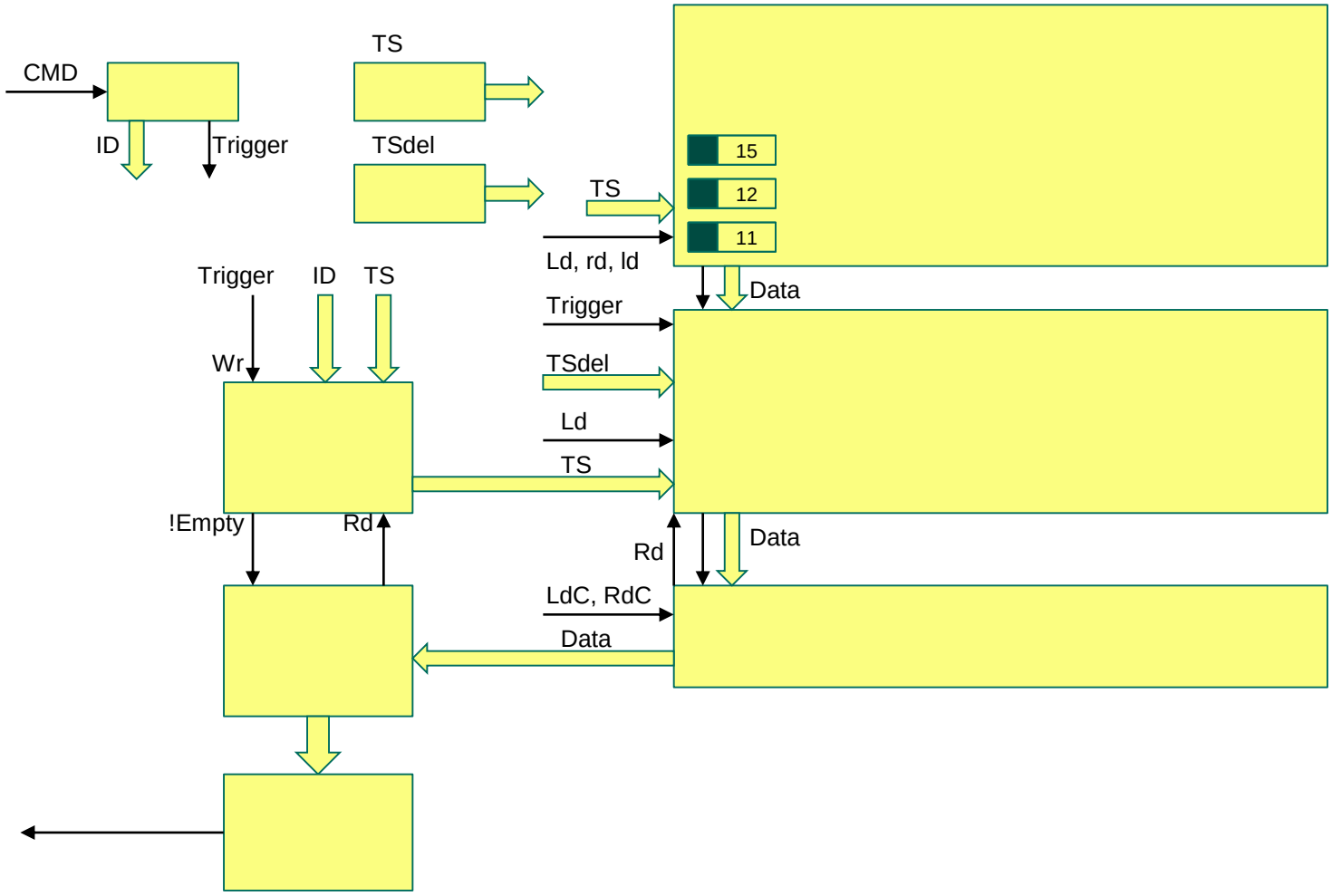

Hit
TS
CMD
11
ID
Trigger
TSdel
1
TS
11
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

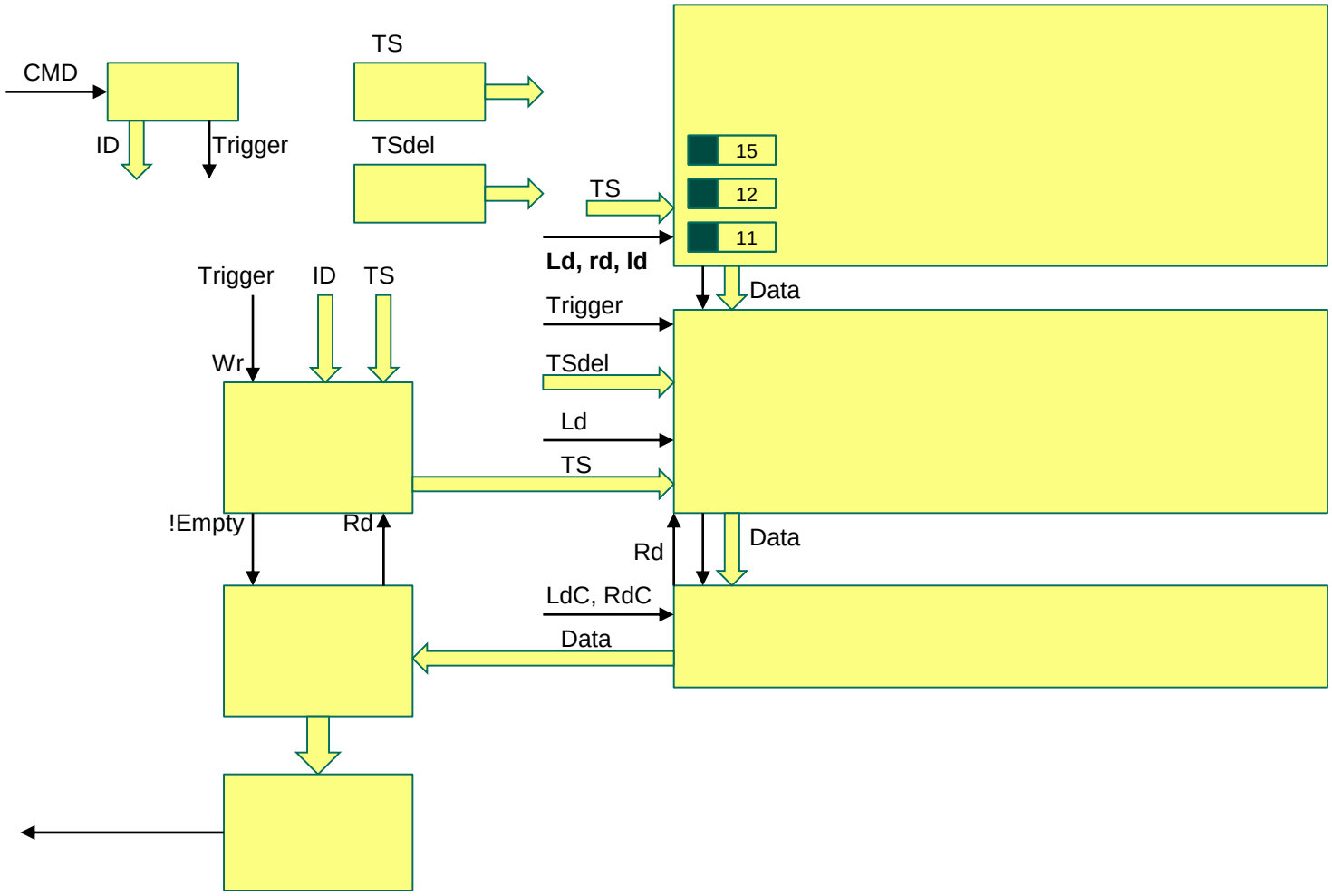

CMD
ID
Trigger
TS
12
TSdel
2
TS
11
Ld, rd, ld
Data
Trigger
TSdel
Ld
TS
Data
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd
Rd

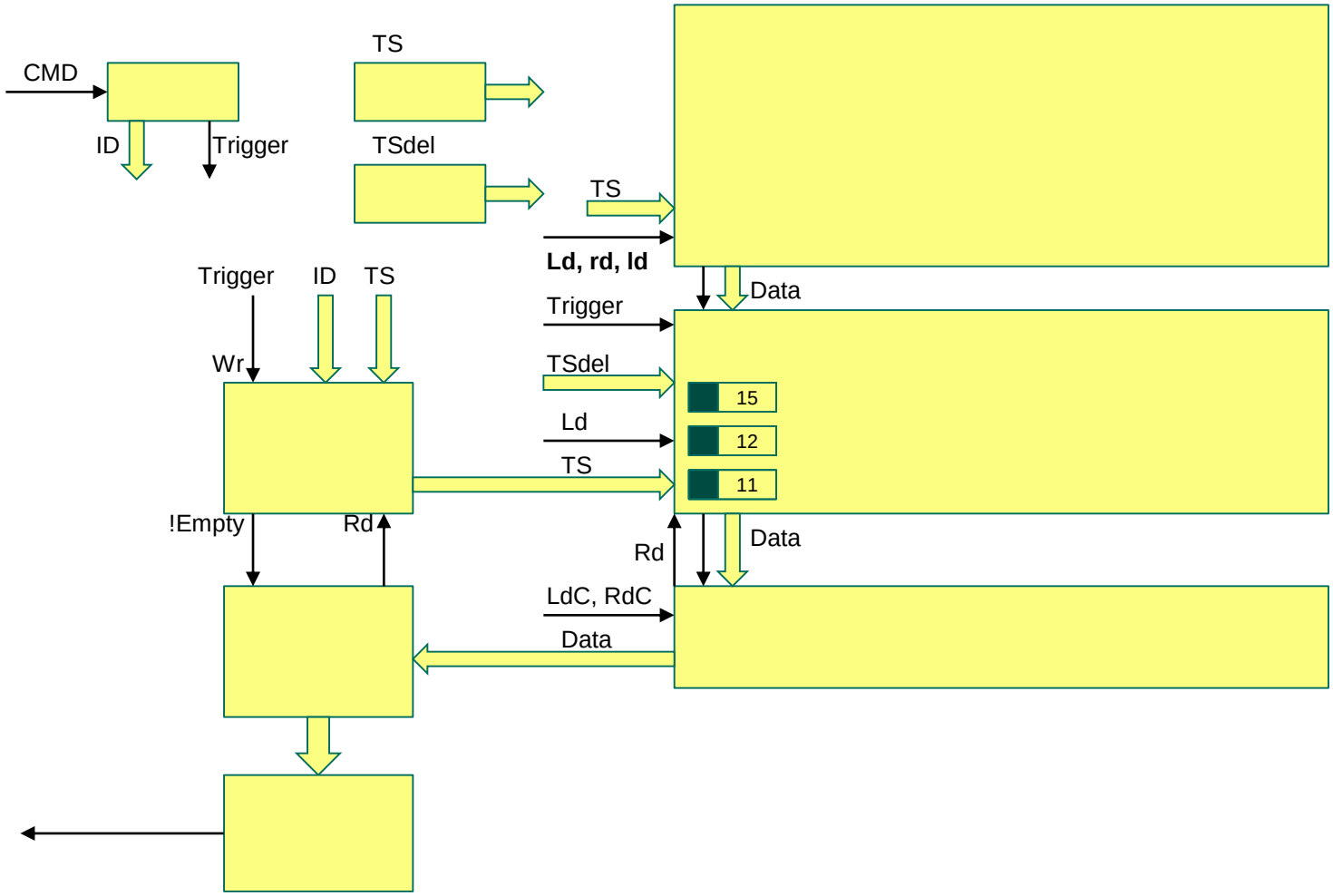

Hit
TS
CMD
12
ID
Trigger
TSdel
2
TS
12
11
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

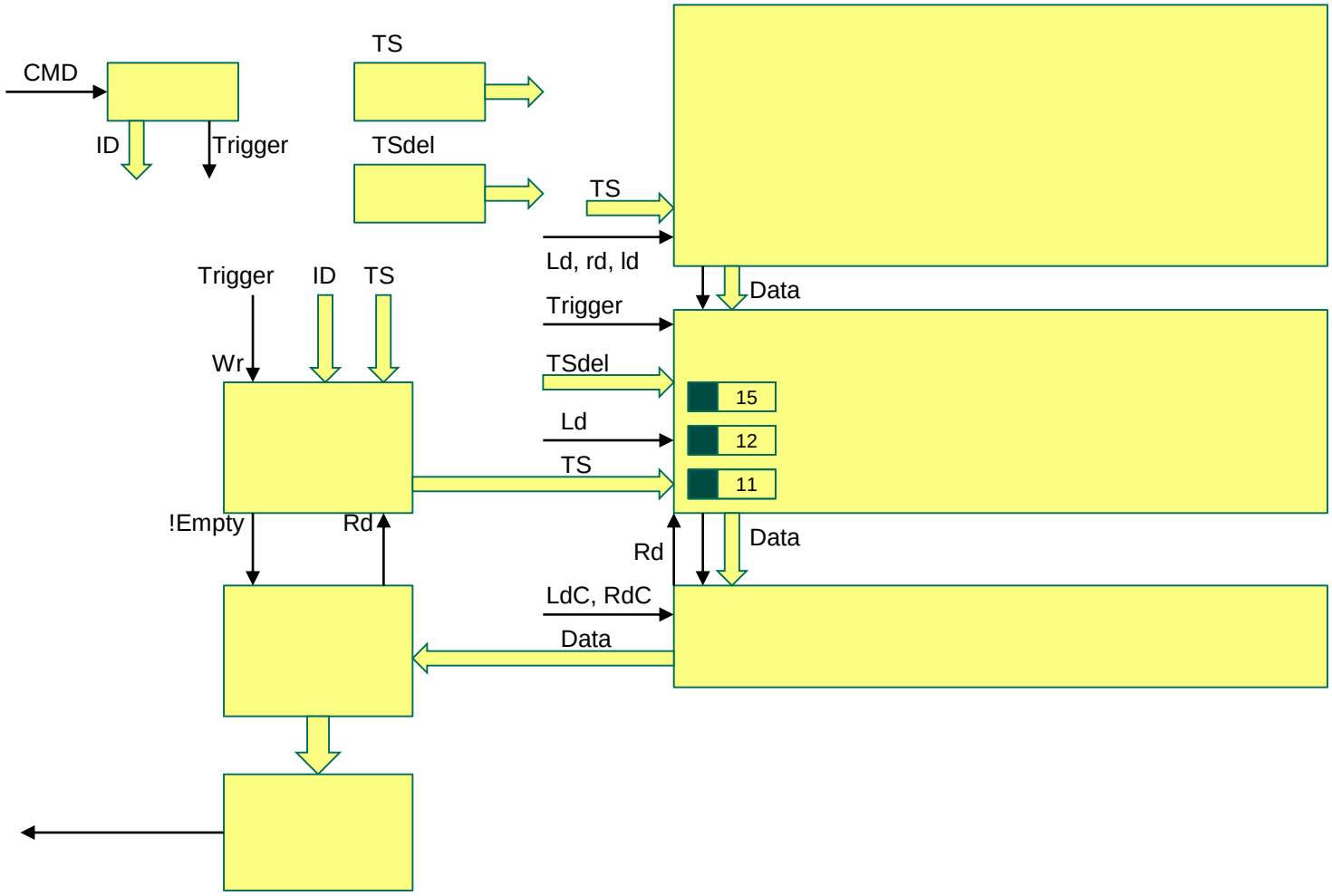

CMD
ID
Trigger
TS
15
TSdel
5
TS
12
11
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

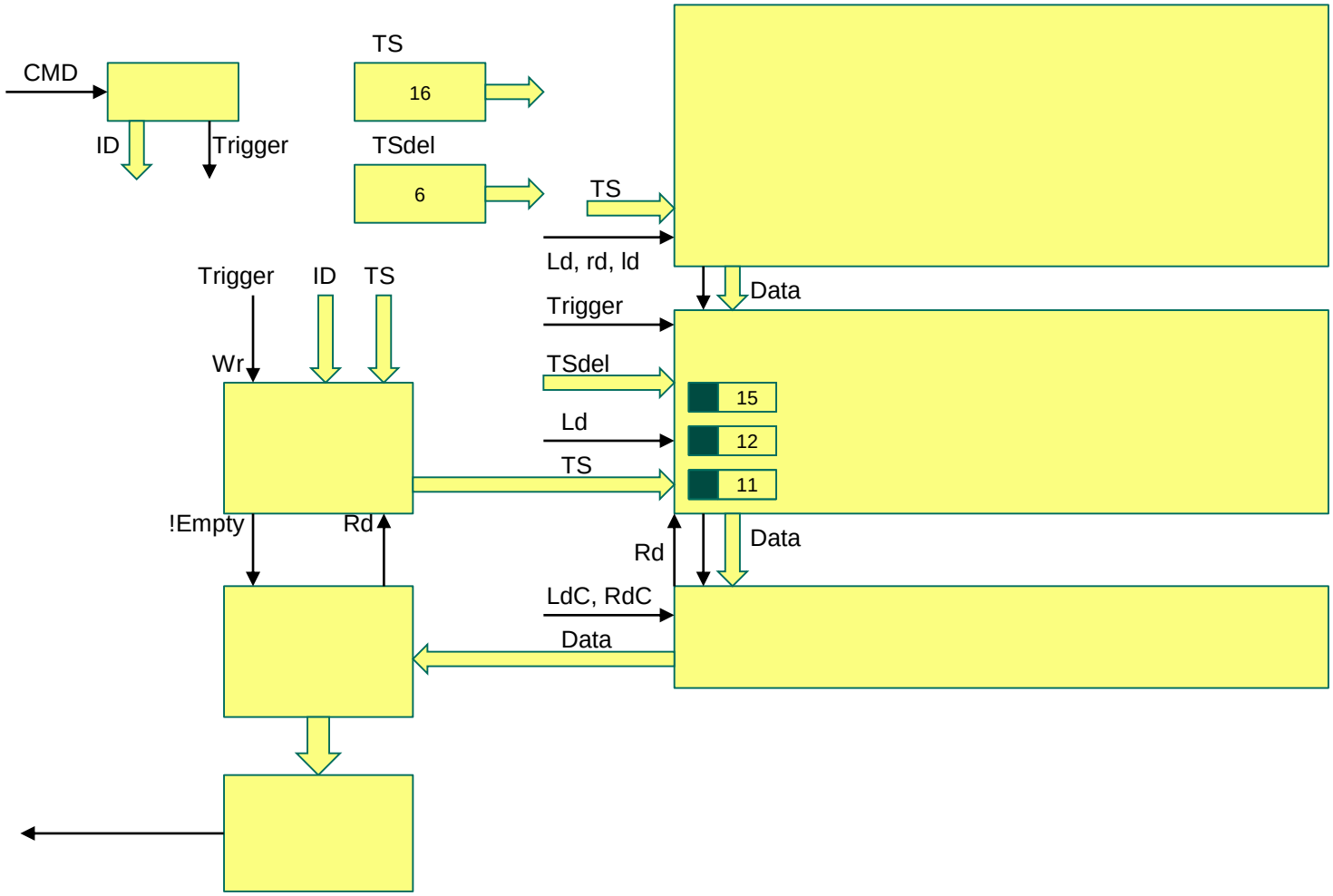

Hit
CMD
ID
Trigger
TS
15
TSdel
5
15
12
11
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

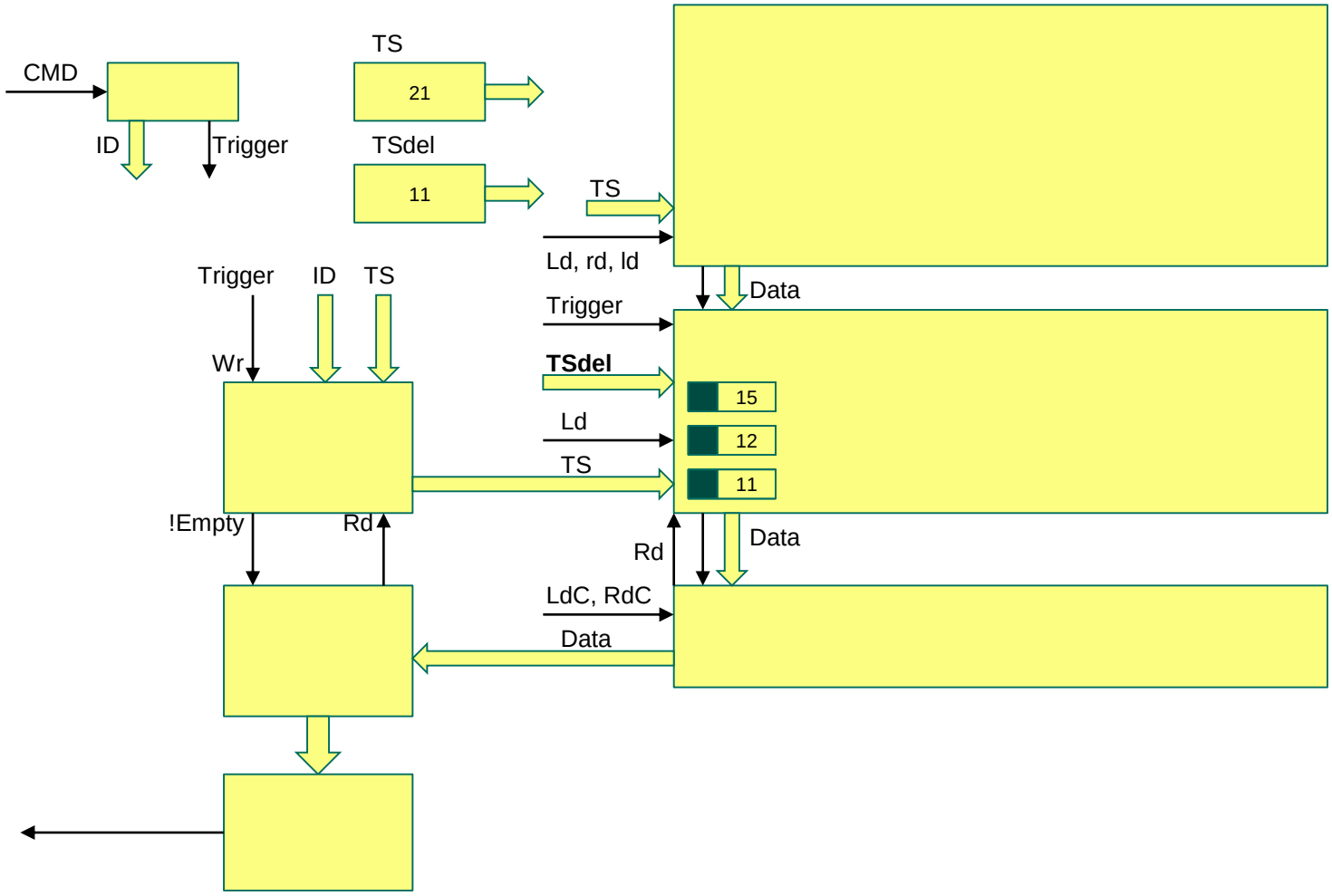

CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
15
12
11
Data
Trigger
TSdel
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd

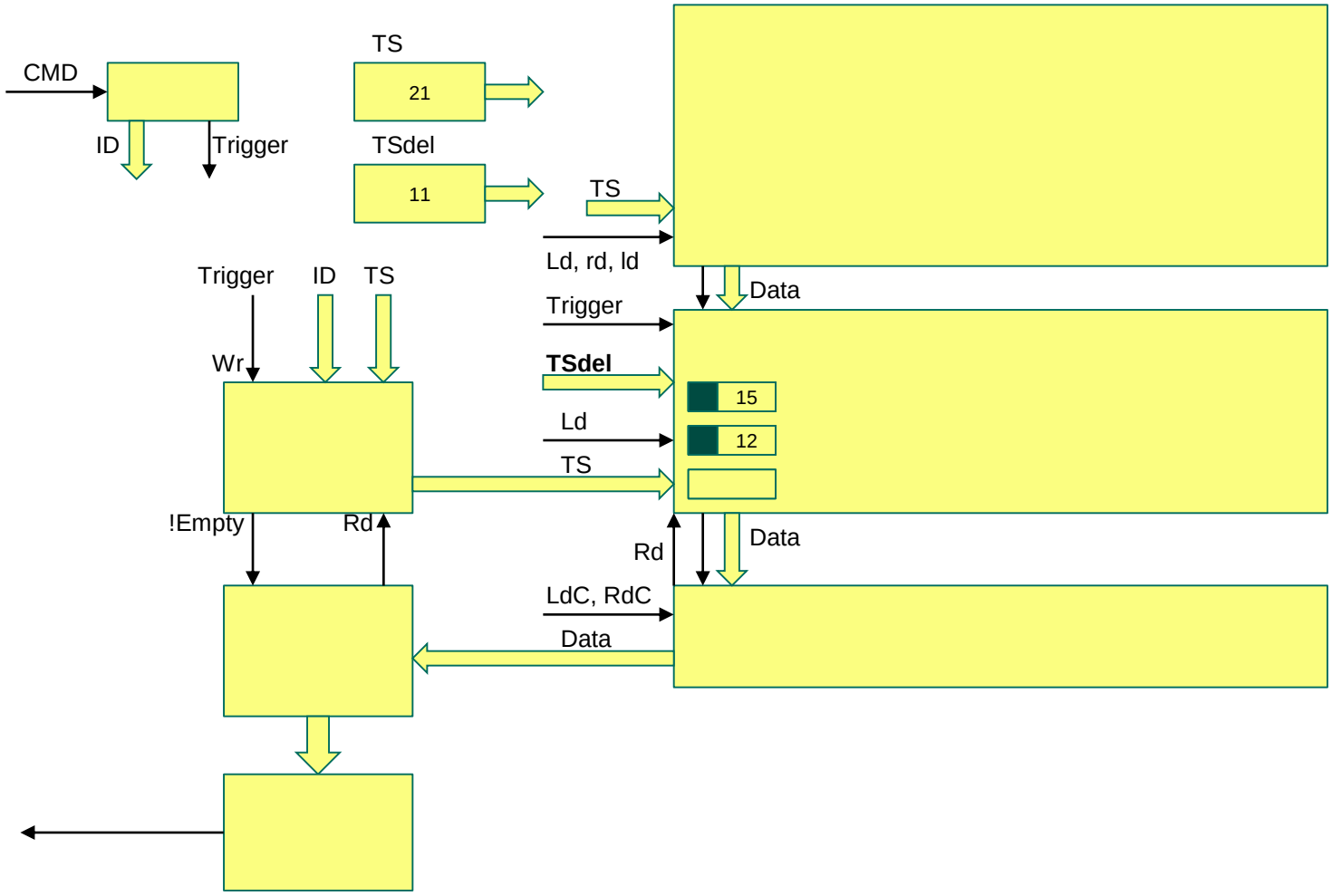

CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
15
12
11
Data
Trigger
TSdel
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd

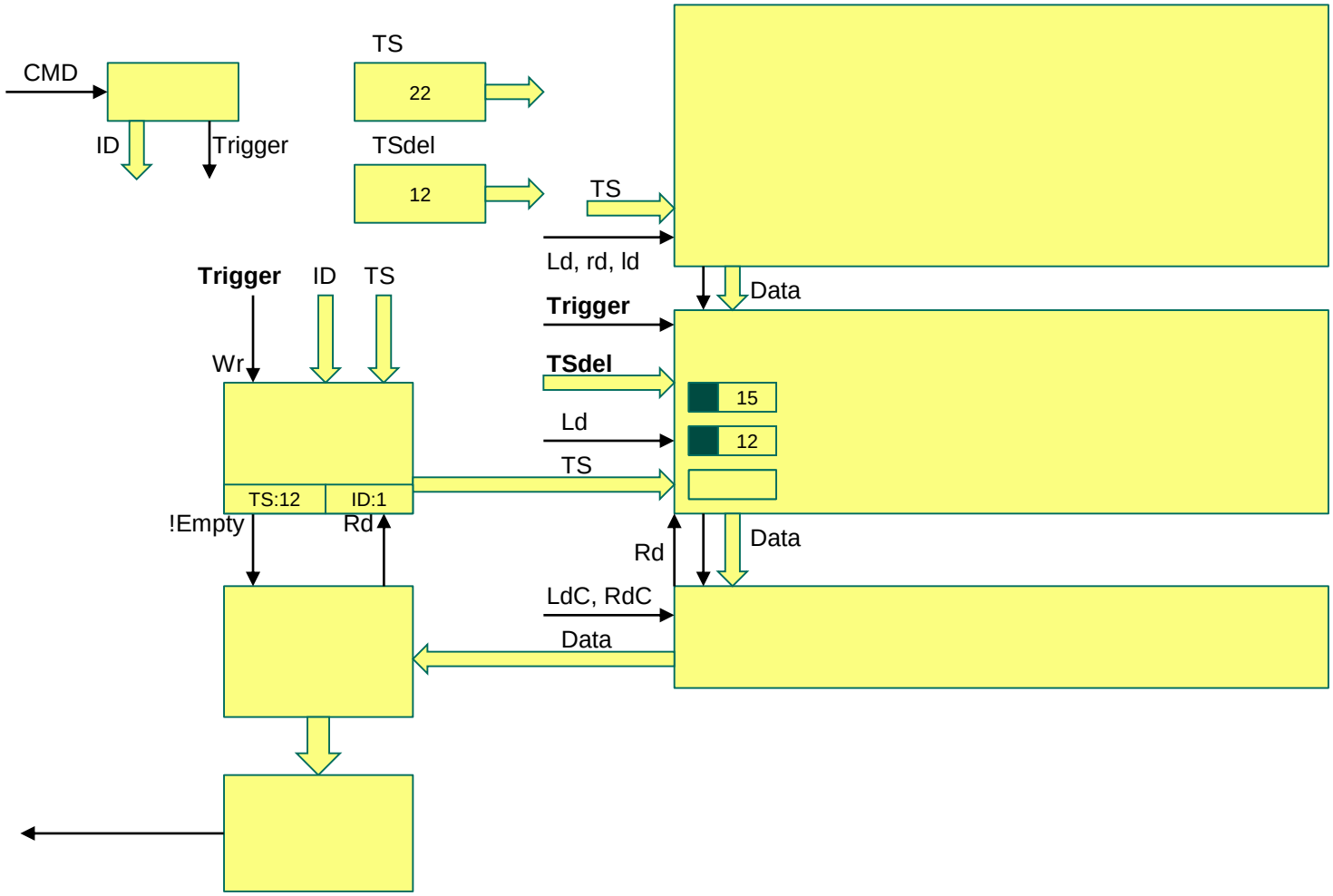

CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
Ld
TS
15
12
11
!Empty
Rd
Rd
Data
LdC, RdC
Data

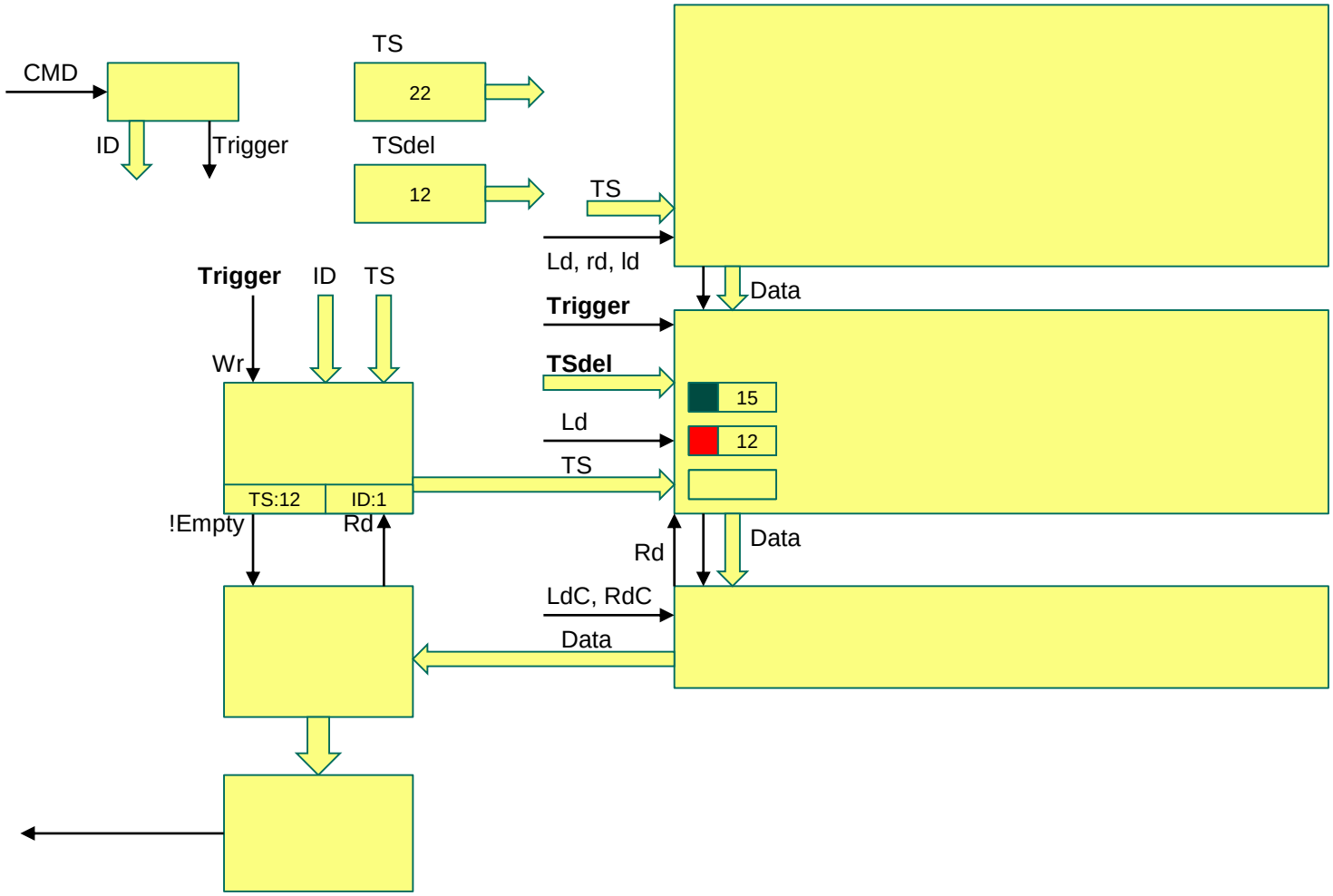

CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
11
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd


CMD
ID
Trigger
TS
16
TSdel
6
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
11
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd


CMD
ID
Trigger
TS
21
TSdel
11
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
15
Ld
12
TS
11
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
21
TSdel
11
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
Ld
TS
Data
Rd
LdC, RdC
Data
Trigger
ID
TS
Wr
!Empty
Rd


CMD
ID
Trigger
TS
22
TSdel
12
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
Ld
TS
Trigger
ID
TS
Wr
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
22
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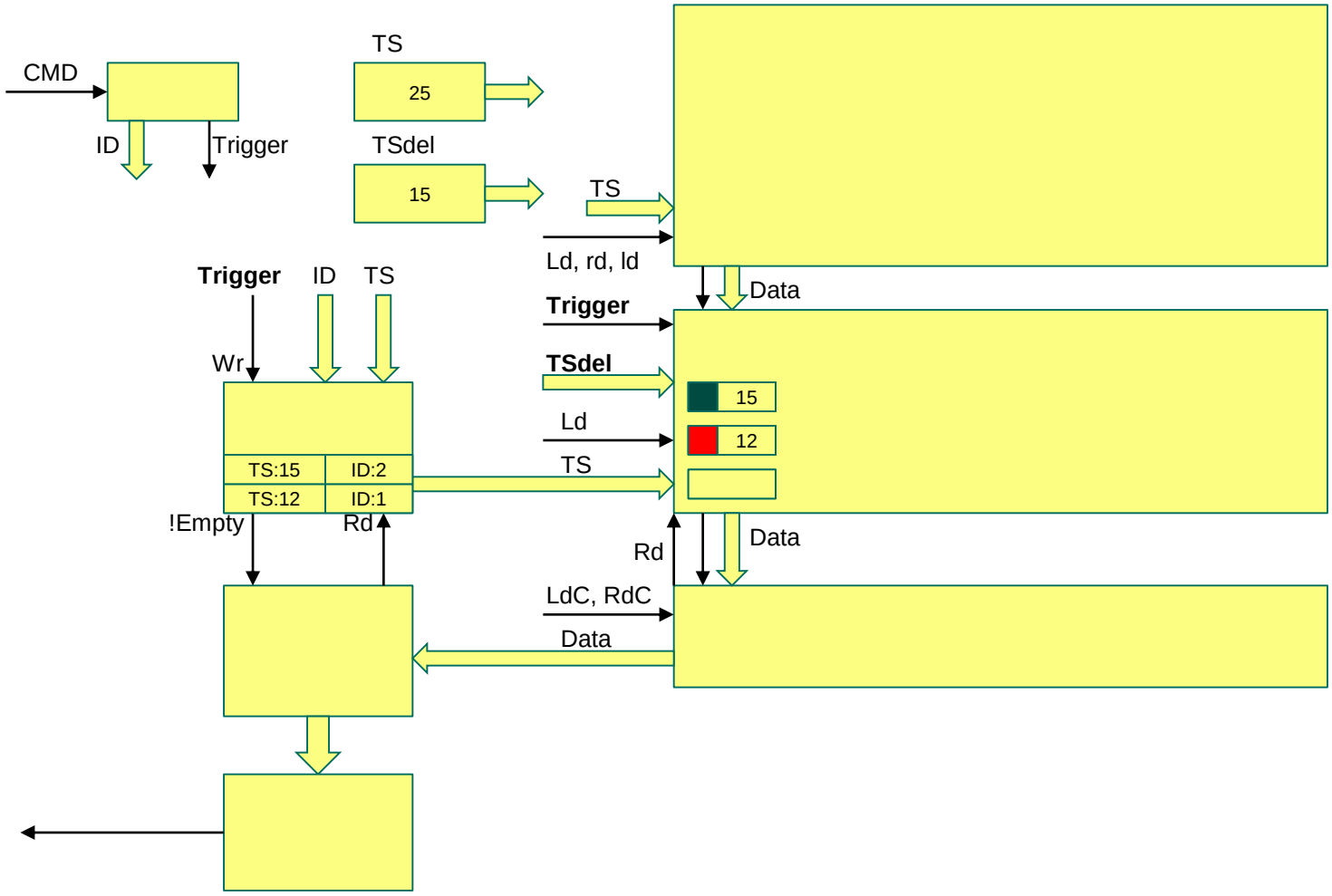
12
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
15
Ld
12
TS
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data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Trigger
TS
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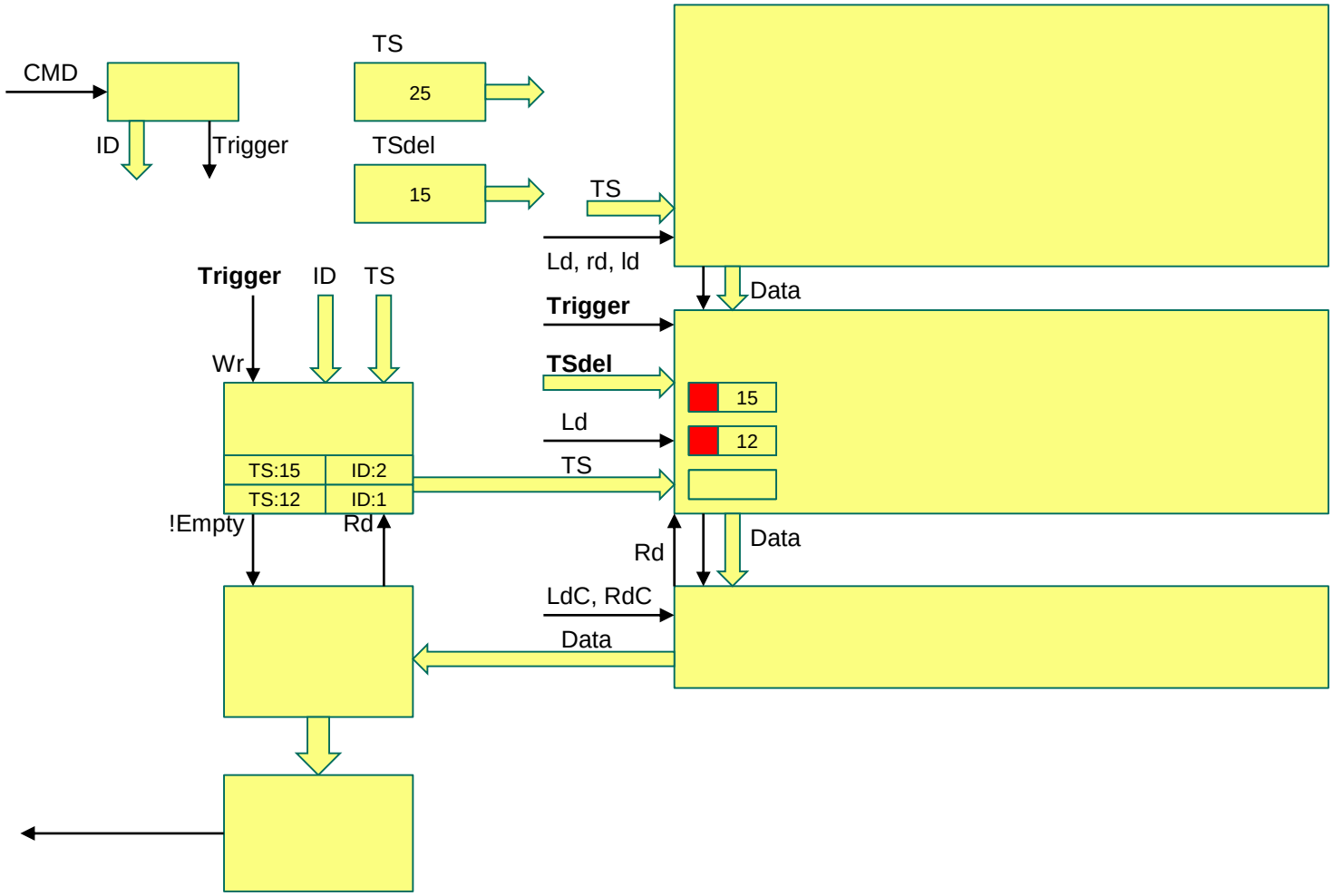
TSdel
15
TS
Ld, rd, ld
Data
Trigger
TSdel
Ld
TS
Rd
Data
LdC, RdC
Data
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
15
12


CMD
ID
Trigger
TS
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TSdel
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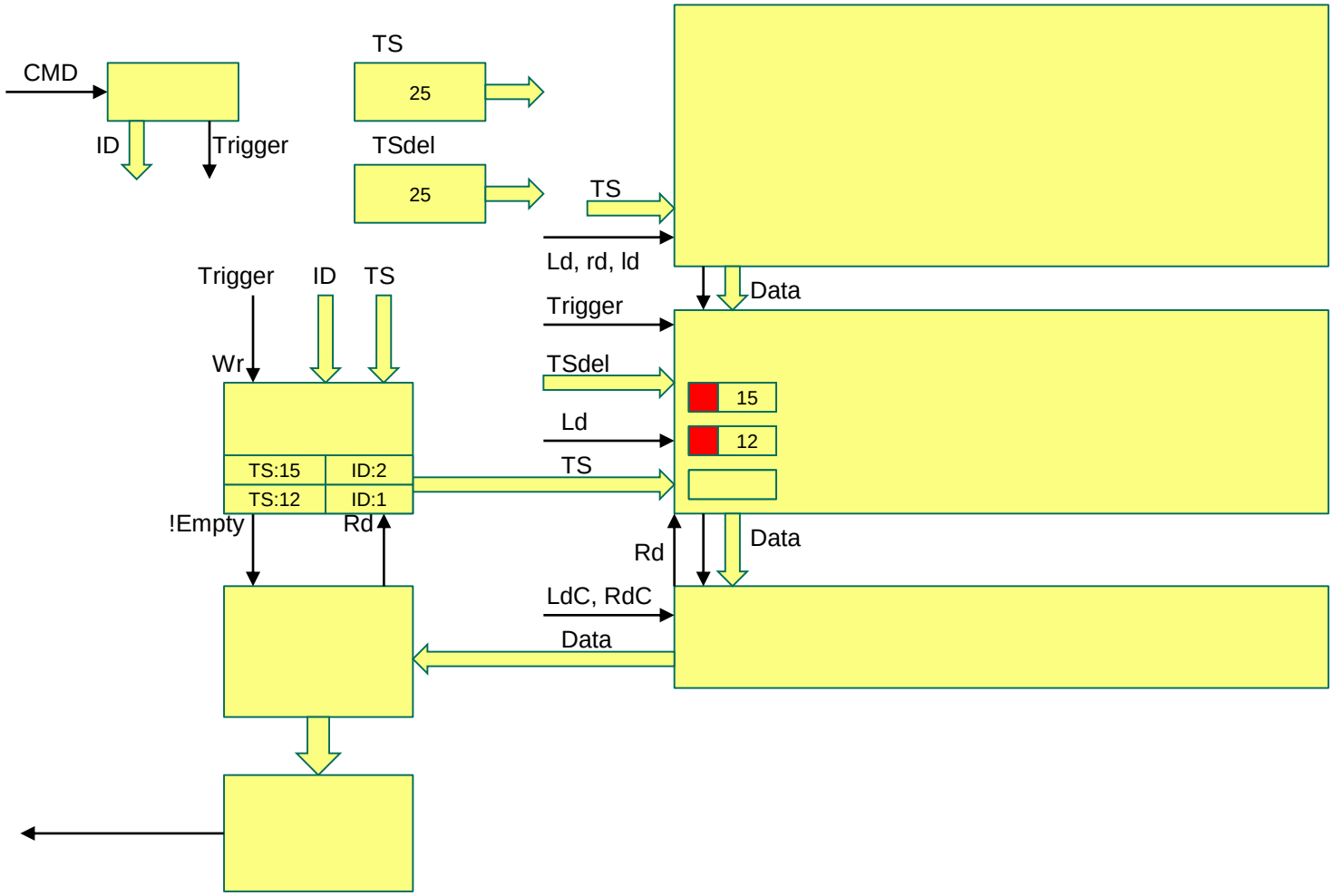
TS
Ld, rd, ld
Data
Trigger
TSdel
Ld
TS
15
12
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data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Ld, rd, ld
Data
Trigger
TSdel
15
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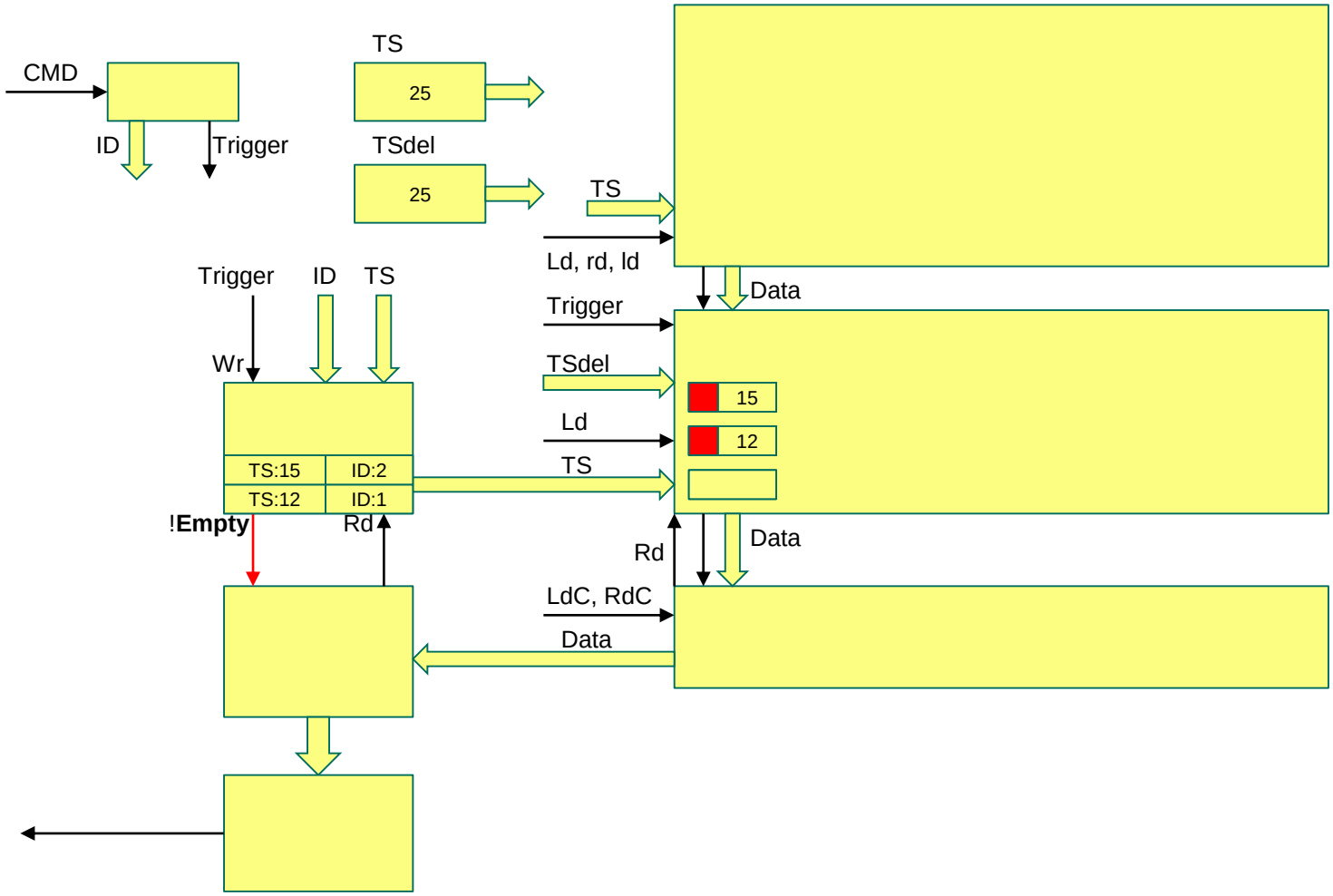
Ld
TS
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data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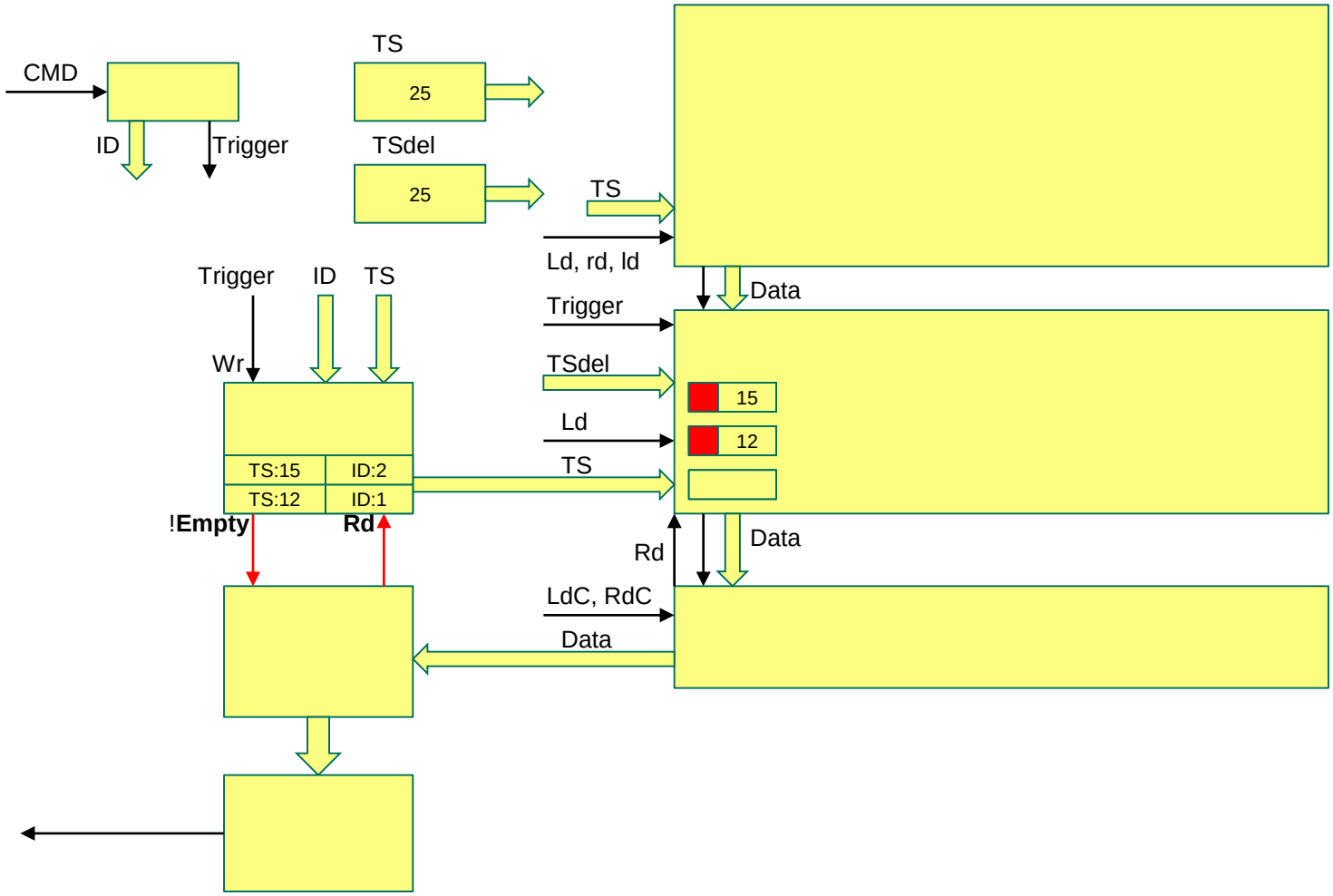
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
Ld
TS
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
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Ld, rd, ld
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Trigger
TSdel
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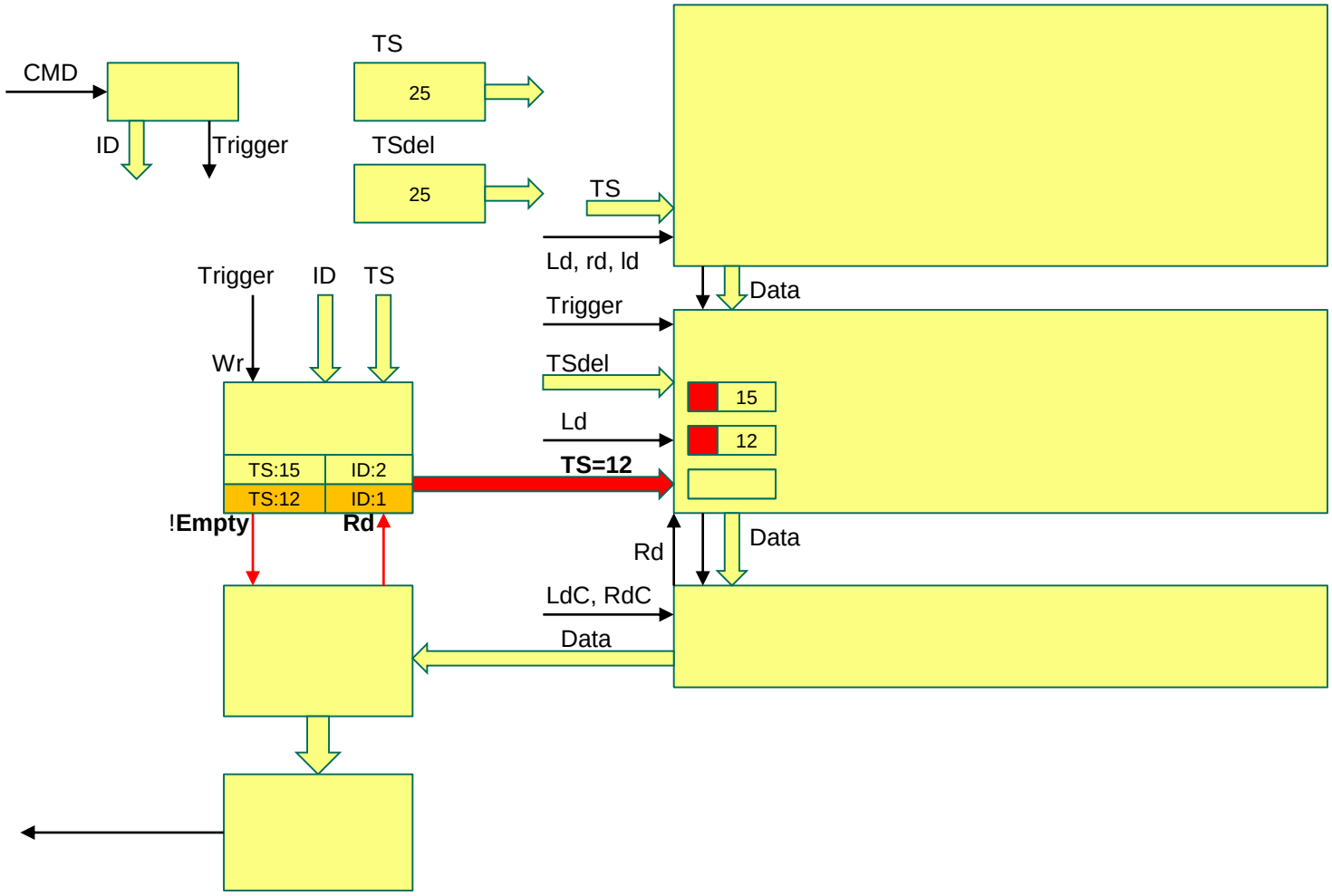
Data
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd


CMD
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TSdel
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TS
Ld, rd, ld
Data
Trigger
TSdel
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Ld
TS=12
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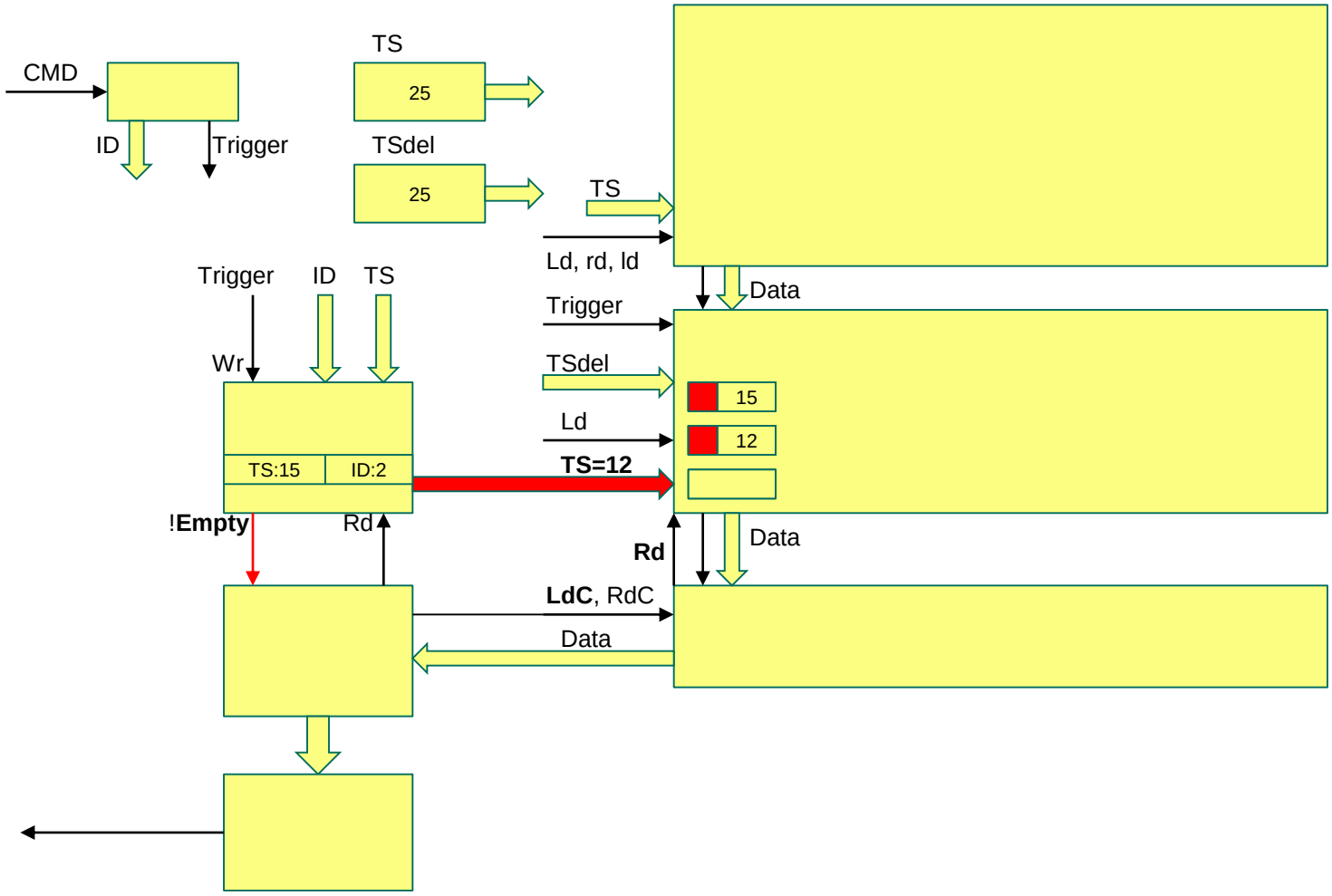
Data
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd


CMD
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TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
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Trigger
TSdel
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TS=12
TS:15
ID:2
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!Empty
Rd
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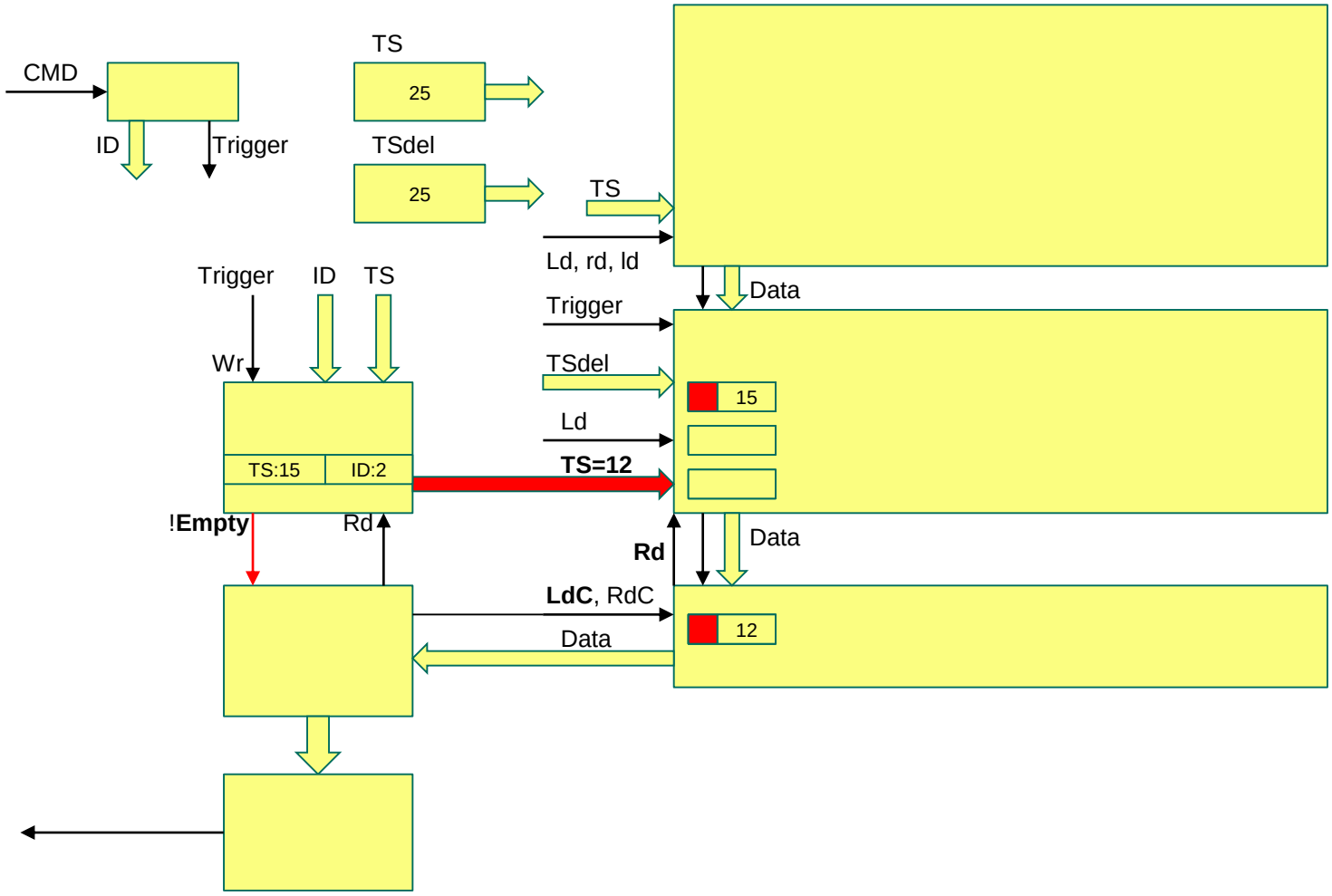
LdC, RdC
Data


CMD
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25
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Ld, rd, ld
Data
Trigger
ID
TS
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TS:15
ID:2
TS=12
!Empty
Rd
Rd
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LdC, RdC
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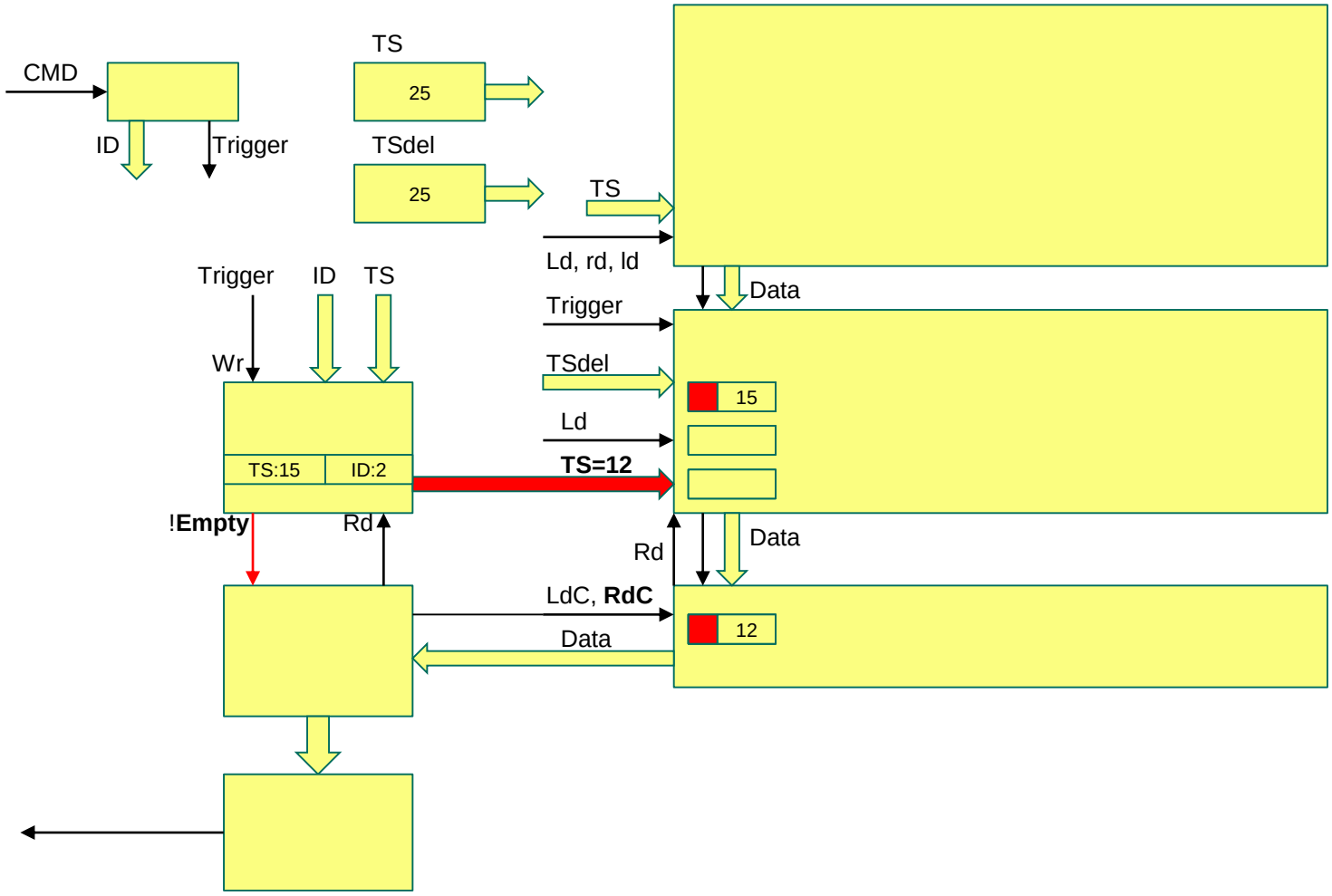
Data


CMD
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Trigger
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TSdel
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Ld, rd, ld
Data
Trigger
ID
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TS:15
ID:2
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!Empty
Rd
Rd
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Data
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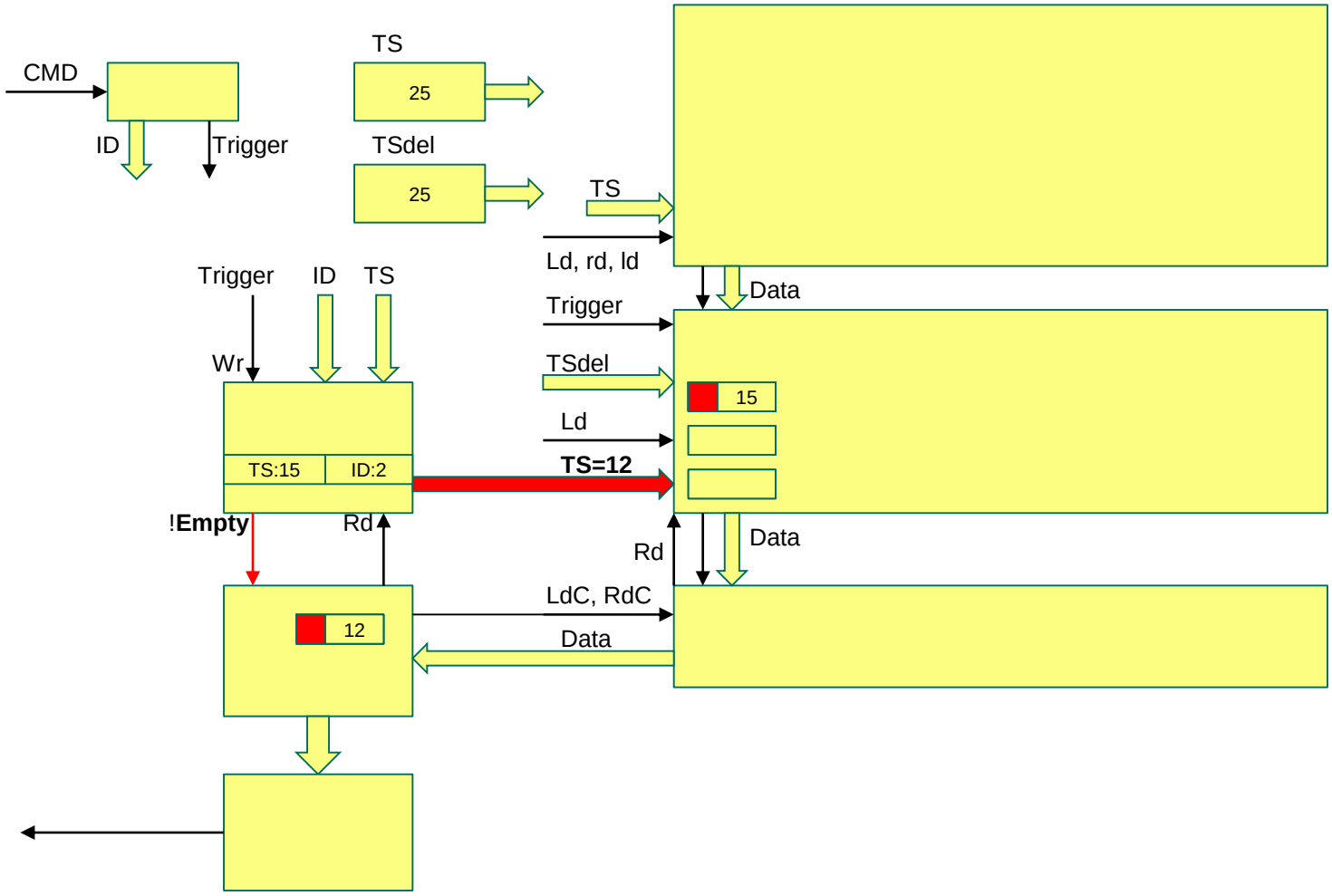
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TSdel
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TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
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TSdel
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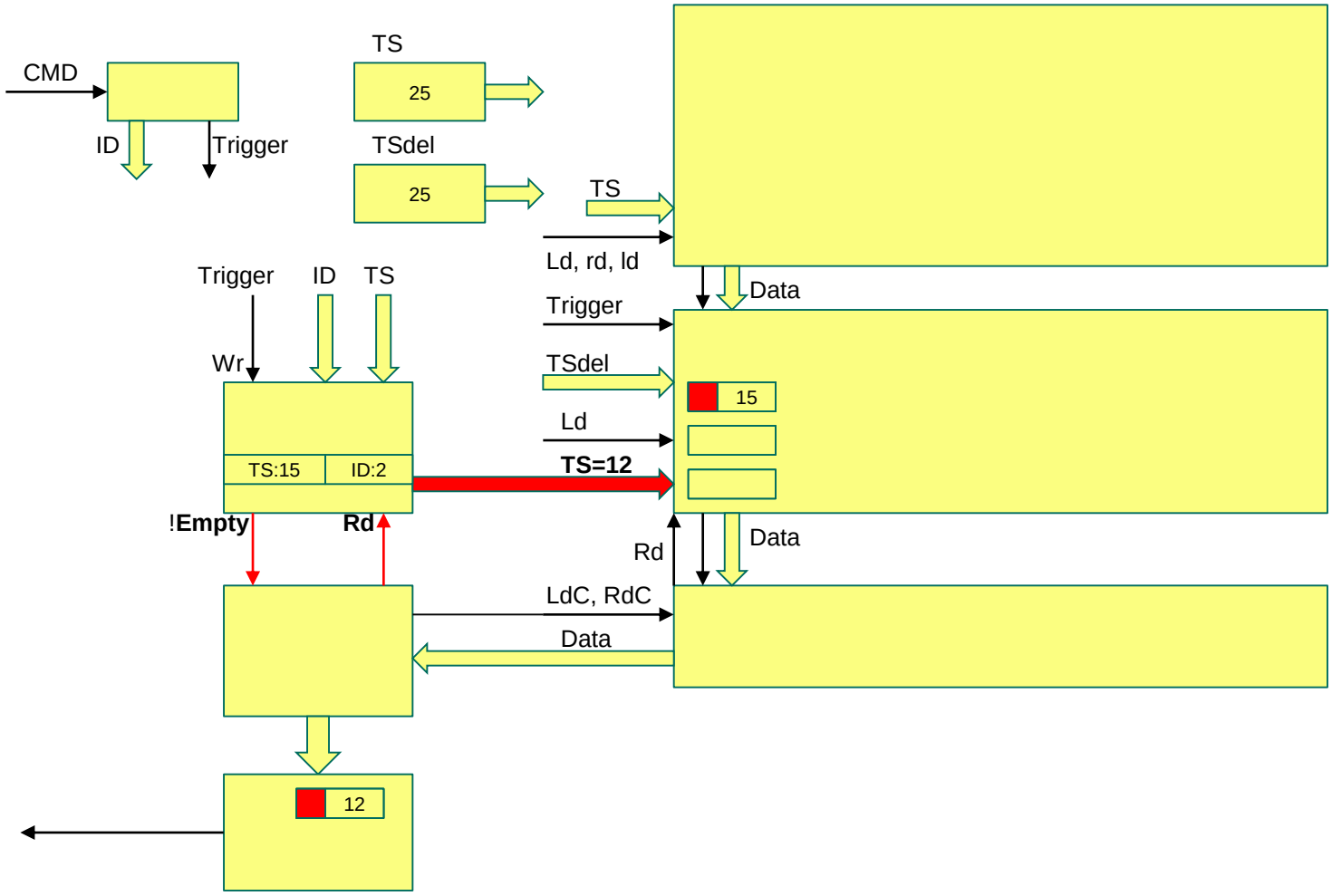
TS:15
ID:2
15
!Empty
Rd
Rd
Data
LdC, RdC
Data
12


CMD
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Ld, rd, ld
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Trigger
TSdel
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TS:15
ID:2
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Data
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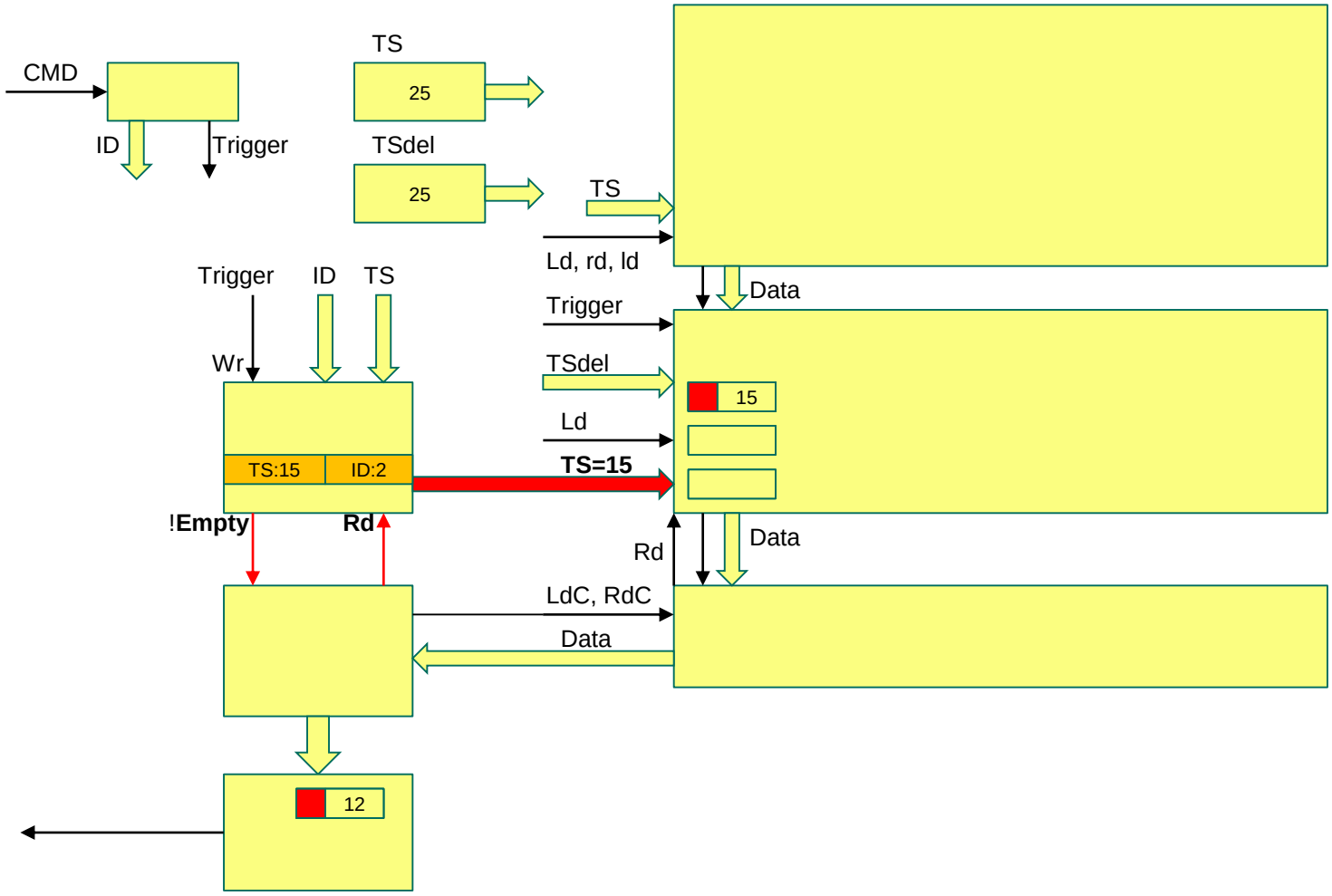
CMD
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TS
Ld, rd, ld
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Trigger
TSdel
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LdC, RdC
Data
Trigger
ID
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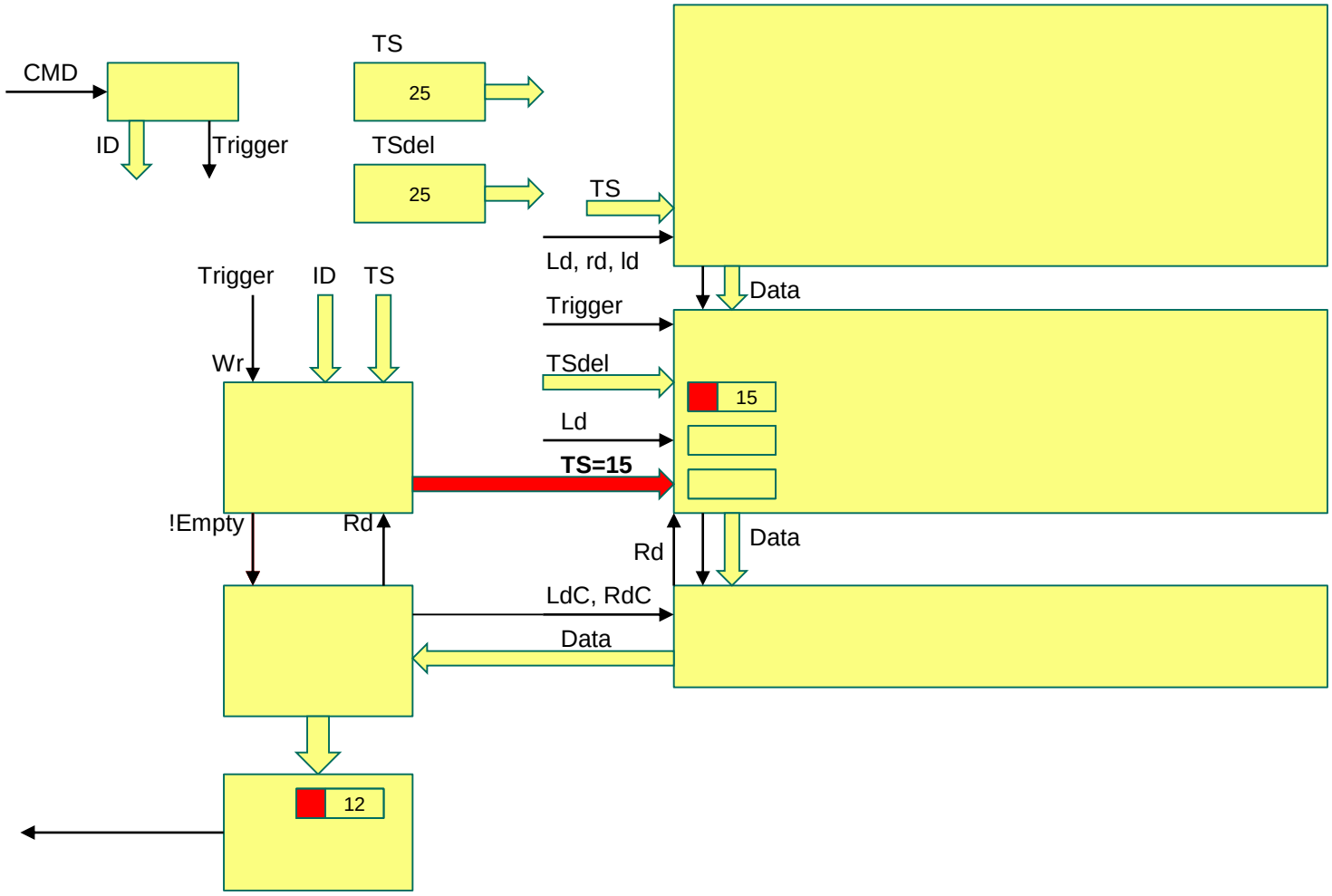
Wr
TS:15
ID:2
!Empty
Rd
12


CMD
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!Empty
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Rd
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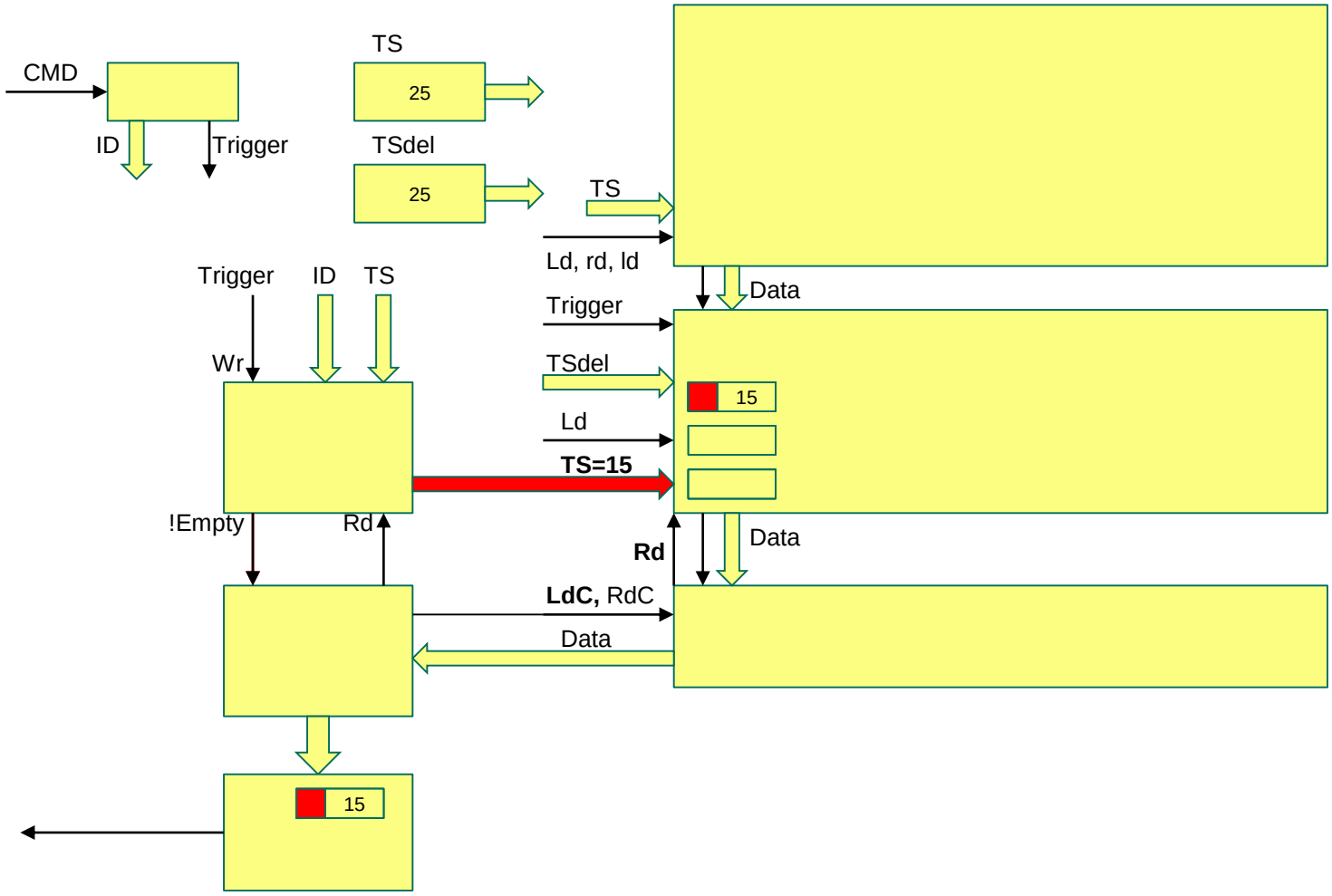
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Trigger
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!Empty
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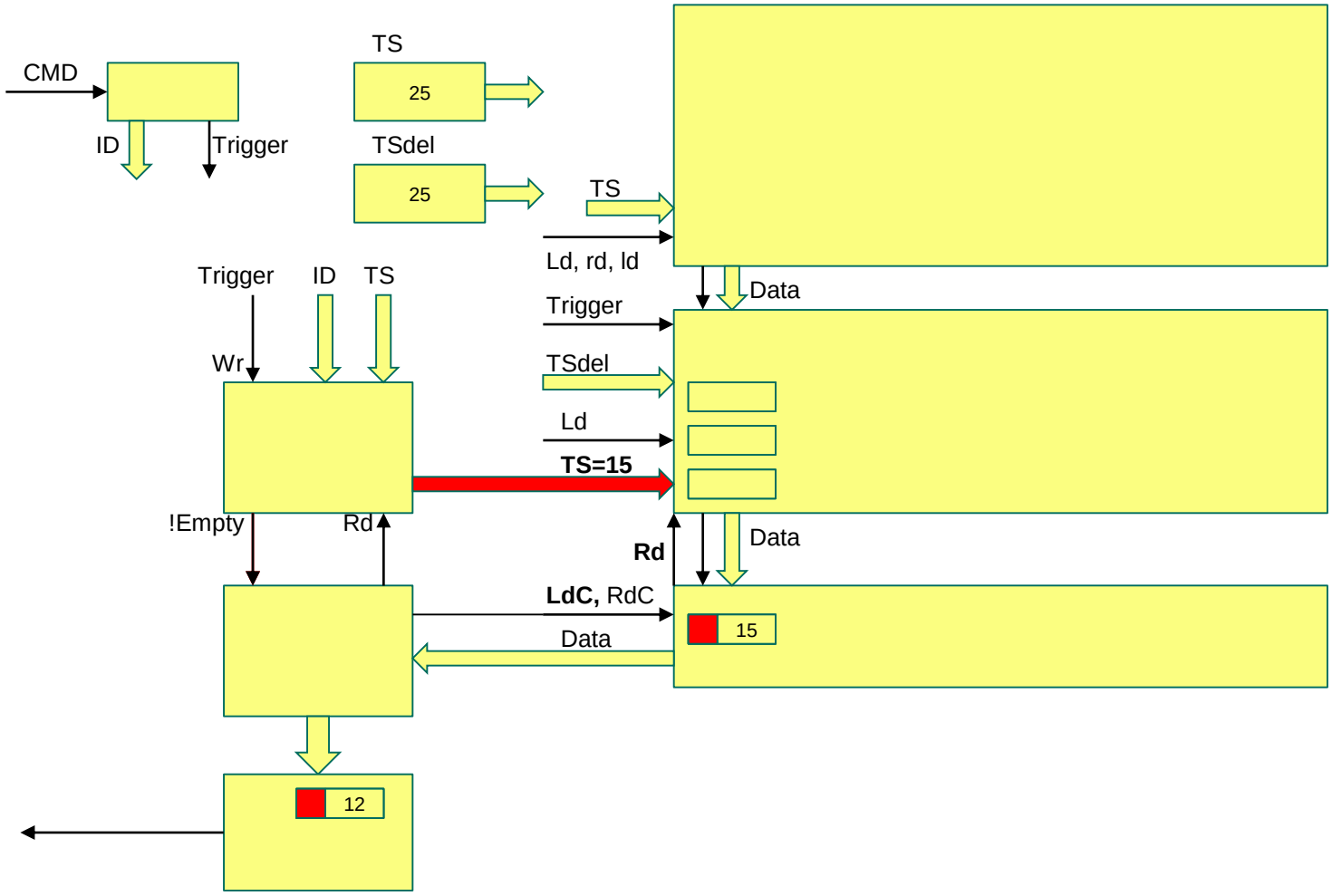
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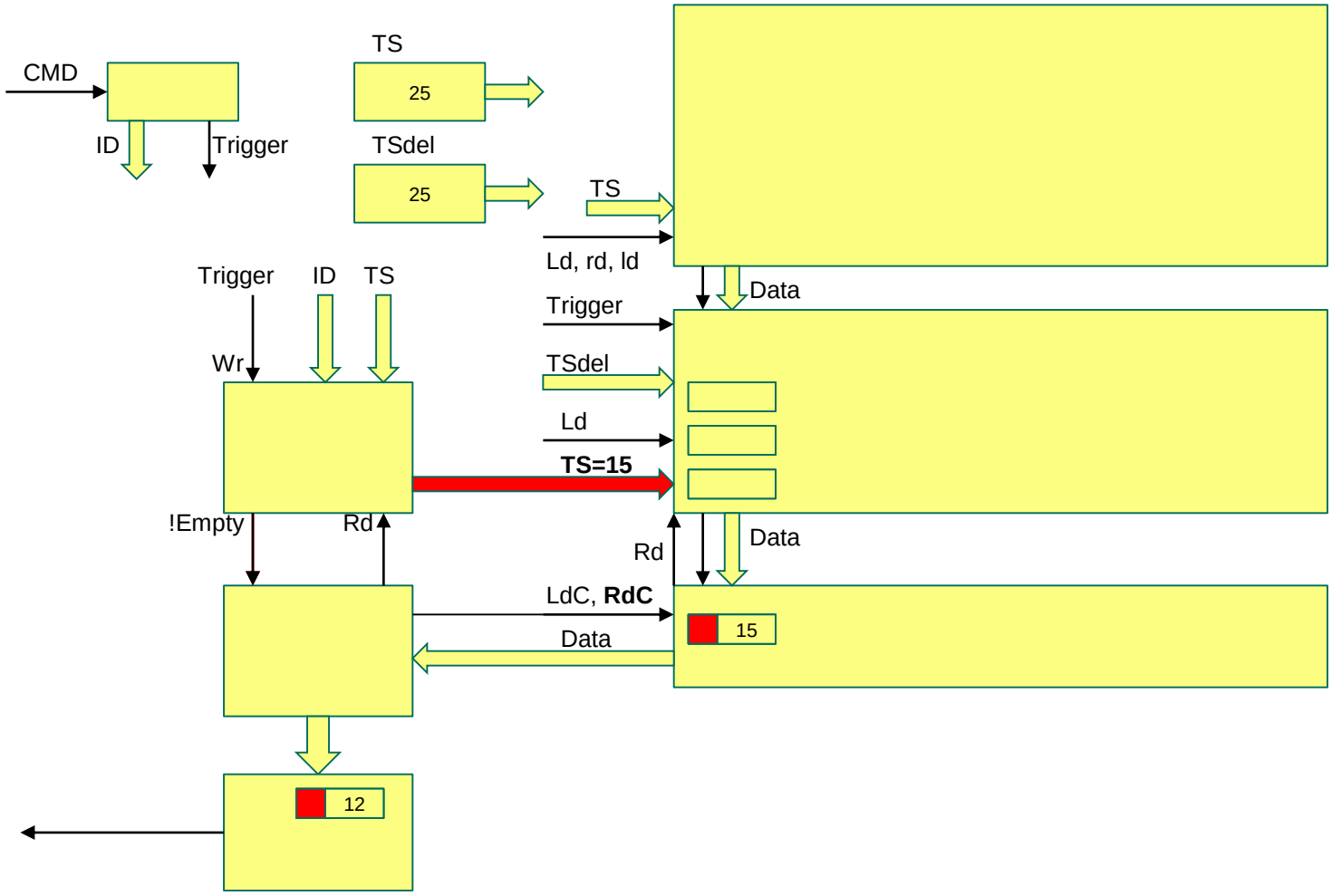
CMD
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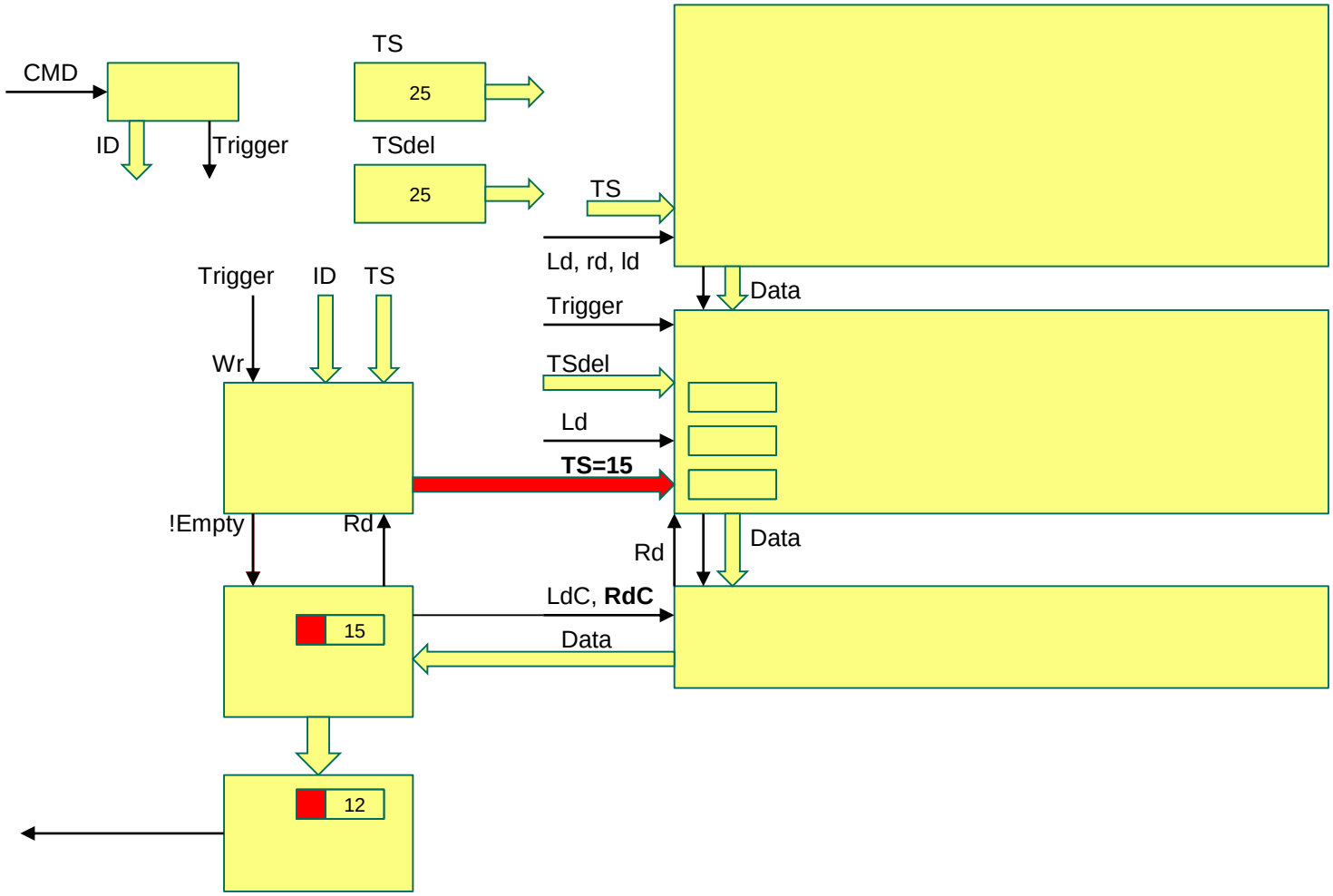
CMD
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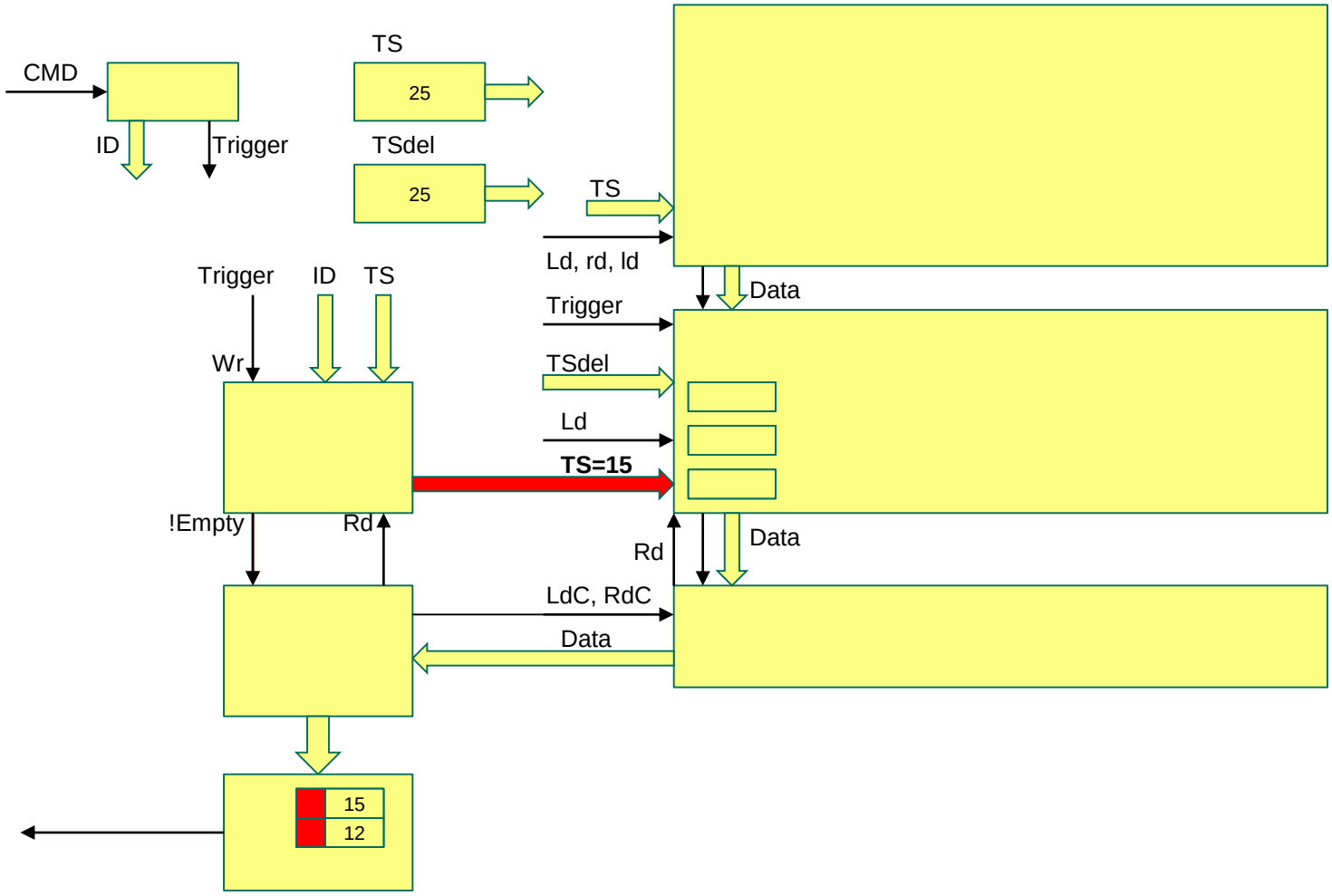
CMD
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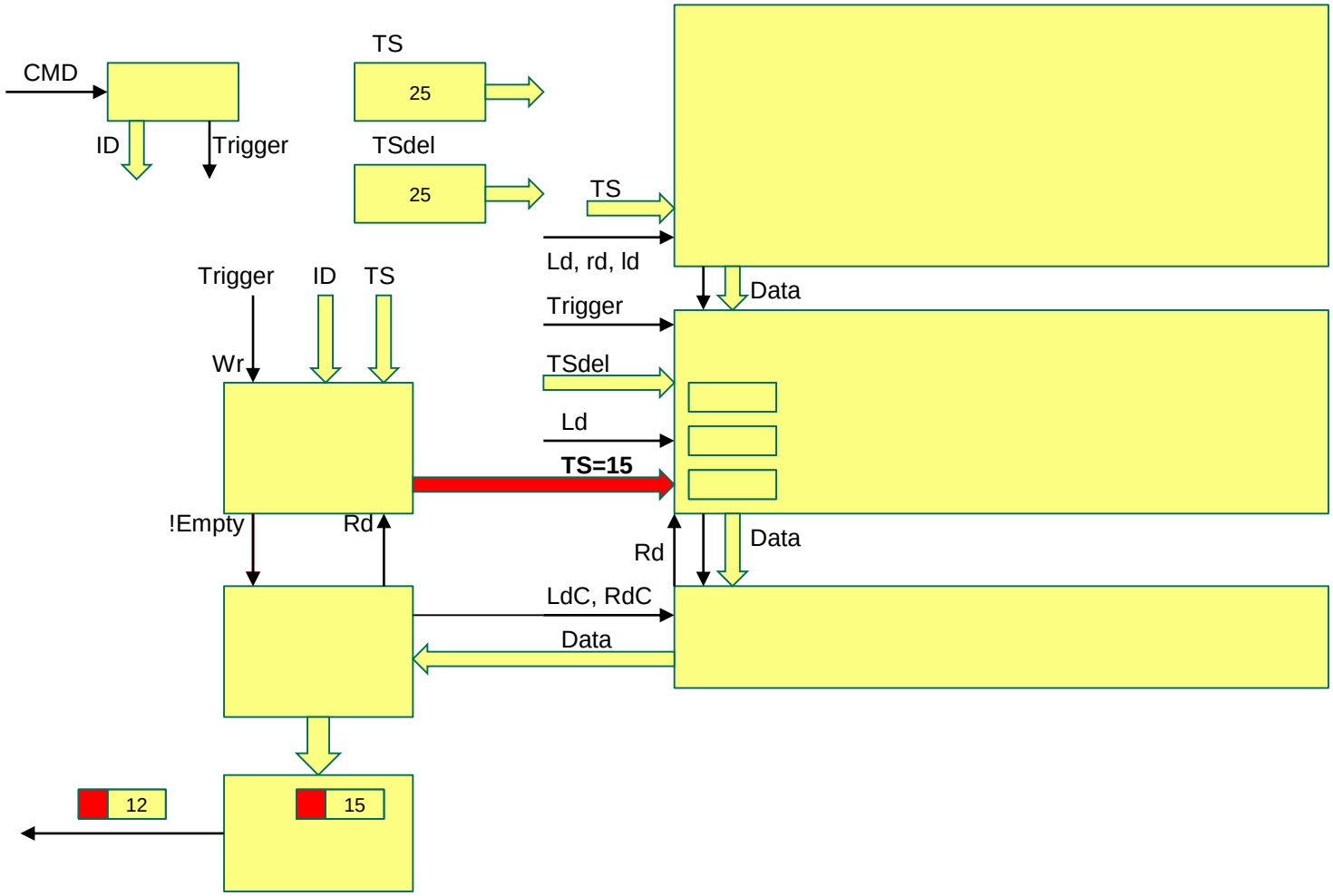
CMD
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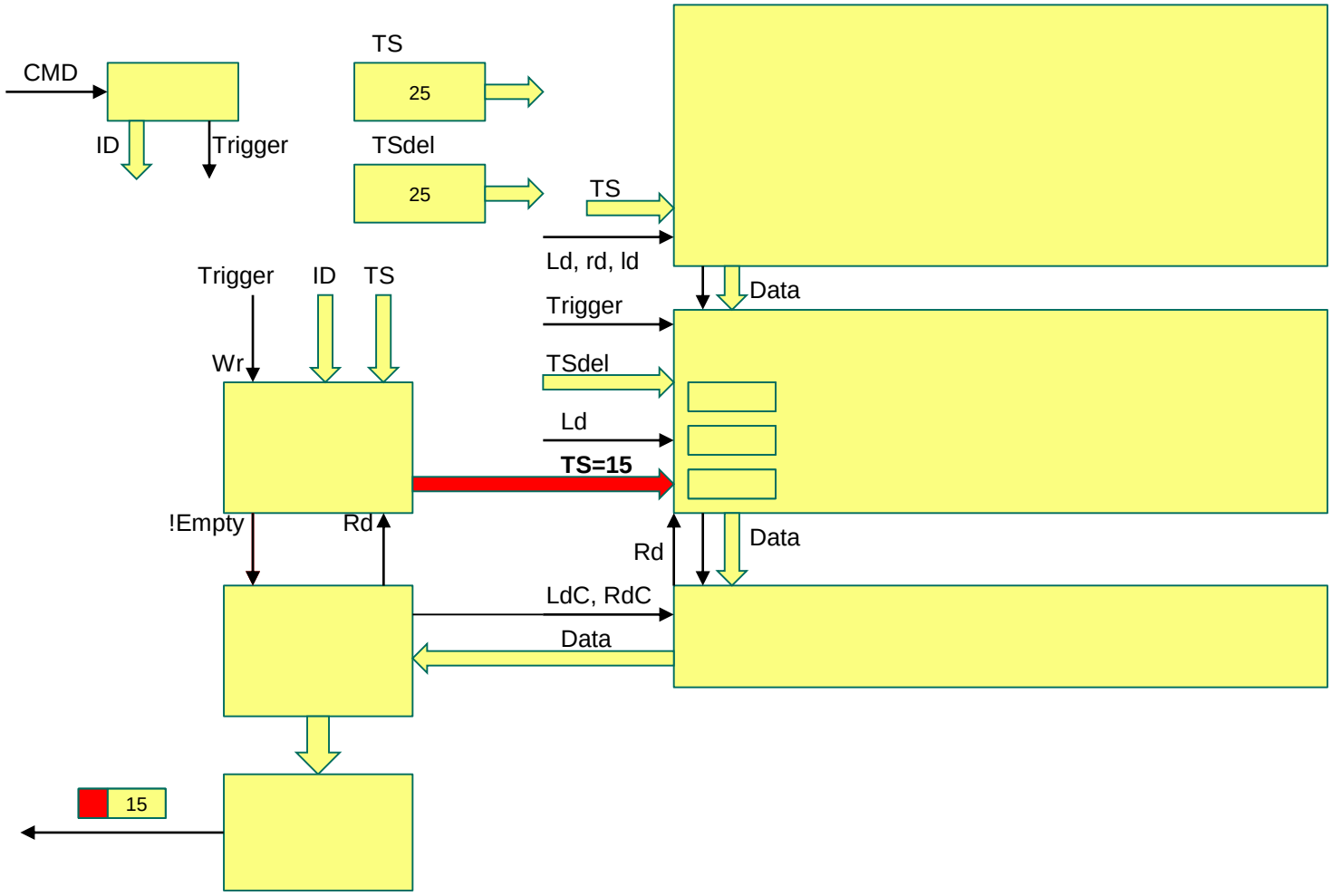
CMD
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LdC, RdC
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Trigger
ID
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!Empty
Rd
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