TIGER: Turin Integrated Gem Electronics for Readout

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INFN Turin

COMPASS Front-End, Trigger and DAQ Workshop

CERN, 02.03.2020

Outline

- ASIC design
- TIGER performance
  - Test system
  - Electrical characterization
  - Results from tests with GEM detectors
- Summary and outlook

TIGER ASIC

Turin **I**ntegrated **G**em **E**lectronics for **R**eadout

Front-end ASIC for GEM readout

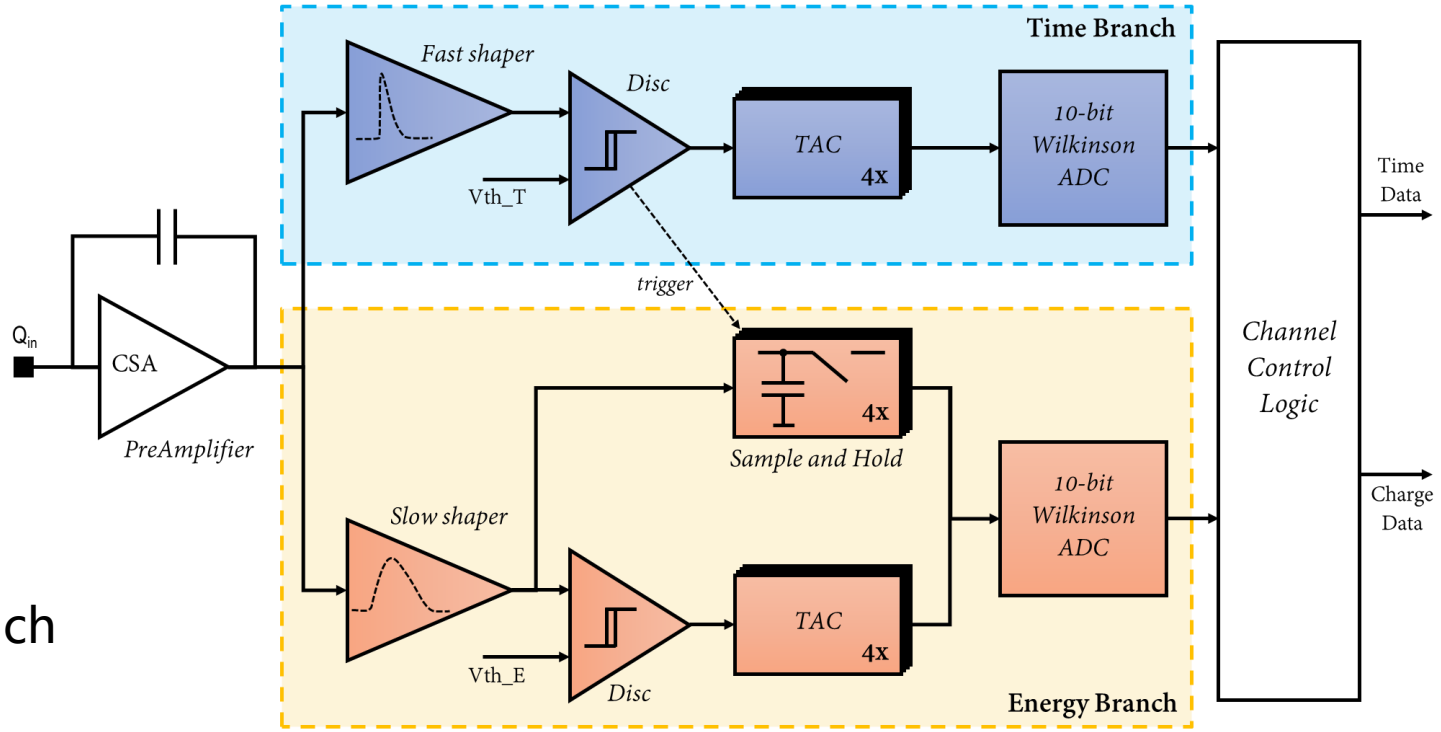
- TIGER has been designed for the readout of the **CGEM-IT** (Cylindrical Gas Electron Multiplier Inner Tracker)
  - new inner tracker of BESIII Experiment (summer 2021)
  - **10 000 channels** readout by 160 **64-channel TIGER ASICs**
- **Time** and **charge** measurements with fully-digital output
  - **Charge centroid** and **μ-TPC** algorithms
  - 130 μm spatial resolution with strip pitch of 650 μm
  - Reduced number of electronics channels (10 000 *vs* 25 000)
- Sensor capacitance dependent on strips length, up to **100 pF**
- Input charge: **2 - 50 fC**
- Time resolution for μTPC mode: **5 ns**
- Rate per channel: **60 kHz** (4x safety factor)
- Power consumption: **< 12 mW/ch**
- SEU-tolerant

CGEM-IT design specs

Efficiency	98%
Rate capability	10 kHz/cm^2
$\sigma_{r\Phi}$	130 μm
σ_z	1 mm
σ_{pt}/p_t	0.5% at 1 GeV/c
Coverage	93% 4π
Material budget	< 1.5 X_0
Inner radius	78 mm
Outer radius	178 mm
Magnetic field	1 T

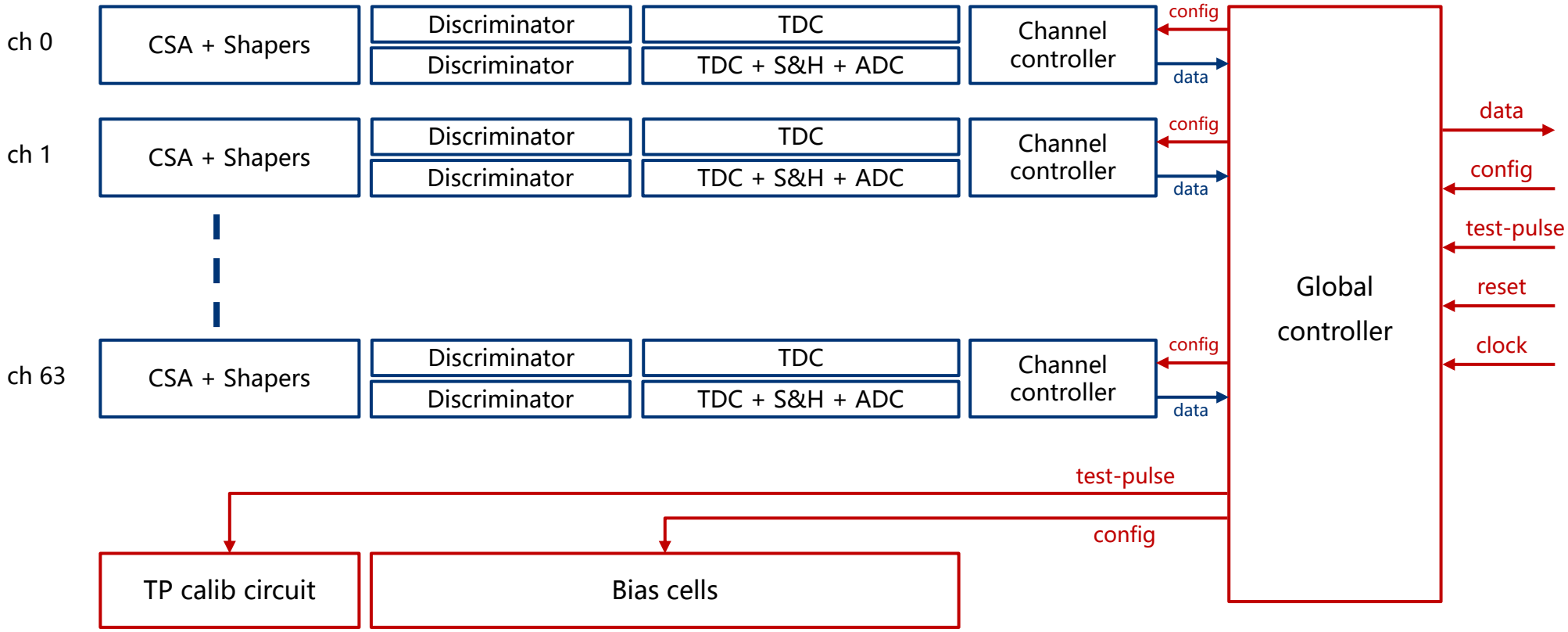
Channel architecture

- Analogue Front-End:
  - **Charge Sensitive Amplifier**
  - **dual-branch** shaper optimized for time and charge measurements
- **Trigger-less** readout architecture:
  - 2 LE discriminators with 6-bit DAC for threshold equalization
  - dual-threshold readout mode
- **Timestamp** on rising edge of fast branch
  - Time resolution < 5 ns
  - Low-power TDCs based on analogue interpolation
- **Charge** measurement:
  - ToT: timestamp on rising/falling edge
  - S&H: slow shaper output sampled and digitized with a 10-bit Wilkinson ADC

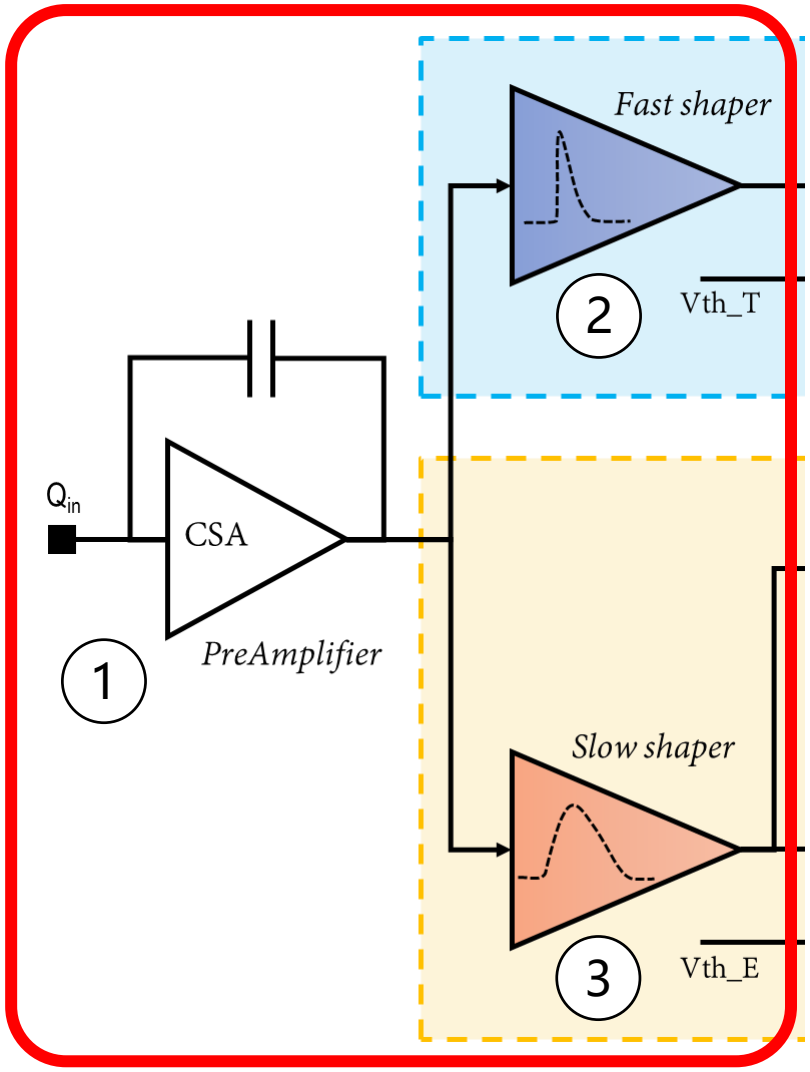


ASIC architecture

The ASIC comprises 64 channels, a digital global controller, bias and references generators and a test-pulse calibration circuit.



Analogue Front-end



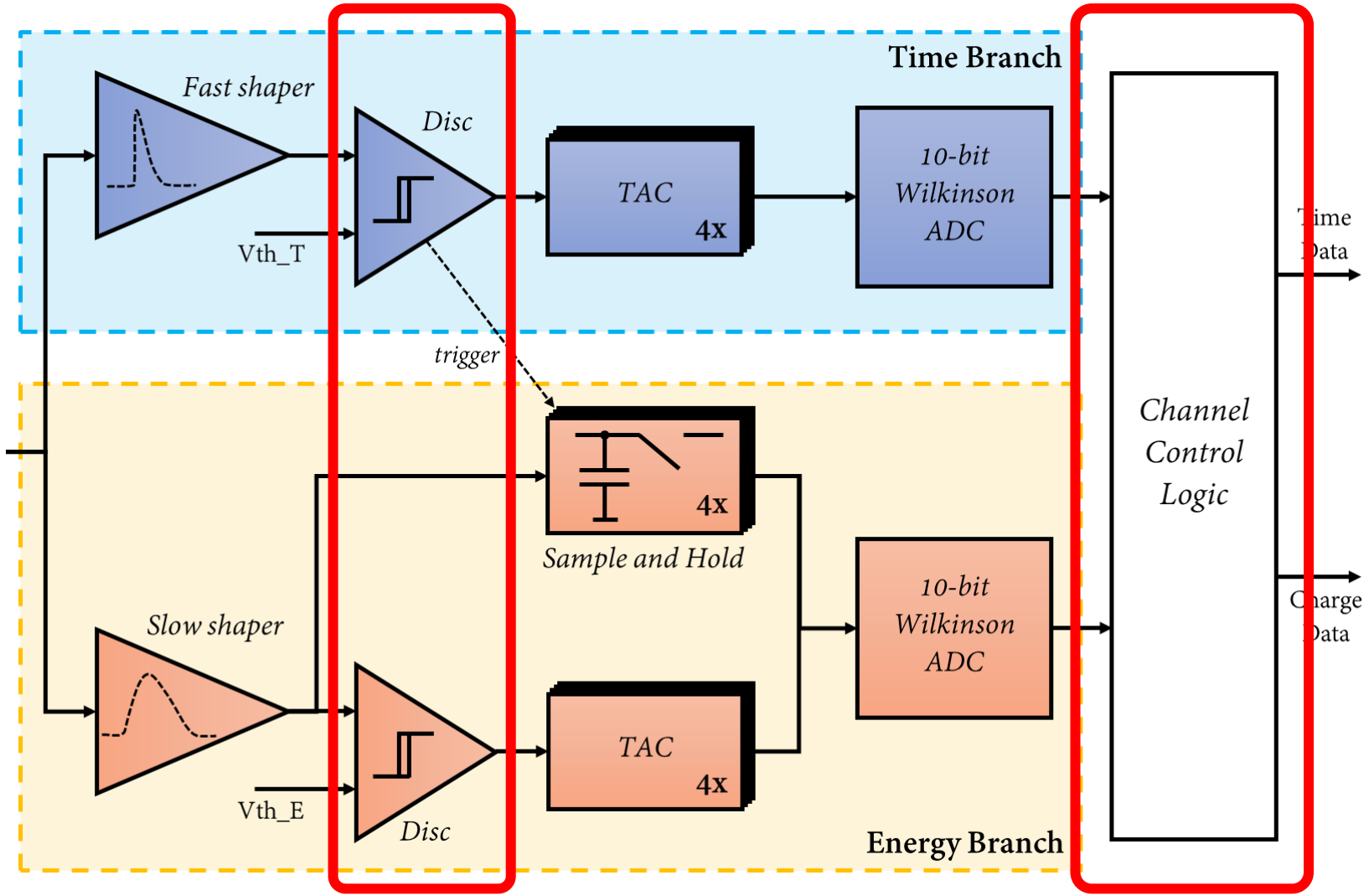
1. **CSA pre-amplifier**
   - Q_{in} = 2 - 50 fC
   - input transistor bias current set by 6-bit DAC (1.5 – 4.5 mA)
   - ENC target < 2000 e^- @ C_{in} = 100 pF
2. **Time-branch**
   - Simple CR-RC shaper
   - 60 ns peaking time for low-jitter timing measurement
3. **Energy-branch**
   - 4 complex-conjugate poles shaper for a more gaussian signal shape to reduce pile-up probability
   - 170 ns peaking time for signal-to-noise ratio optimization

- **BLH** to lock the shapers output DC to an external reference value (V_{BL} = 350 mV)

➢ Total gain ≈ 12 mV/fC

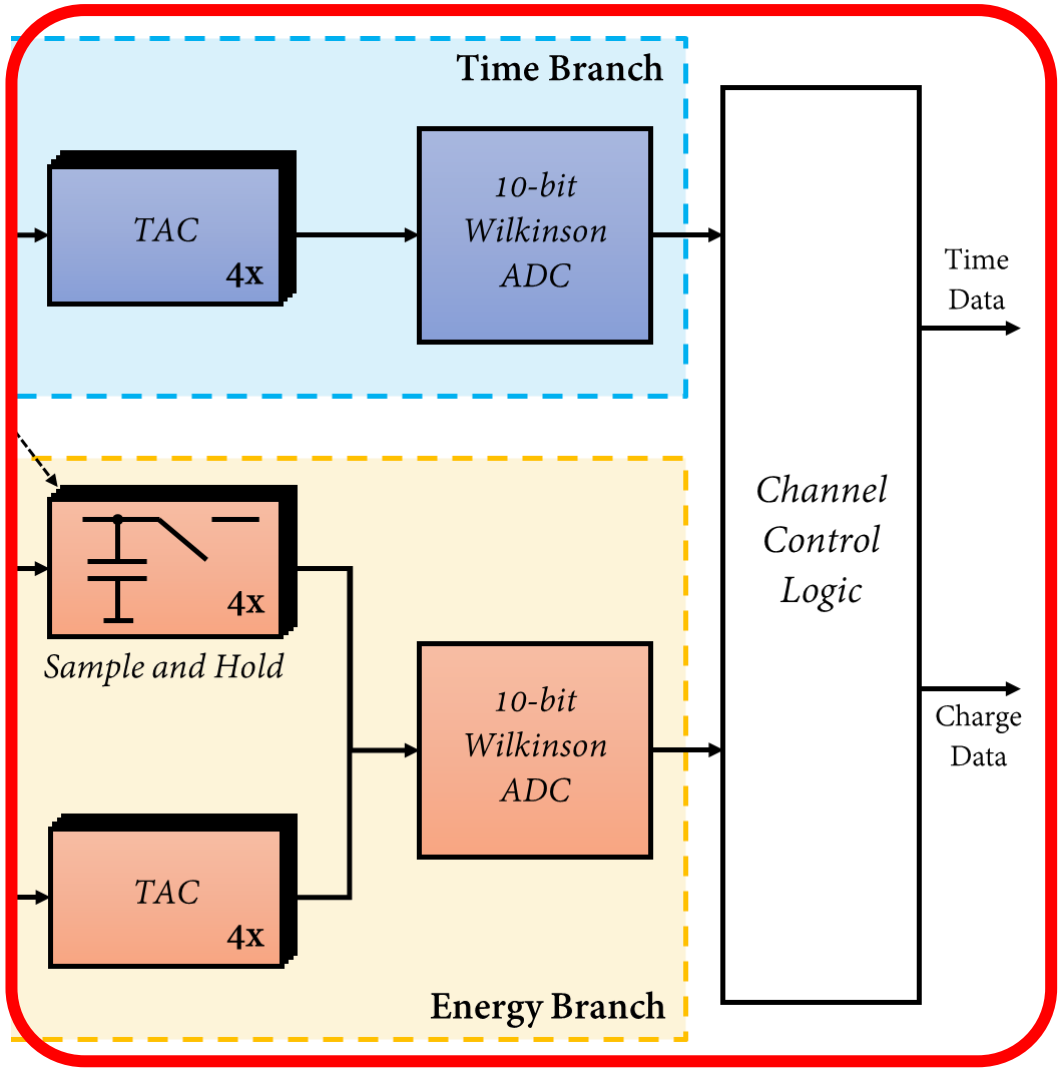
Trigger-less readout

- **LE discriminators** with 6-bit DAC programmable thresholds and 3-bit DAC hysteresis
- **Data-push** readout architecture: each signal above the selected threshold is taken as a good event, digitized and sent off-chip (no external trigger)
- **Dual-threshold** readout mode to reduce events induced by noise



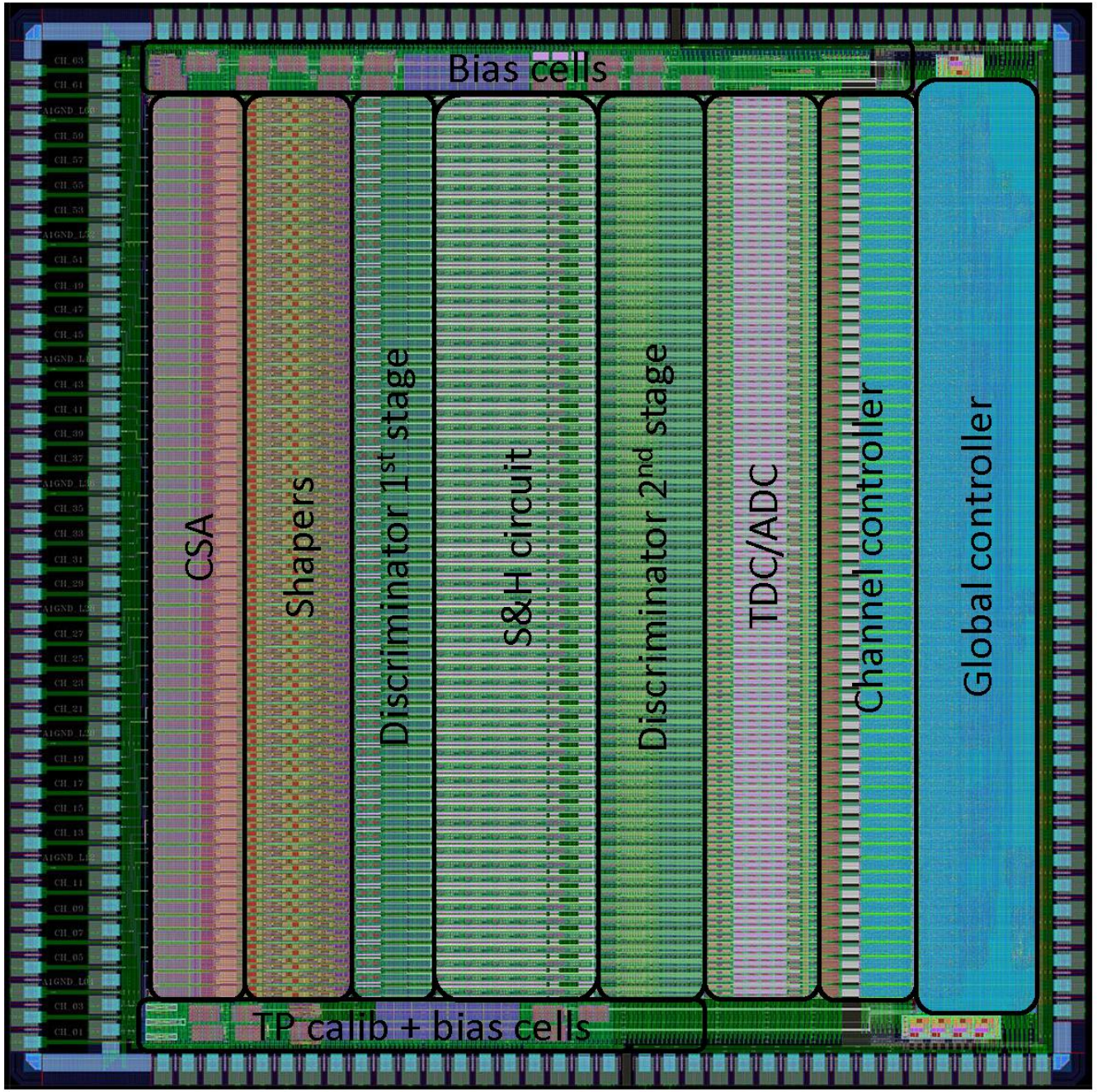
Time and charge measurements

- **Coarse time measurement** from the chip master clock counter
- **Fine time measurement** with low-power analogue TDCs based on time interpolation (I.F. = 128)
  - 50 ps time binning @ 160 MHz
  - Quad-buffered TACs for **event de-randomization**
  - TAC buffers with refresh scheme to avoid off-chip correction algorithm for leakage
- **Charge measurement** with S/H circuit sampling the E-branch shaper output
  - Programmable sampling time targeting the **signal peak**
  - Digitization with **Wilkinson ADC** shared with the TDC
  - Quad-buffered sampling capacitors for **event de-randomization**
- **Charge measurement** from ToT information by operating both branches in TDC mode (backup solution)



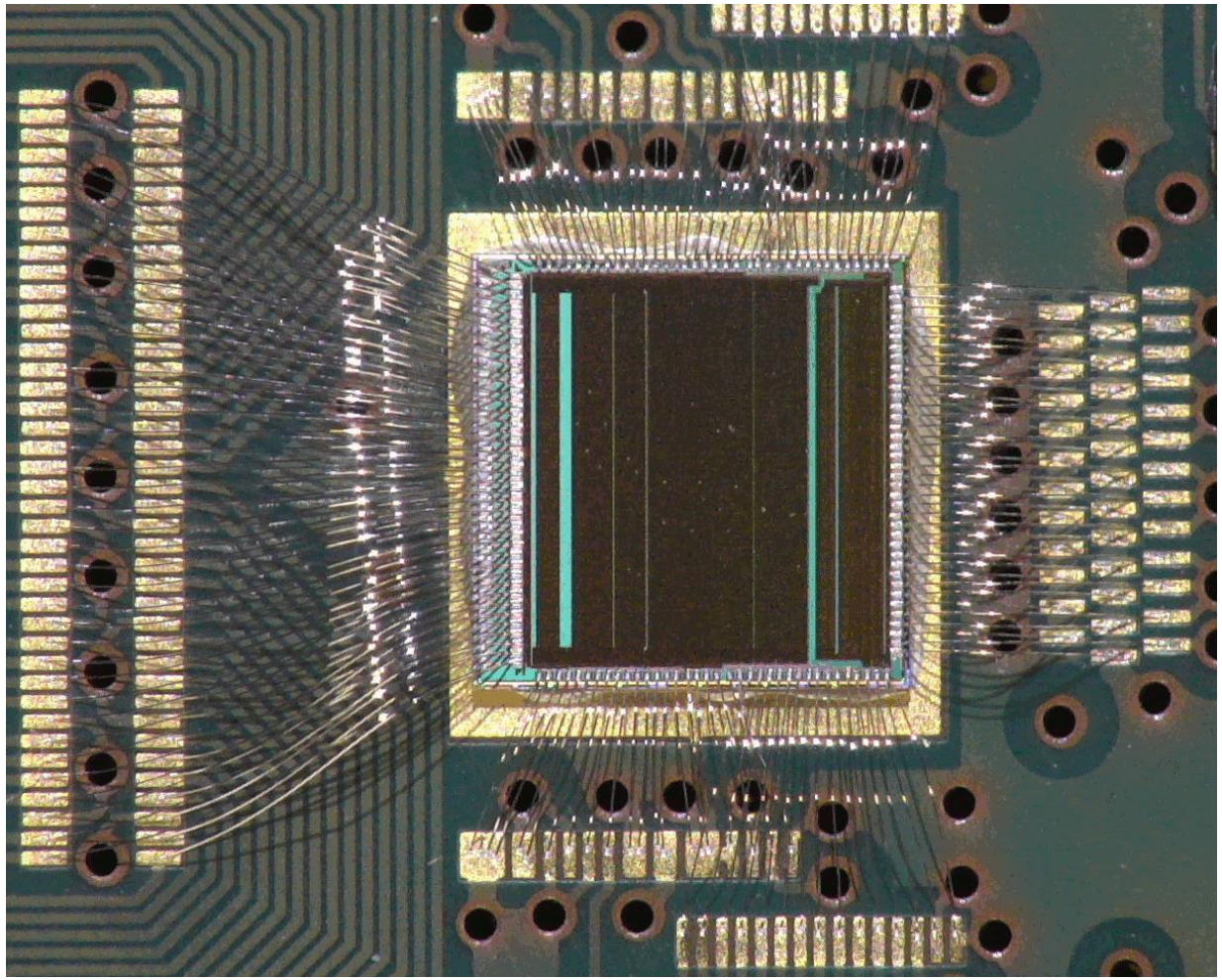
TIGER specs

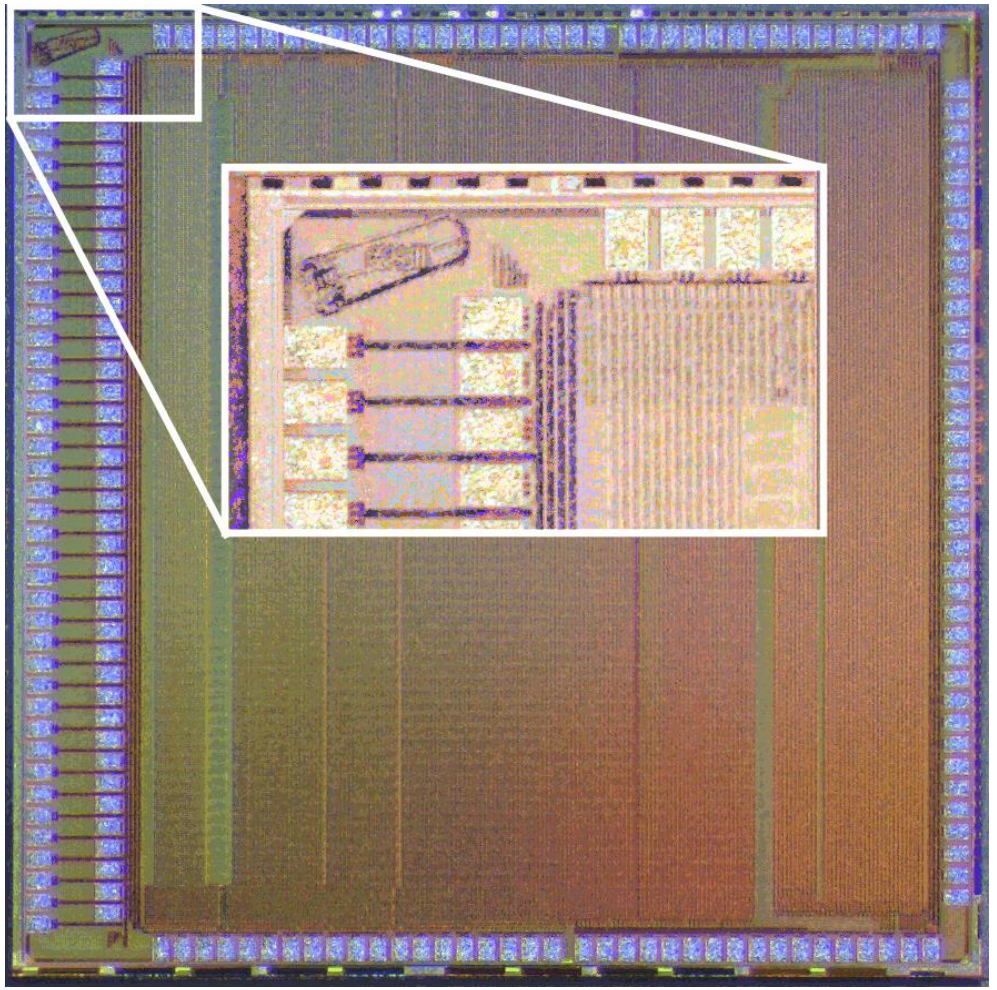
- 5 x 5 mm^2 110nm CMOS technology
- Digital backend from **TOFPET2 ASIC** (SEU protected)
- **64 channels**: CSA, shapers, TDC/ADC, local controller
- On-chip bias and power management
- On-chip calibration circuitry
- **Trigger-less** operation, fully digital output
- 160-200 MHz system clock
- 4 TX SDR/DDR LVDS links, 8B/10B encoding
- 10 MHz SPI-like configuration link
- Power consumption < **12 mW/ch**
- Sustained event rate > **100 kHz/ch**



TIGER performance

TIGER on PCB test-board



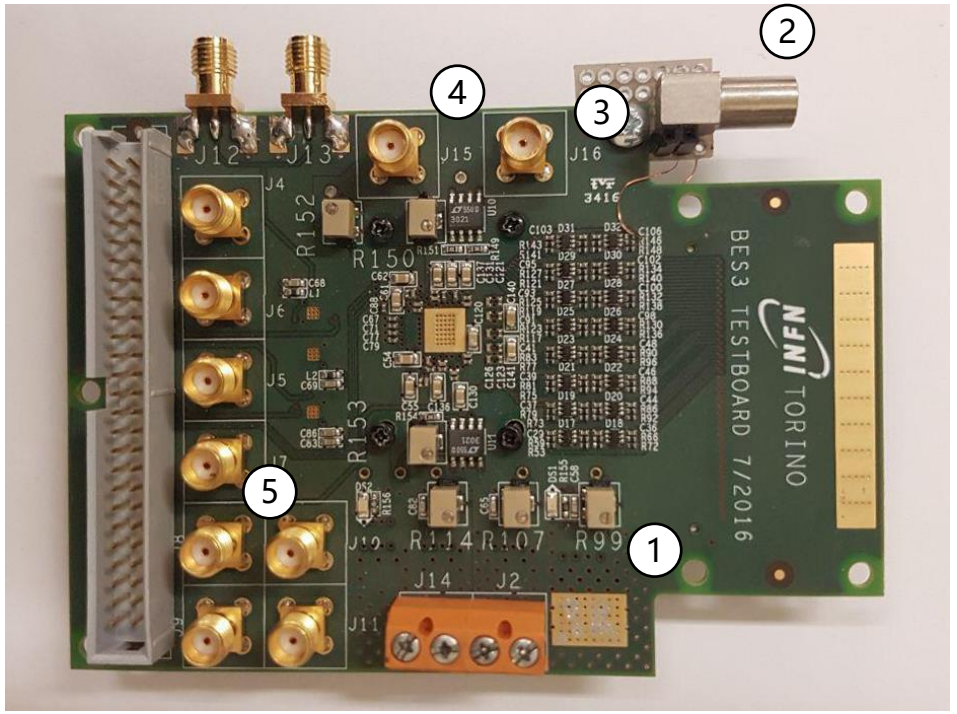


PCB test-board

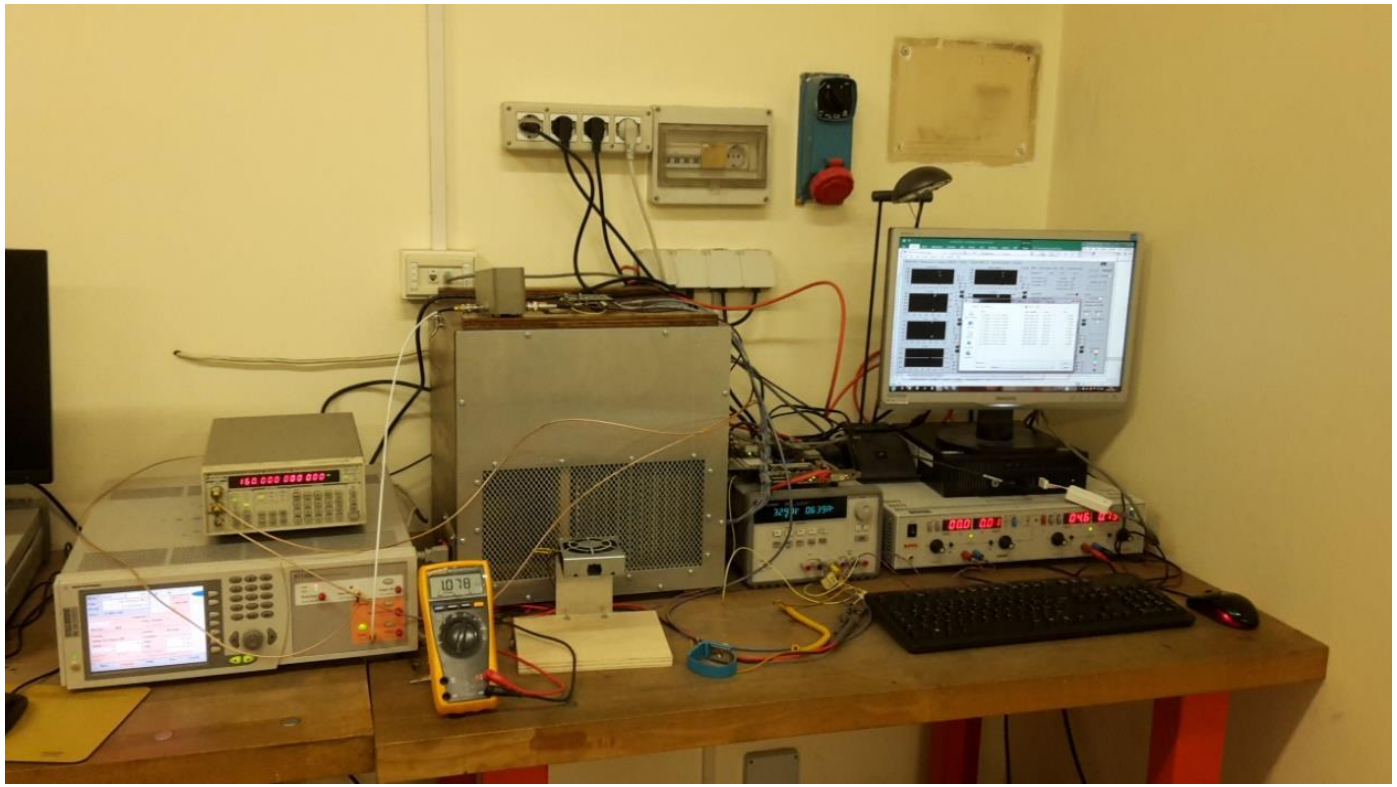
Test-board for ASIC electrical characterization

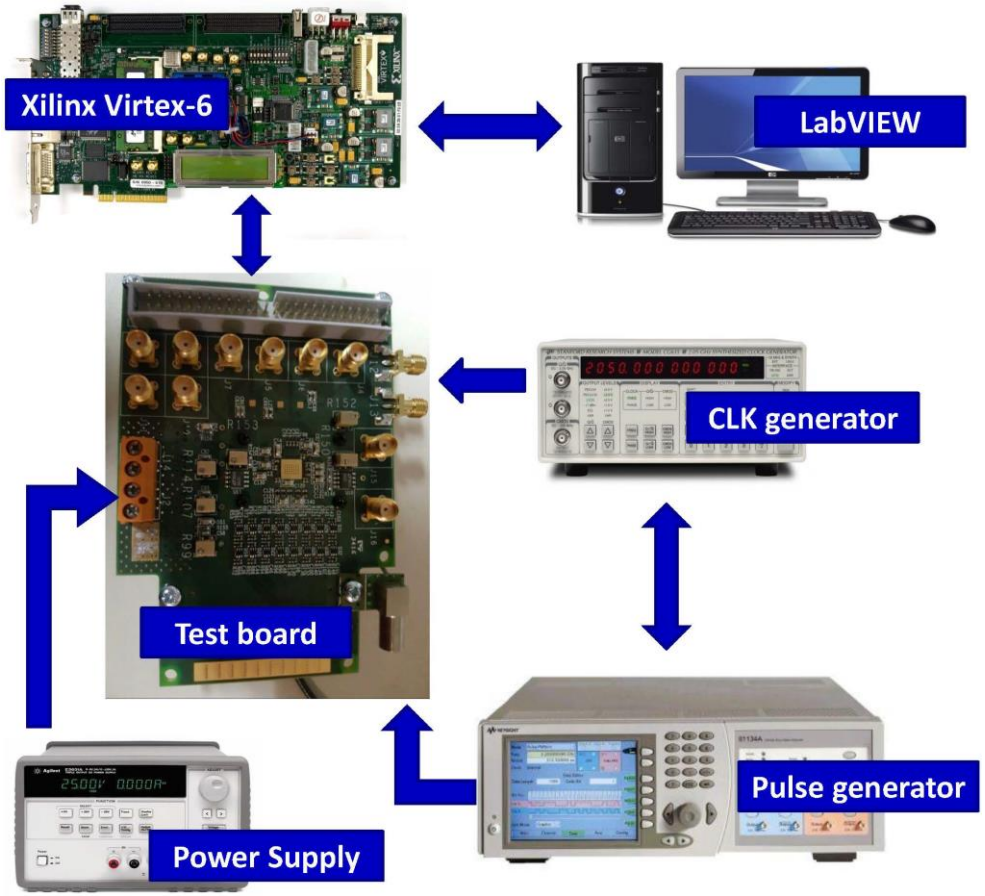
1. Trimming capability for analogue and digital power domains and external reference voltages

- Debug IO ports:
    2. External test-pulse injection
    3. External capacitor insertion
    4. T-branch shaper output and threshold probe points (ch. 63)
    5. Digital back-end control signals (TDC and S&H)

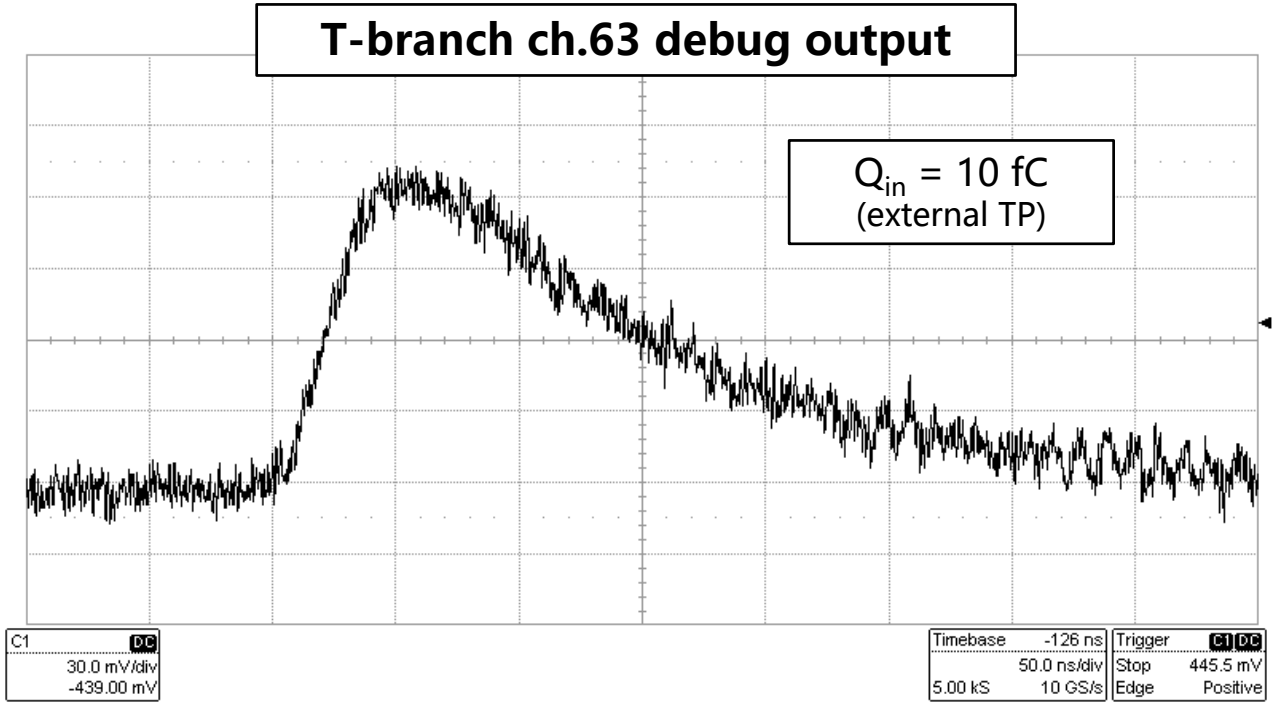


Experimental setup in Torino



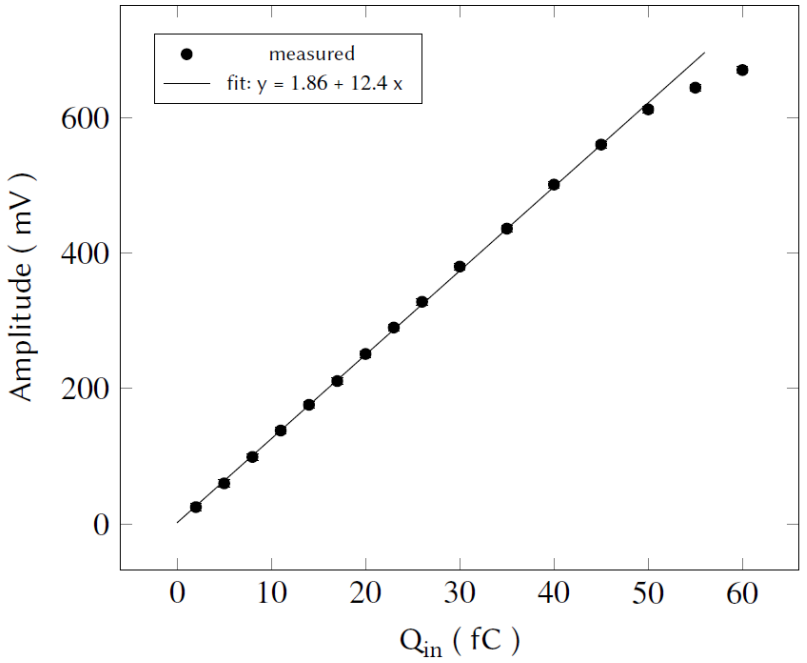


Front-End response



ΔV ≈ 120 mV

Peaking time ≈ 60 ns

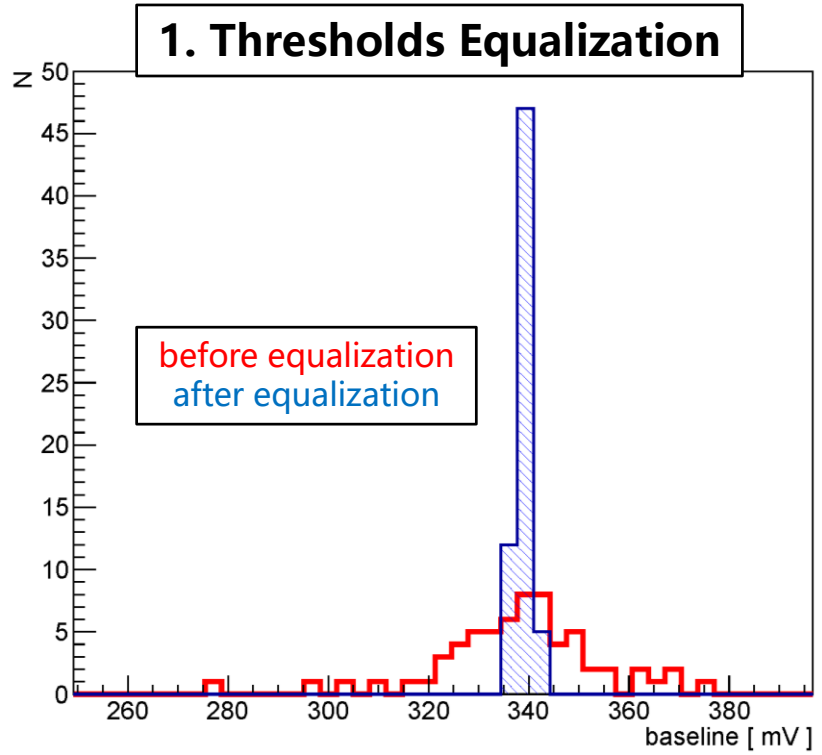


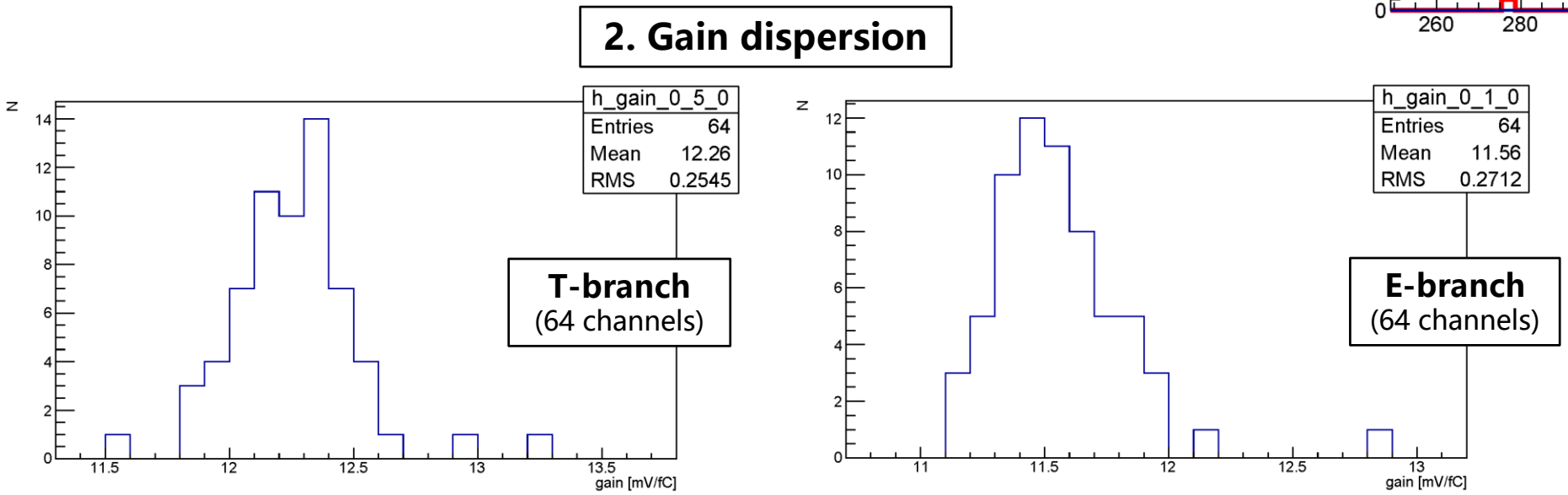
Gain ≈ 12.4 mV/fC

Front-End performance

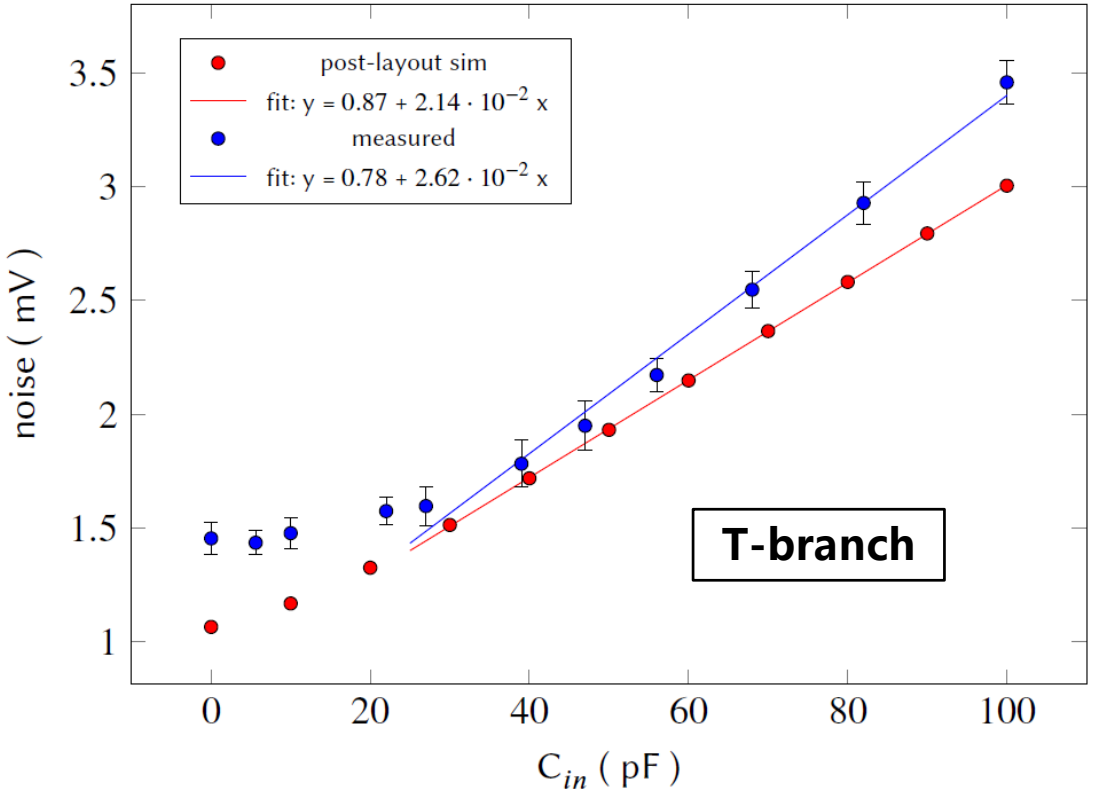
1. V_{th} scan to generate LUT to equalize thresholds
   - ➢ below 5 mV RMS dispersion after V_{th} equalization

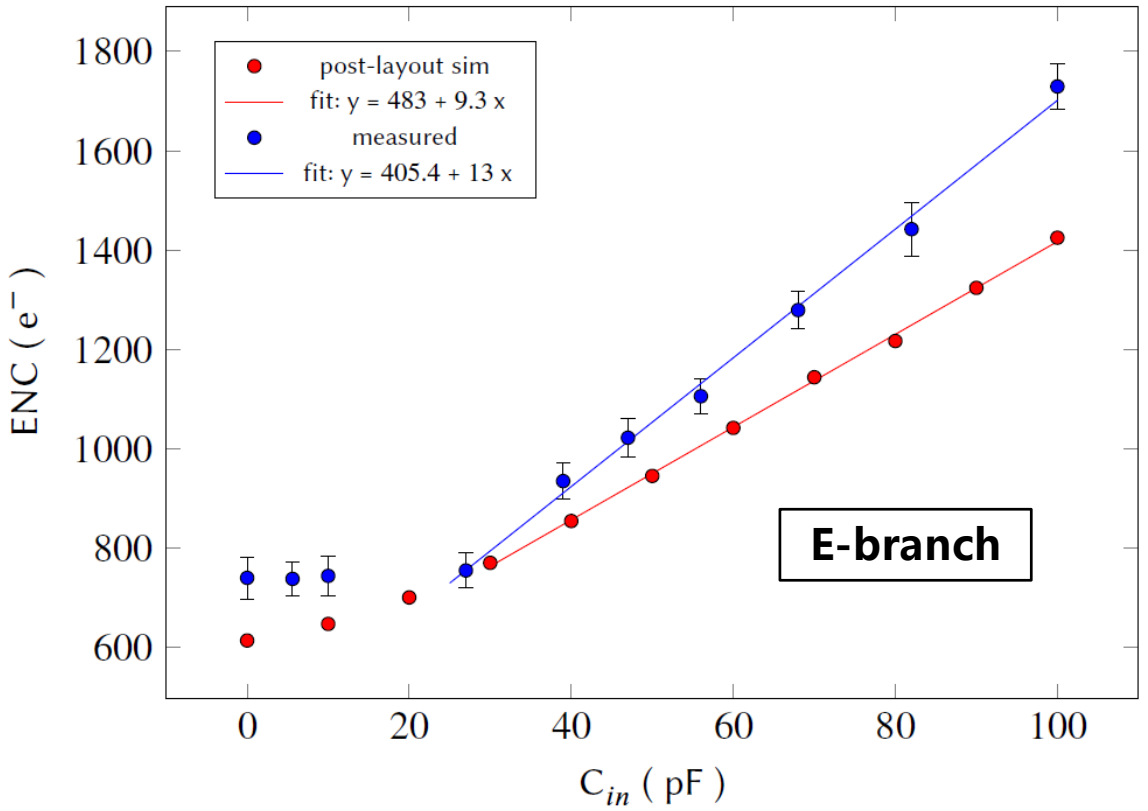
2. V_{th} scan with internal TP to measure gain of 64 channels on both branches





Front-End noise



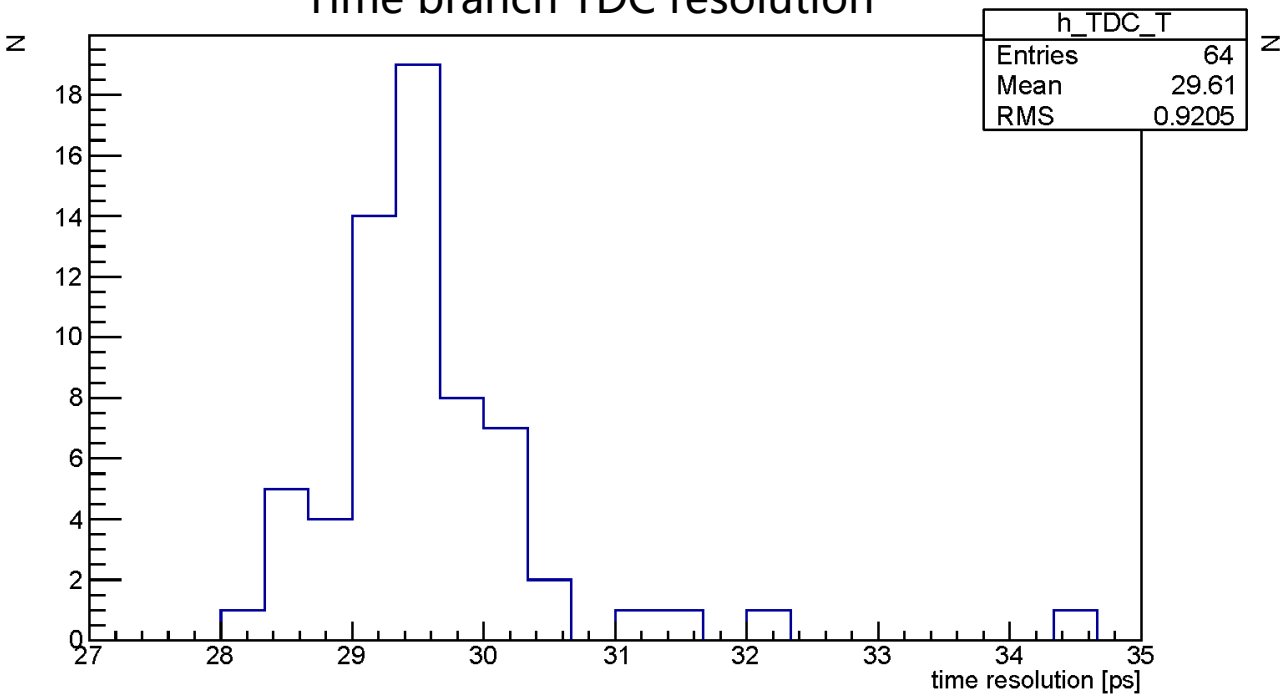


- 15-20% increase from post-layout simulation to silicon measurements
- Plateau at low C_{in} values indicates common-mode noise

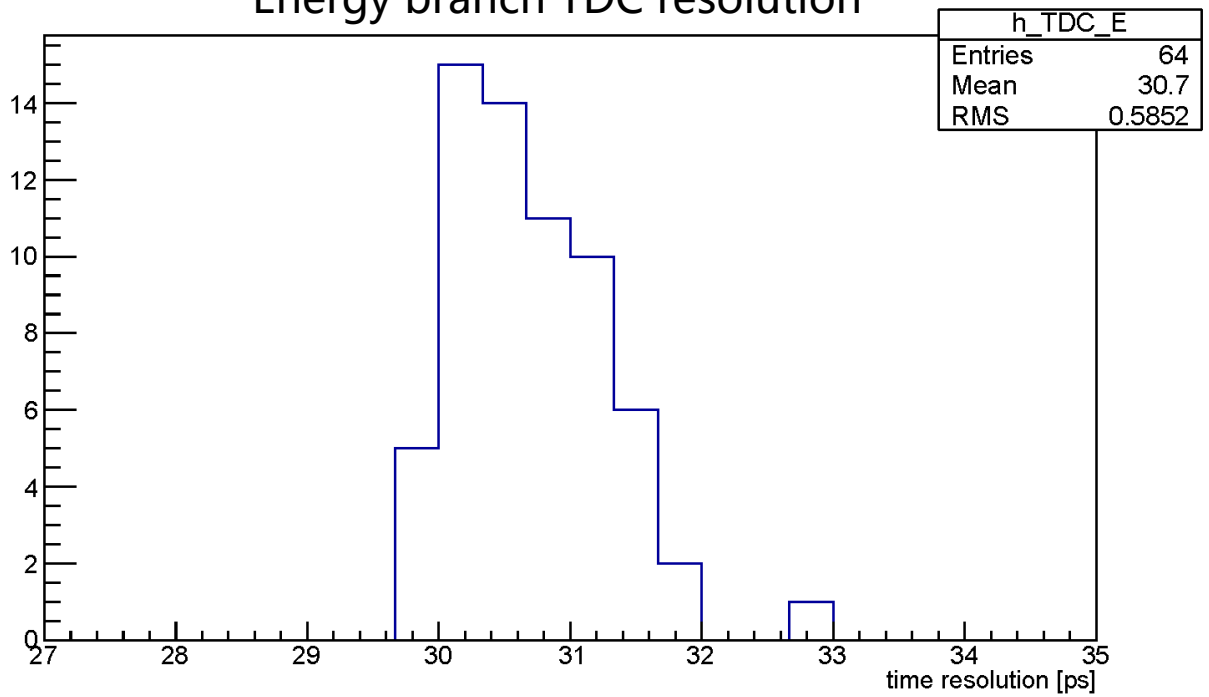
TDC performance

- Digital TP to the TDCs input, scanning phase of one clock cycle
- LUT with gain and offset correction for 64 channels
- TDC **resolution< 50 ps RMS** after calibration

Time branch TDC resolution

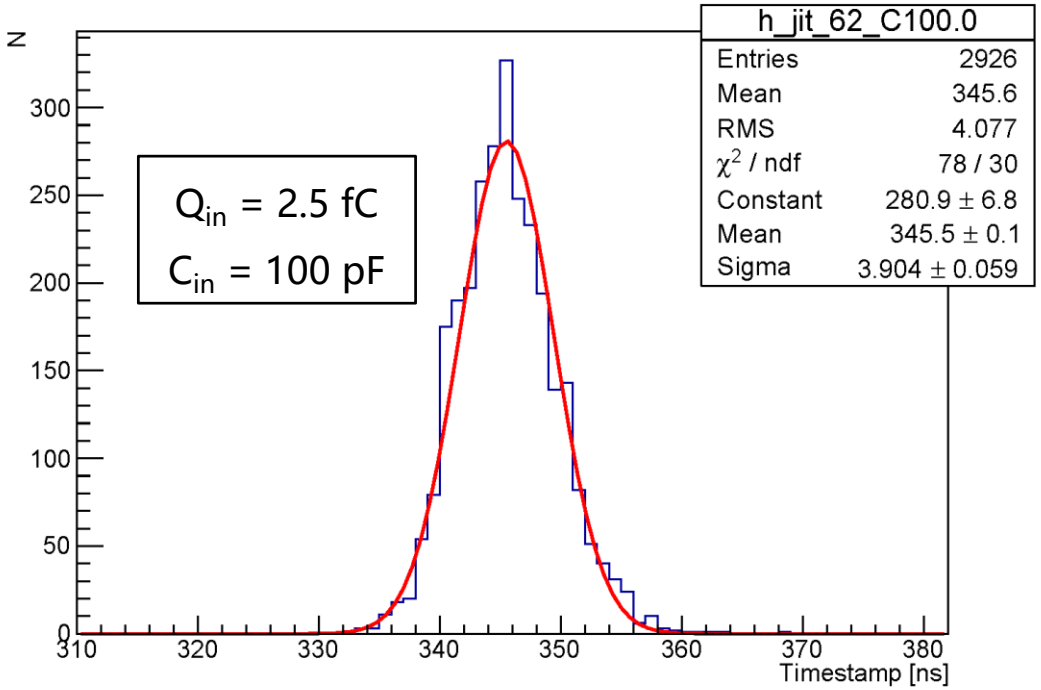


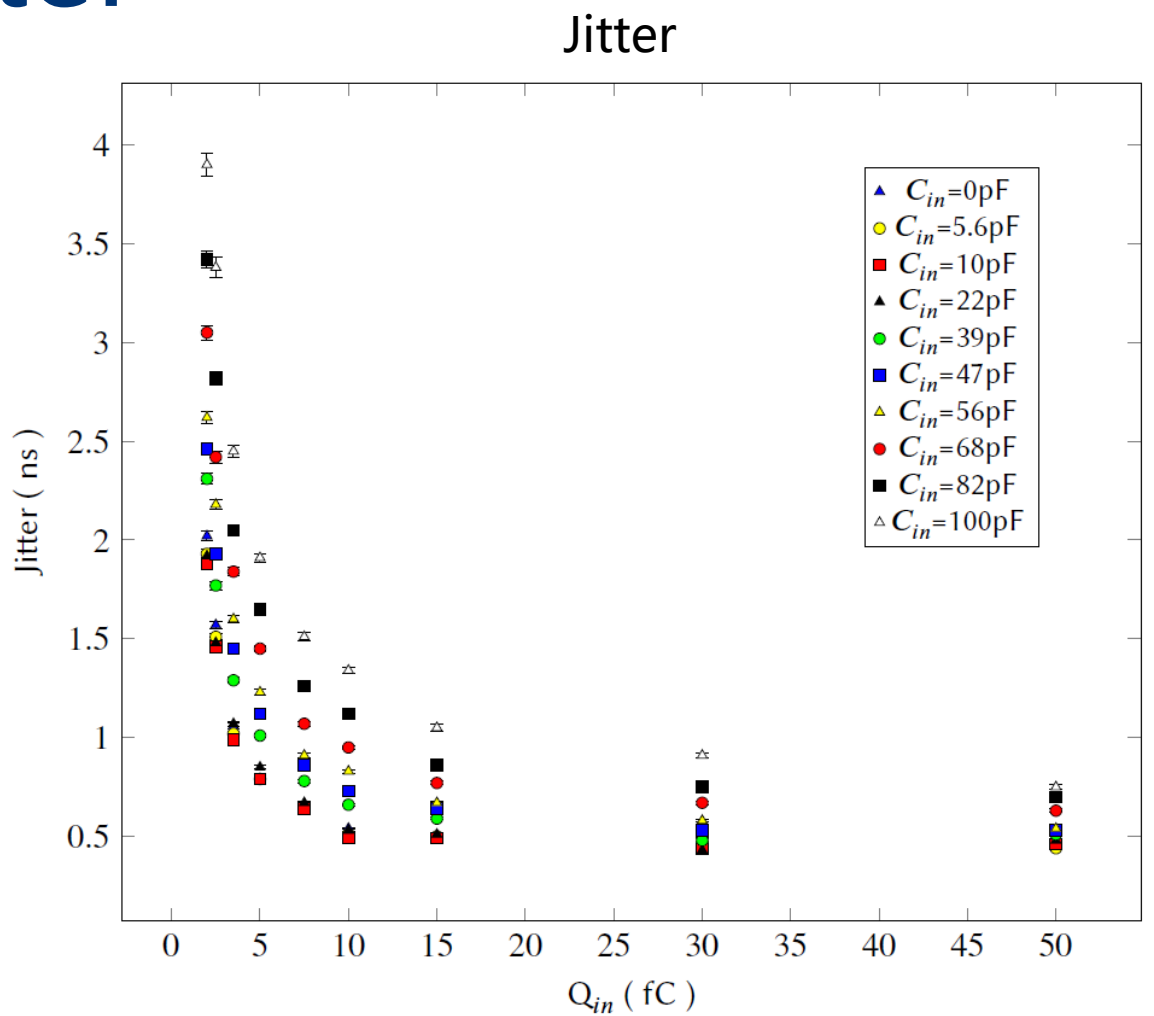
Energy branch TDC resolution



Time resolution - jitter

- Repeated TP with fixed amplitude and timing

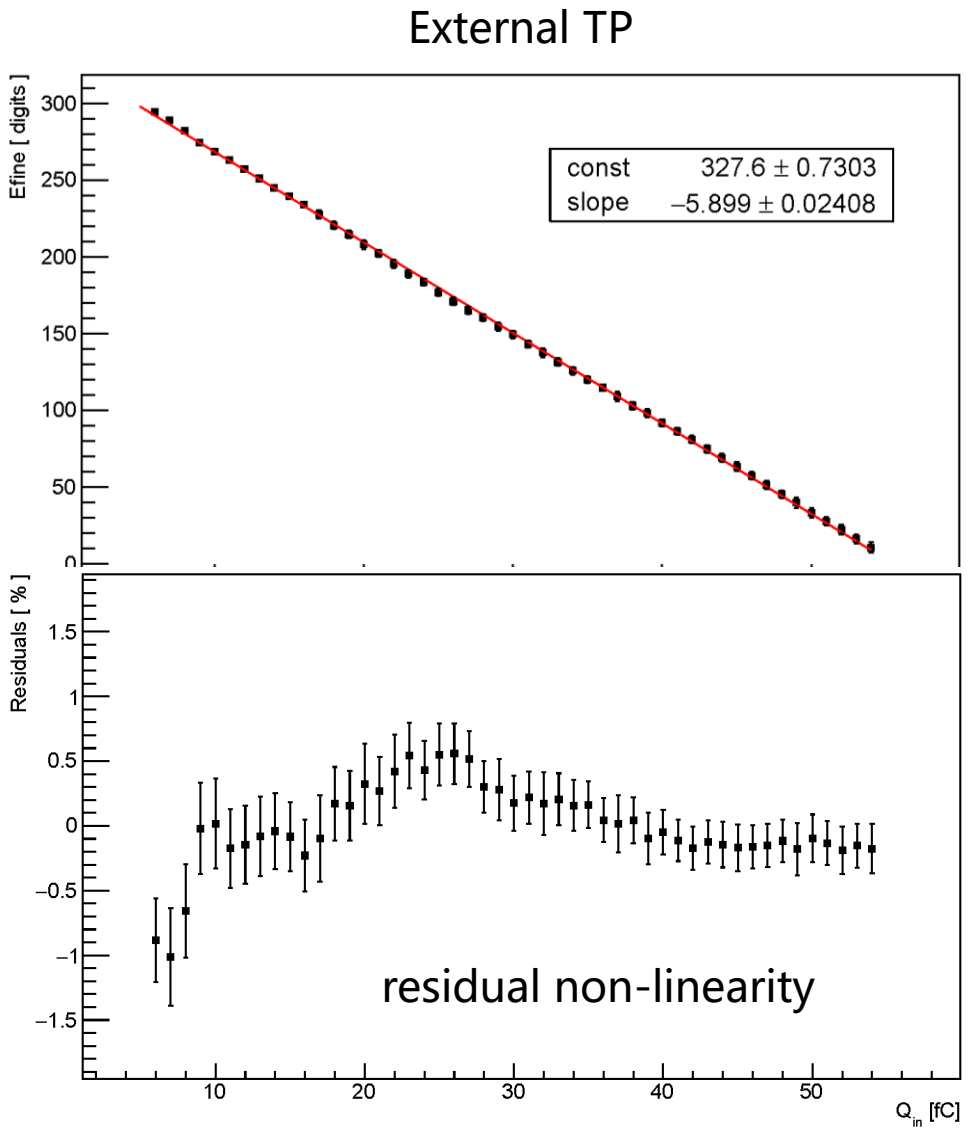




➢ Time resolution dominated by FE jitter contribution

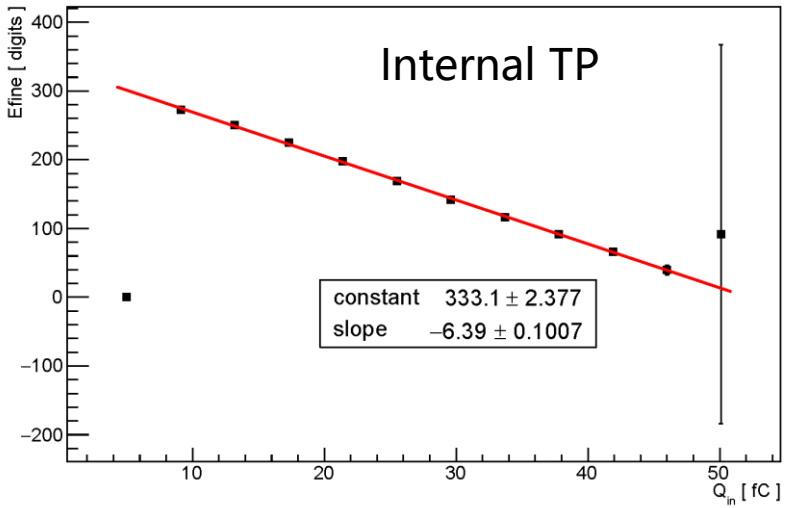
Charge measurement

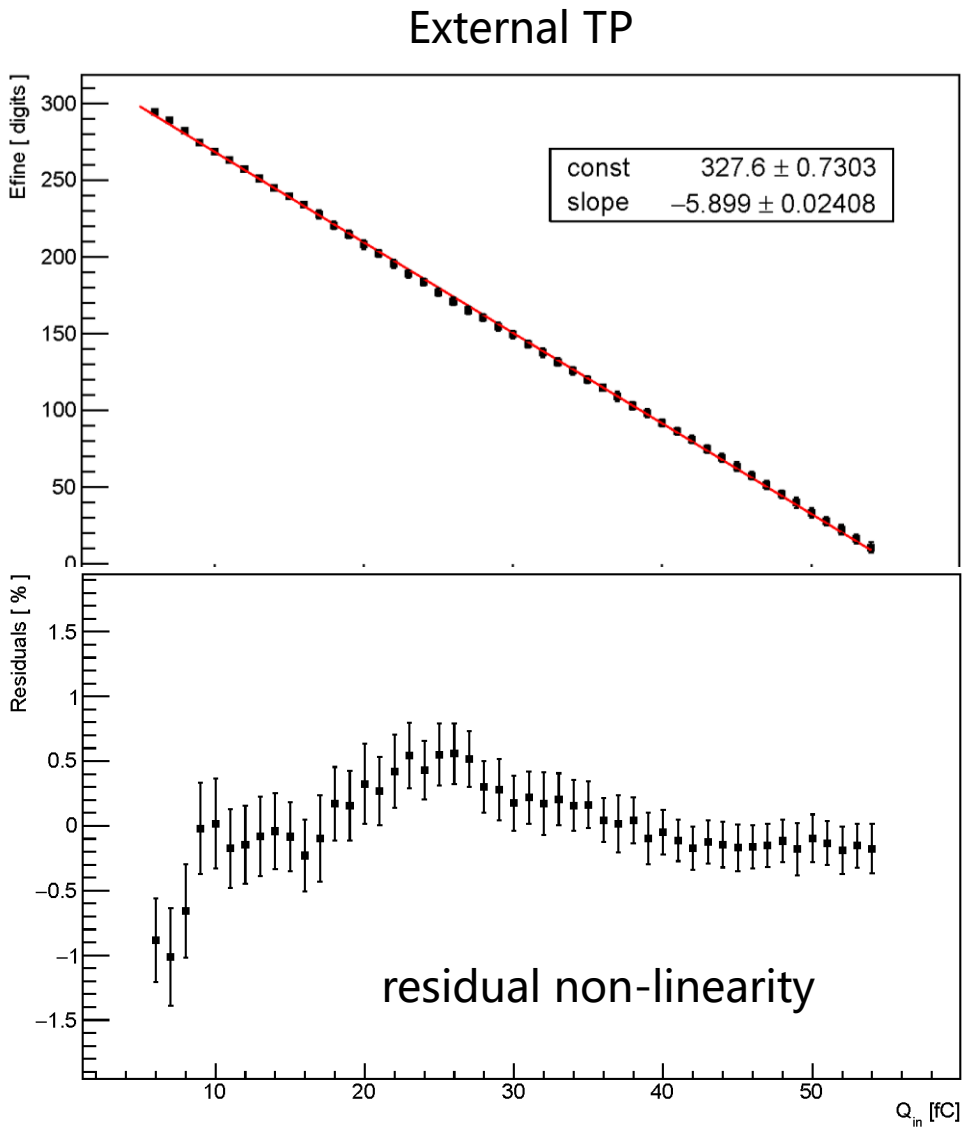
- S/H **dynamic range** and **linearity** with external test-pulse generator (ch. 63 input debug port)



Charge measurement

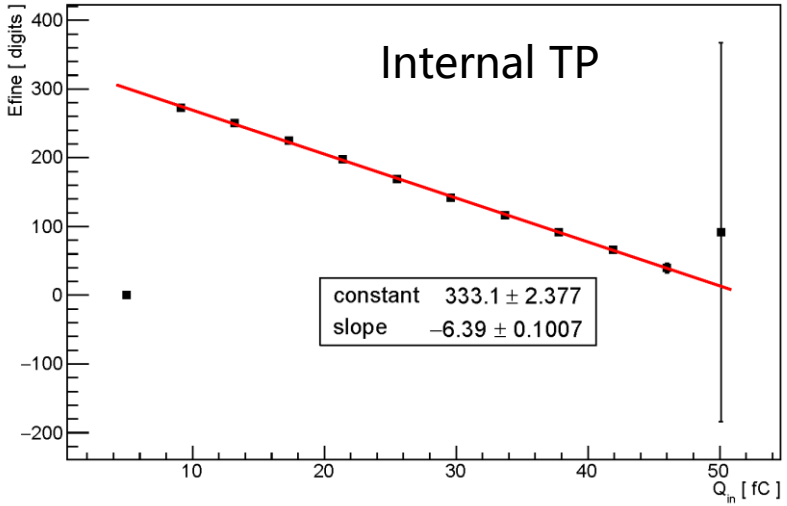
- S/H **dynamic range** and **linearity** with external test-pulse generator (ch. 63 input debug port)
- Back-annotation for **internal test pulse calibration** to assess all channels

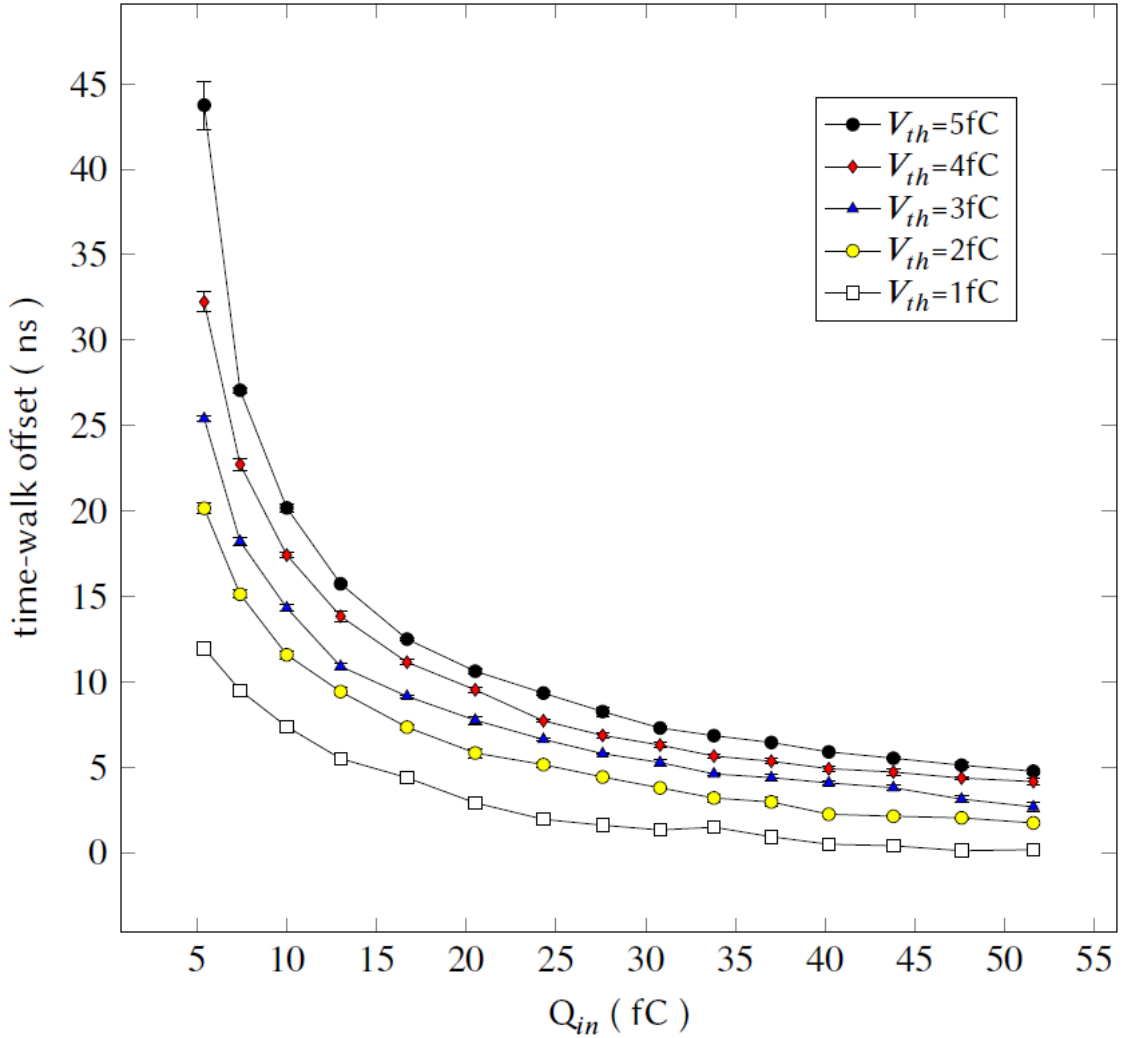




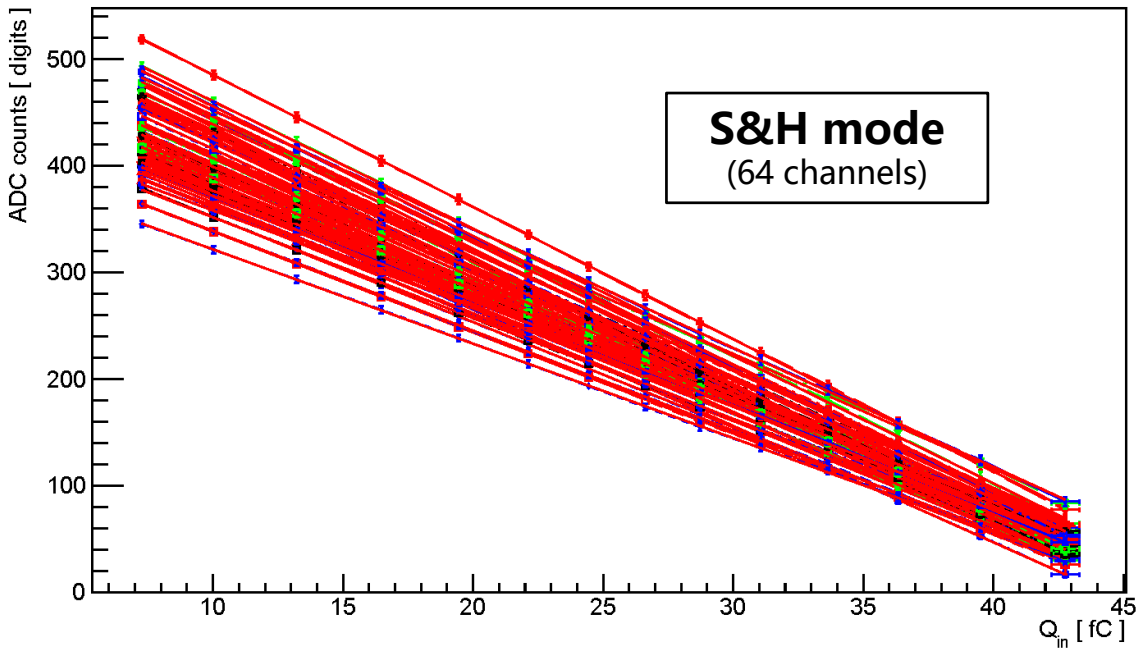
Charge measurement

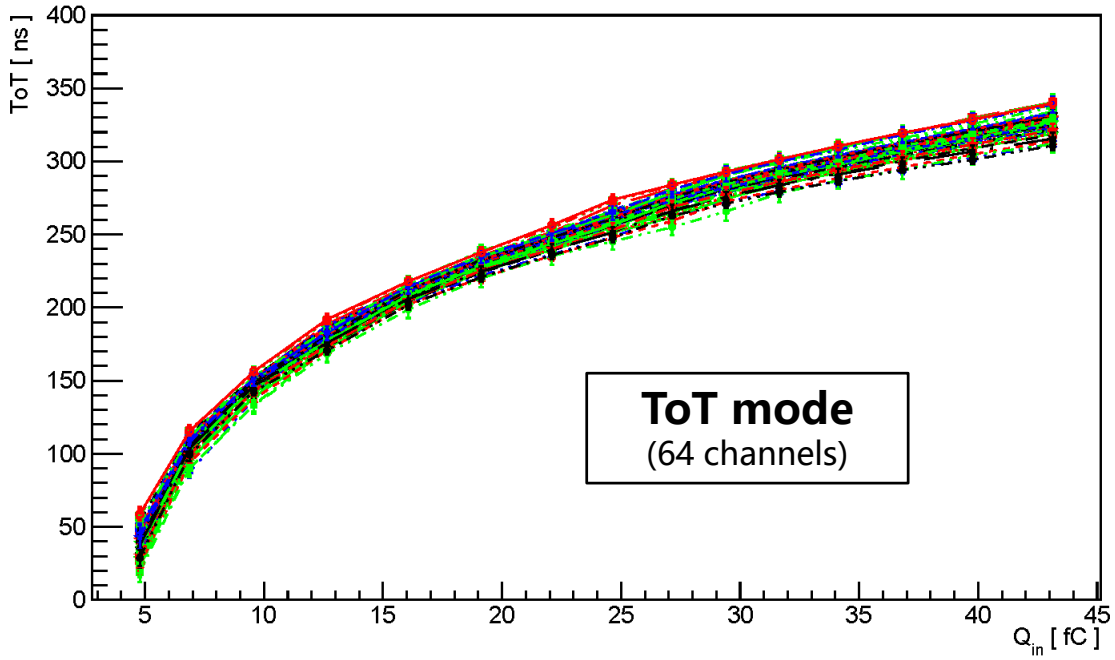
- S/H **dynamic range** and **linearity** with external test-pulse generator (ch. 63 input debug port)
- Back-annotation for **internal test pulse calibration** to assess all channels
- Charge information can be used to correct time offset due to **time-walk**





S&H vs ToT





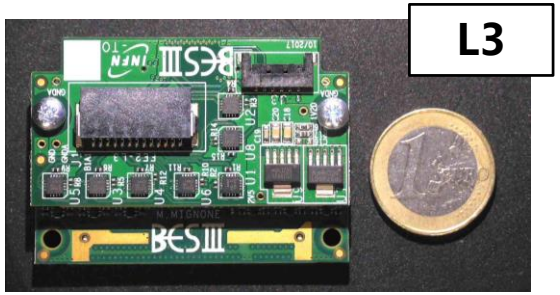
- **Linear response** from S&H circuit → easy to calibrate
- S&H affected by **saturation** (FE and ADC)
- ToT response intrinsically not linear due to shapers waveform
- ToT not affected by saturation → good backup solution

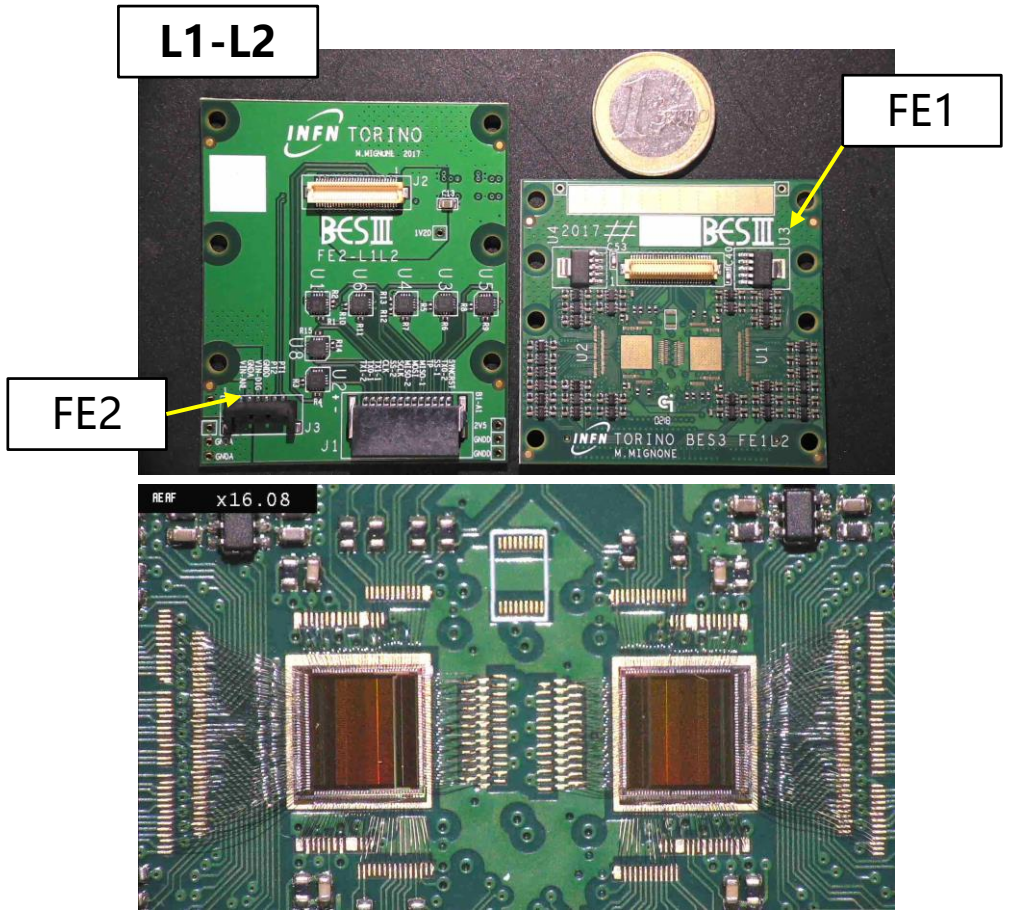
Tests with GEM detectors

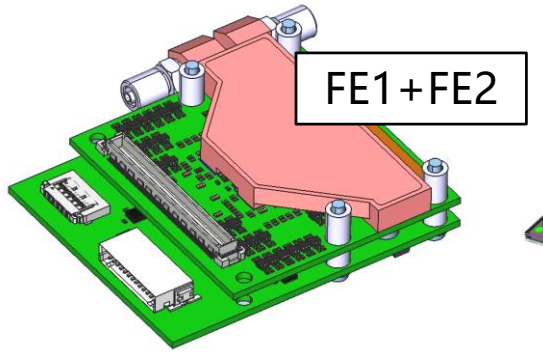
Front-End Board (FEB)

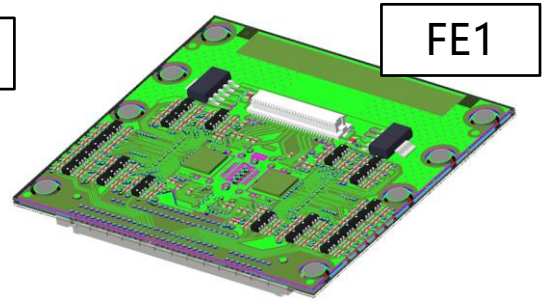
Front-End Board (FEB) to readout the CGEM detector

- Stack of two printed circuit boards:
  - FE1: analogue-most layer
  - FE2: digital layer
- 2 TIGER ASICs mounted on FE1 (128 channels per FEB)
- **Water-cooling heat exchanger plate** for operation at controlled temperature
- Different layout and routing for L3 FEBs due to space constraints inside BESIII

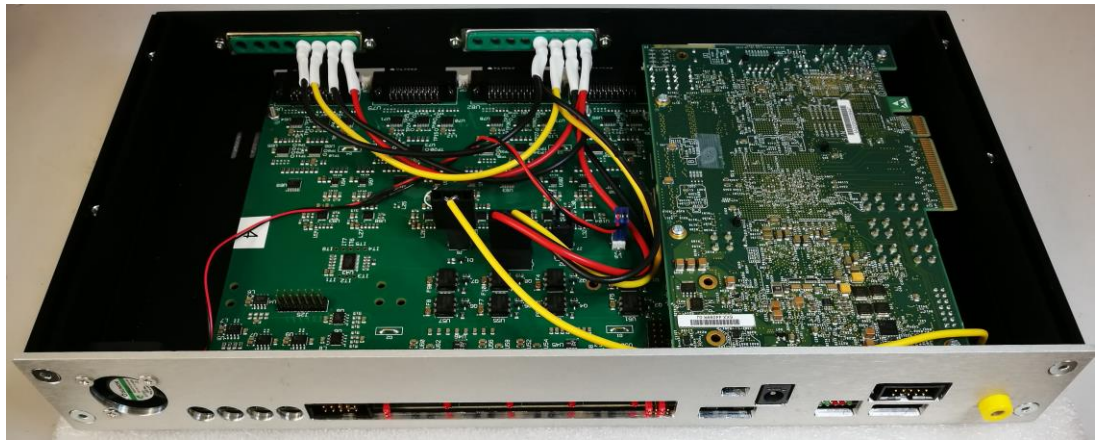




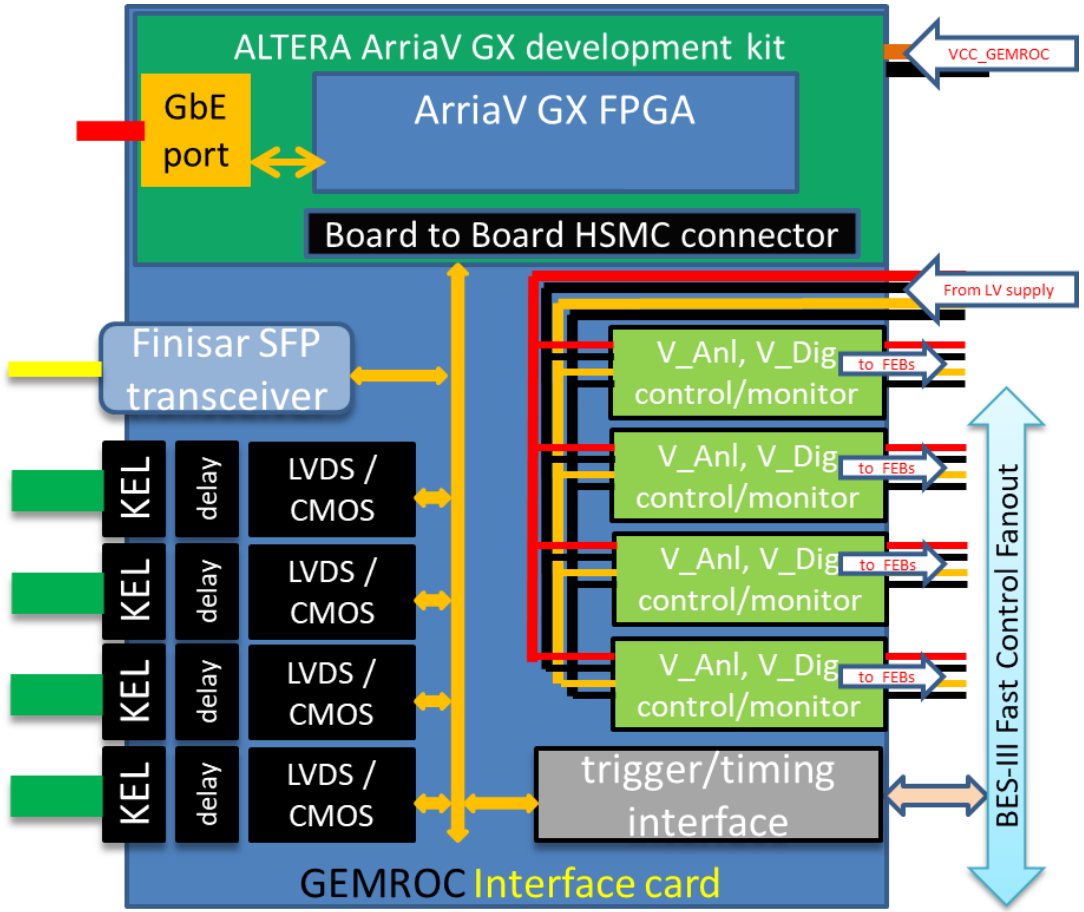




GEMROC (GEM ReadOut Card)

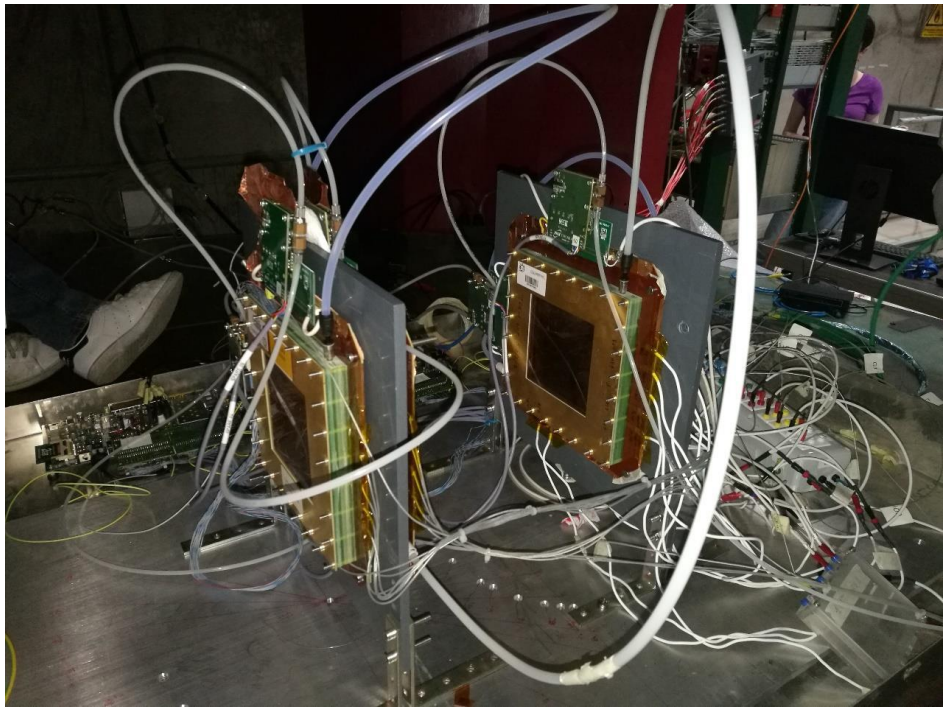


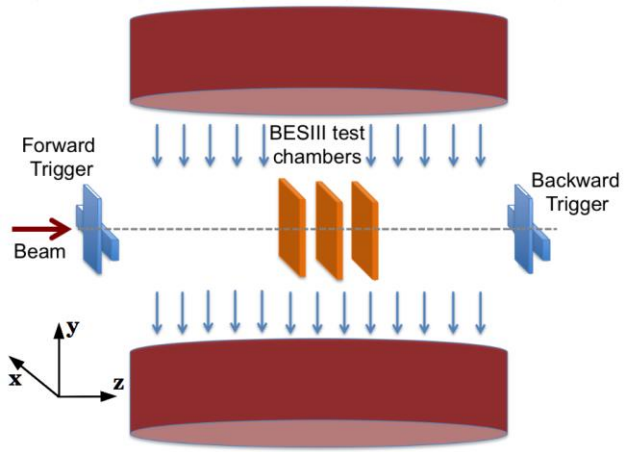
- Developed by INFN Ferrara
- Off-detector electronics for the readout of the CGEM-IT detector (160 TIGER)
- Provides power, configuration and data interface to the TIGER ASICs (up to 8 TIGER for each GEMROC)
- **Trigger-Matching** operations (trigger-less mode also available)



Beam tests with planar GEMs

- 2 beam tests to validate the ASIC with the sensor:
  - 10 x 10 cm^2 planar GEMs
  - XY orthogonal strips
  - Turin FPGA-based DAQ -> readout of 8 TIGER
- Nov 2017: Mainz Microtron (TIGER prototype version)
- Apr 2018: CERN H4 beam line (TIGER final version)

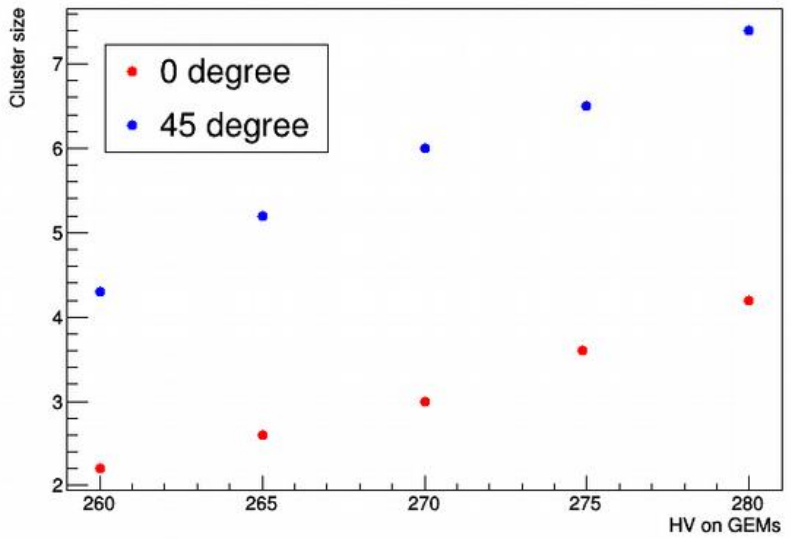




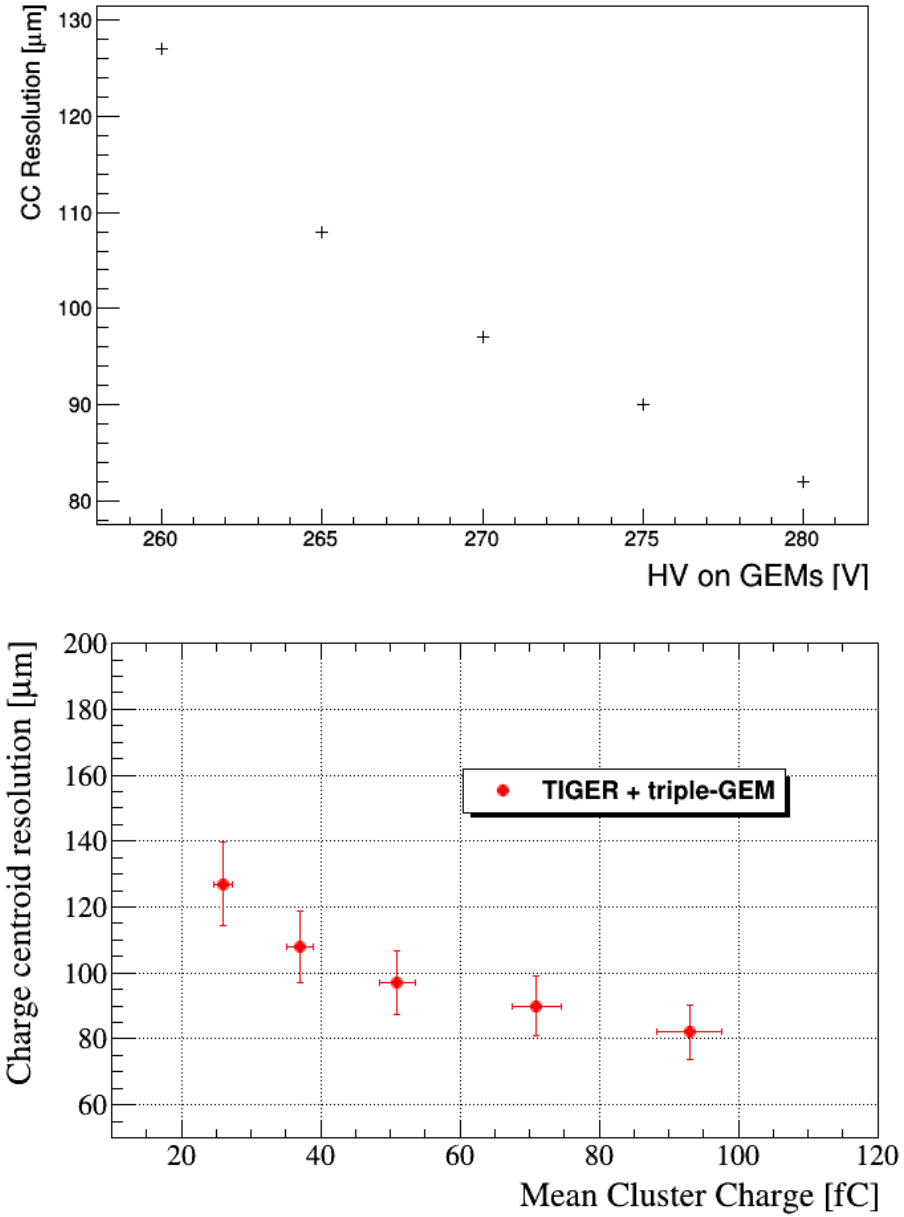
Trigger-less readout: trigger from scintillator bars injected as a digital test-pulse on one TIGER channel to be used as a reference for offline trigger-matching

CERN test beam results

Event clusterization



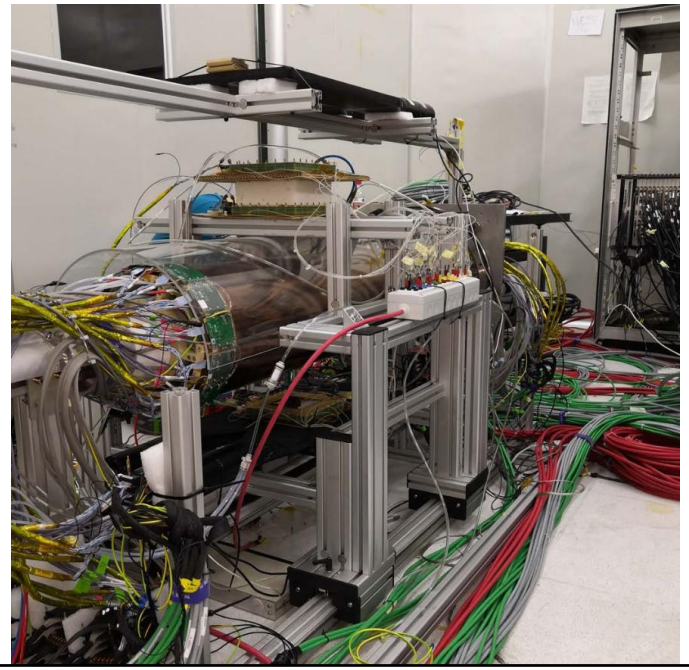
CC resolution

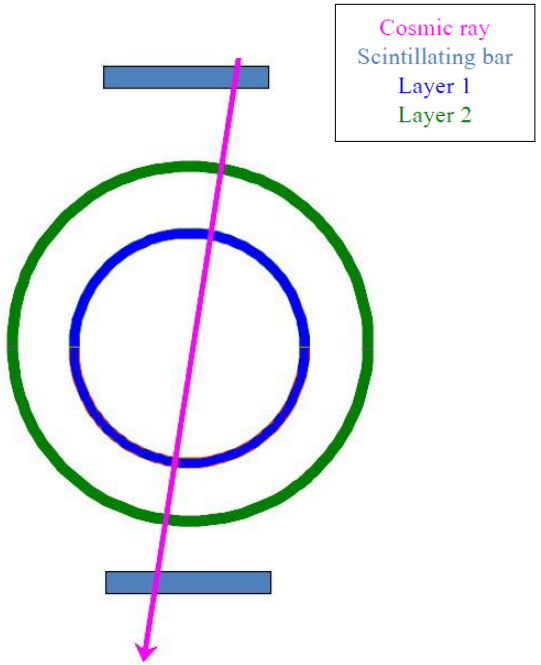


CGEM-IT tests

Two out of three layers of the CGEM-IT detector are assembled together and **cosmic rays** acquisitions are now ongoing at IHEP (Beijing, China)

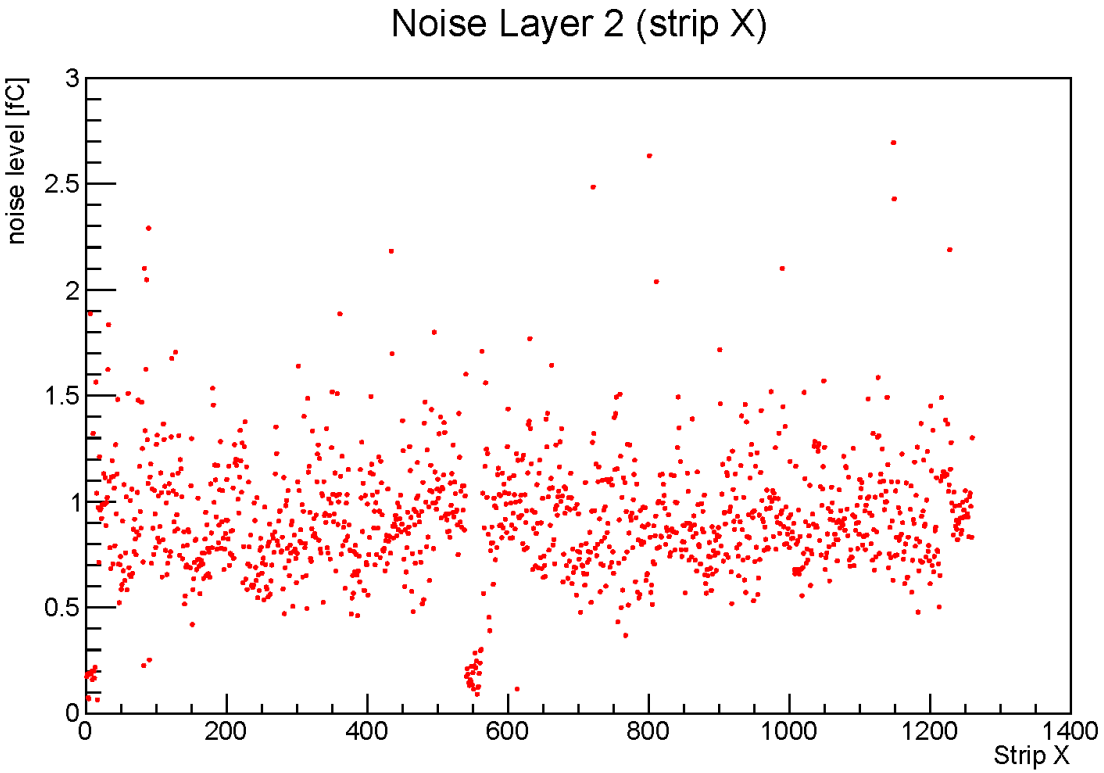
- 88 TIGER ASICs readout by 11 GEMROC modules (>5000 electronics channels instrumented)
- GUFI (Graphical User Front-end Interface) software provides DAQ control tools for:
  - **Trigger-matched** cosmic acquisition
  - **Trigger-less** operation for periodic maintenance

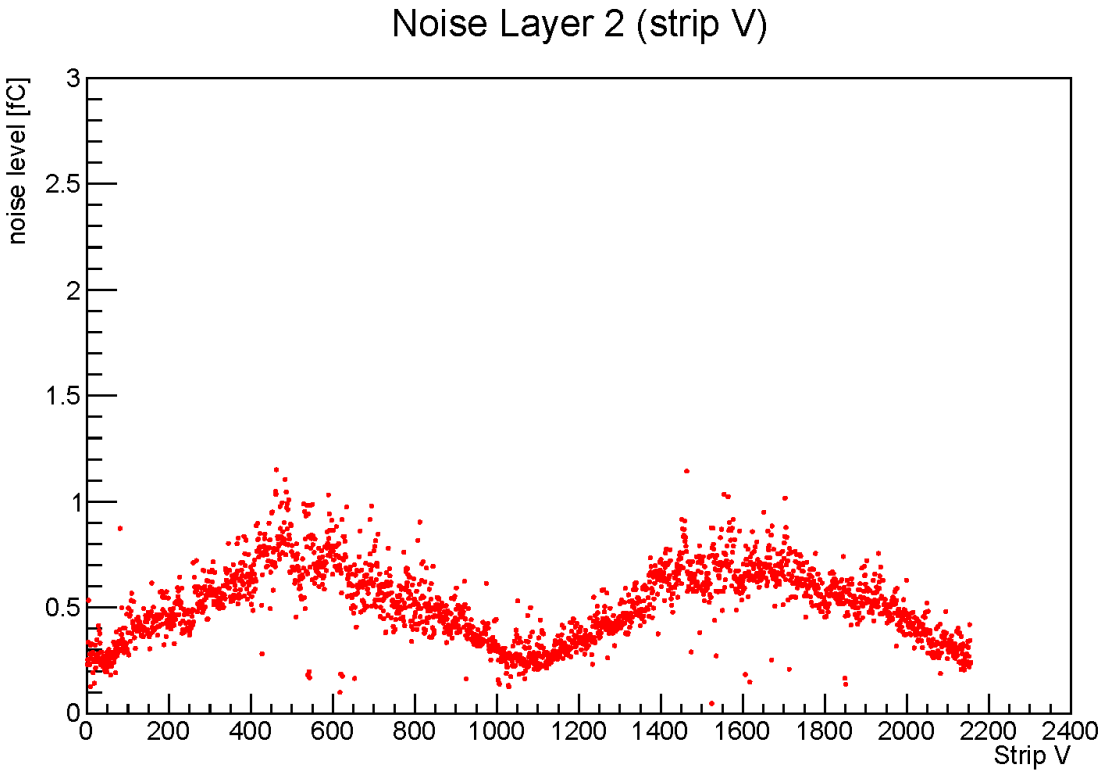




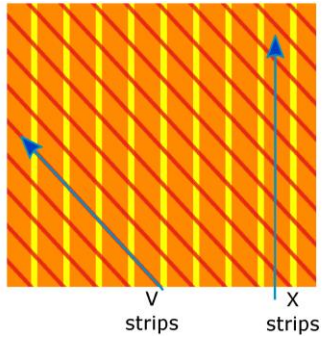
R. Farinelli, *"Preliminary results from the cosmic data taking of the BESIII cylindrical GEM detectors"* , talk at INSTR-20, Novosibirsk, Russia

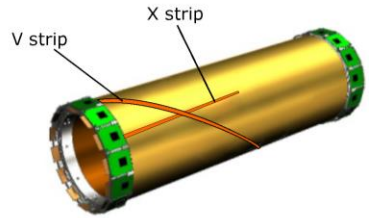
On-detector noise measurements



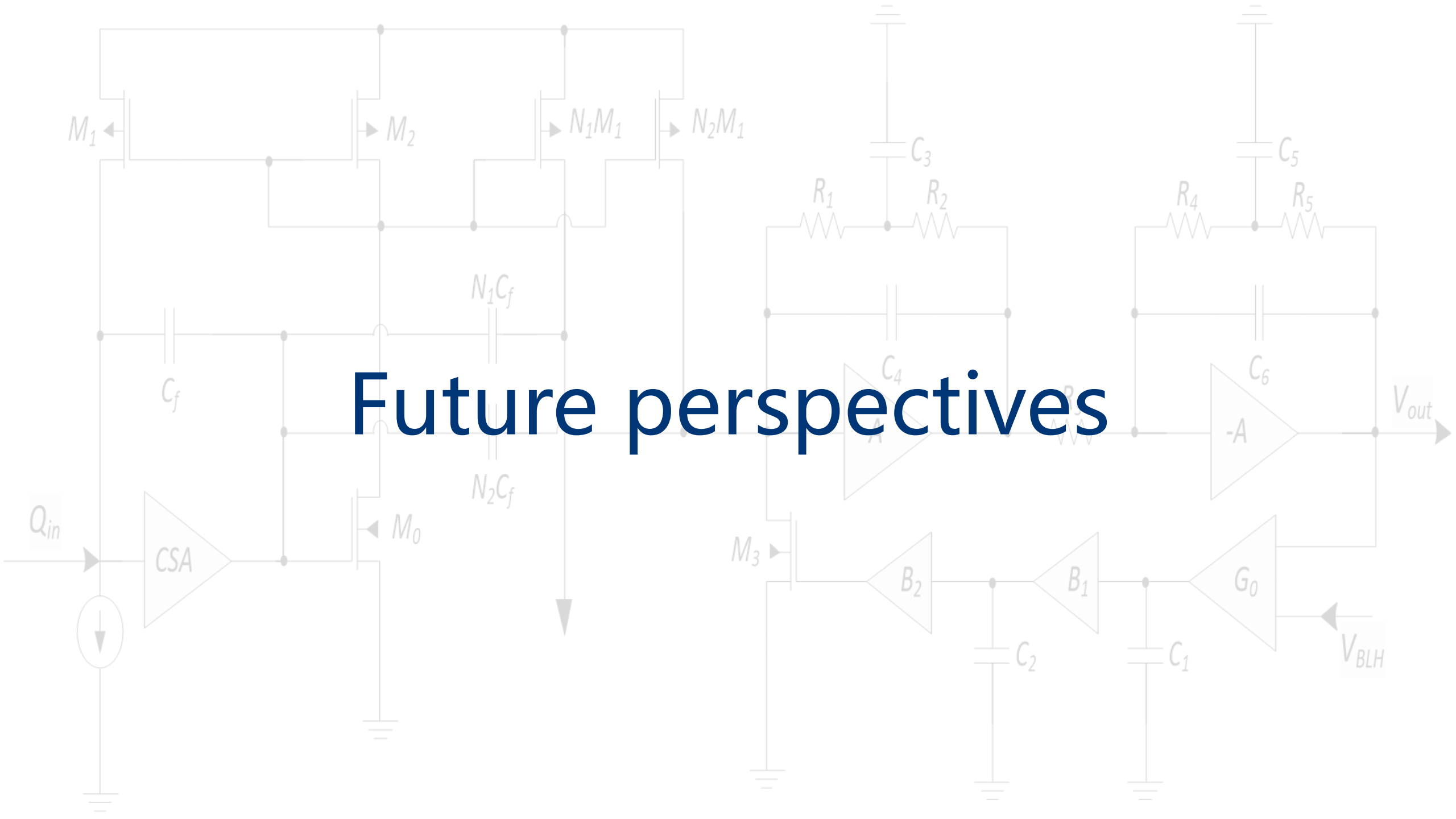


- Almost flat distribution for **X-strips**
- **V-strips** noise follows the strips length



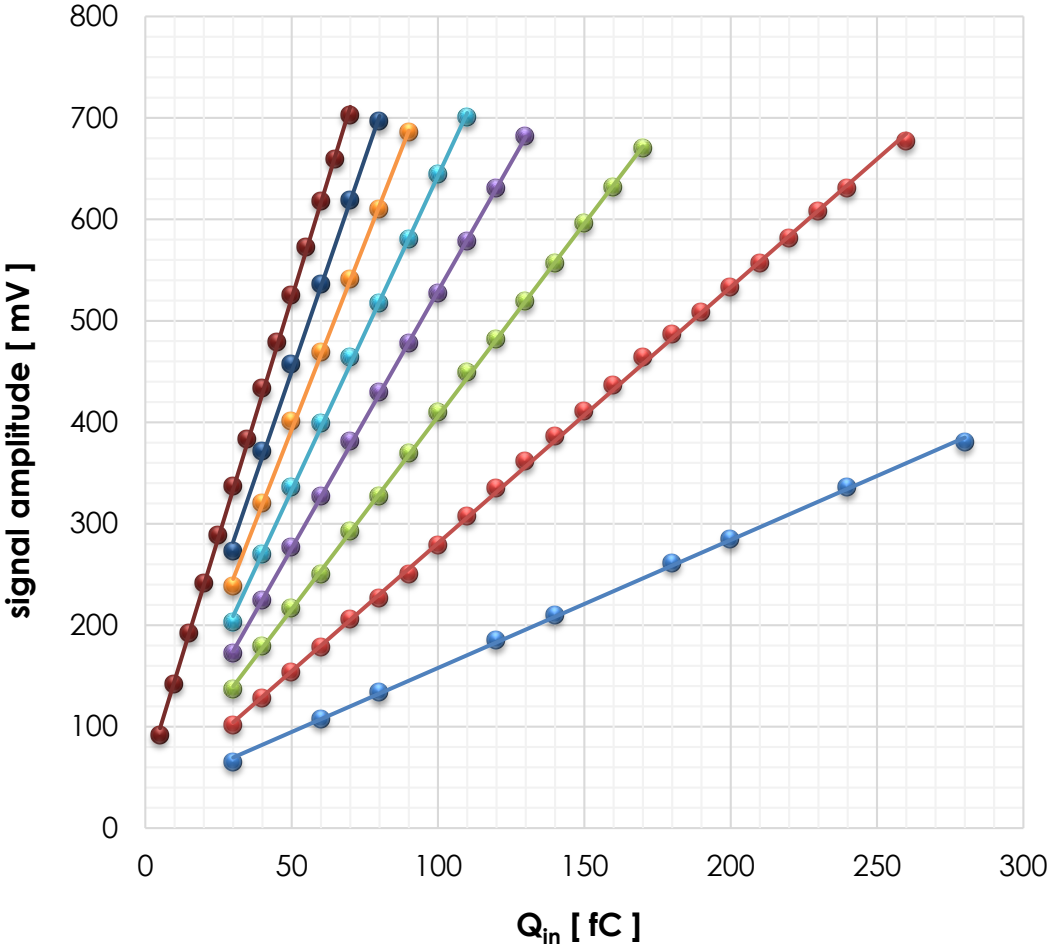


Future perspectives



TIGER alt. version

- **TIGER V**ersatile **D**igitizer
  - Alternative FE design, shared engineering run
  - Versatile front-end, can be used for readout of GEM or other sensors
- **RGC** (common-gate with gm-boosting) **input-stage**
  - Current-mode amplification
  - Low configurable input impedance
  - Programmable gain: 3-bit DAC, range 50-300 fC Input



Cheng, W. et al. *"A mixed-signal large dynamic range front-end ASIC for high capacitance detectors"*, JINST 14.08 (2019): P08013

TIGER new versions

- **ASICs for Si-Strip readout:** TIGER architecture as a baseline for a 1st prototype Si-strip readout chip:
  1. PANDA MVD strip detector
     - Configurable for both input signal polarities
     - Time of Arrival measurement with system clock resolution
     - Charge measurement via Time-over-Threshold
  2. Dedicated low-noise low-power VFE compatible with space applications

Summary and outlook

- TIGER was developed for the **readout of the CGEM-IT** detector
- The ASIC has been found **fully functional** at the second iteration on silicon:
  - time-based readout working properly
  - charge measurement good linearity with S&H circuit
- Two **beam tests** have validated the ASIC with the sensor
- In situ **commissioning of fully instrumented BESIII CGEM-IT** is now ongoing
- TIGER **versatile back-end** can be re-used for new readout chips
- **New applications and versions** of TIGER under development

References

- F. Cossio et al., *"Design and performance of the TIGER front-end ASIC for the BESIII Cylindrical Gas Electron Multiplier detector"* , Proceedings of the 2017 IEEE Nuclear Science Symposium and Medical Imaging Conference, Atlanta, Georgia, US (NSS/MIC 2017)
- M. D. Da Rocha Rolo et al., *"A custom readout electronics for the BESIII CGEM detector"* , Journal of Instrumentation, Volume 12, Issue 07, pp. C07017 (2017)
- A. Rivetti et al., *"TIGER: A front-end ASIC for timing and energy measurements with radiation detectors"* , Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 924 (2019)
- F. Cossio, *"A mixed-signal ASIC for time and charge measurements with GEM detectors"* , PhD thesis, Turin Polytechnic, 2019
- Cheng, W. et al. *"A mixed-signal large dynamic range front-end ASIC for high capacitance detectors"* , JINST 14.08 (2019): P08013

Thank you!

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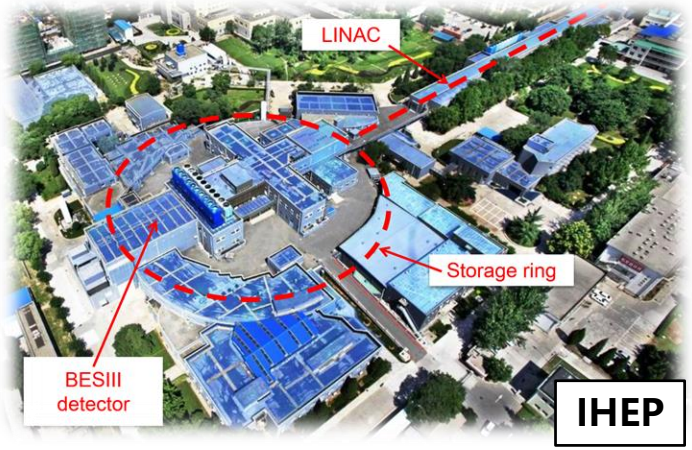
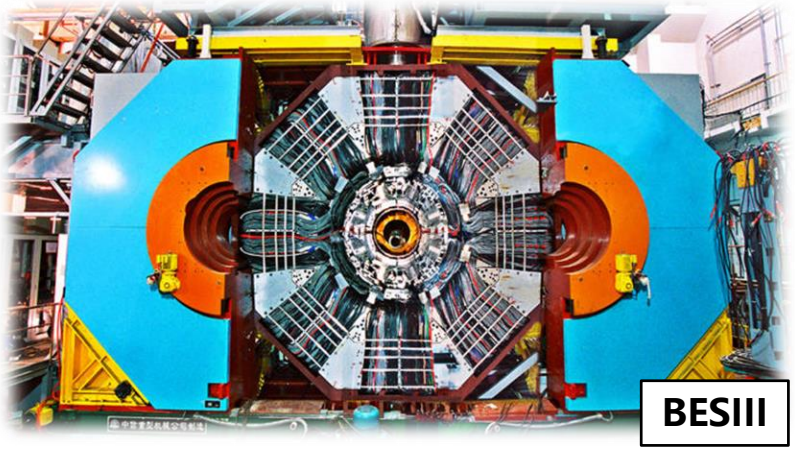
The BESIIICGEM project has been funded by European Commission within the calls H2020-MSCA-RISE-2014 and FEST RISE-MSCA-H2020-2020

BACKUP SLIDES

The BESIII Experiment



IHEP

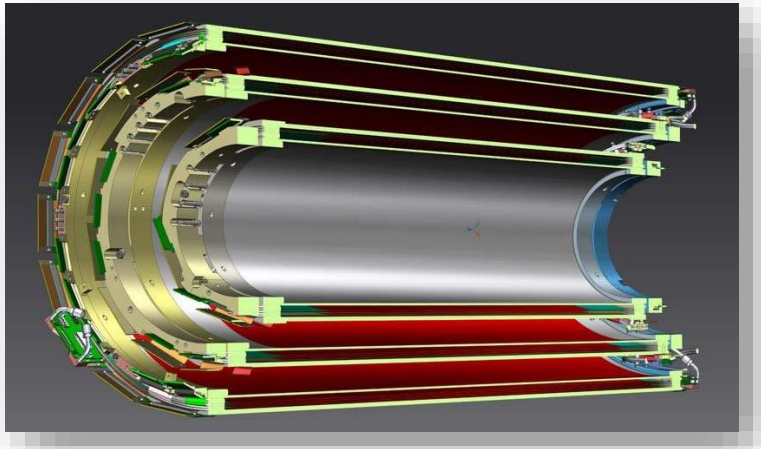

BESIII

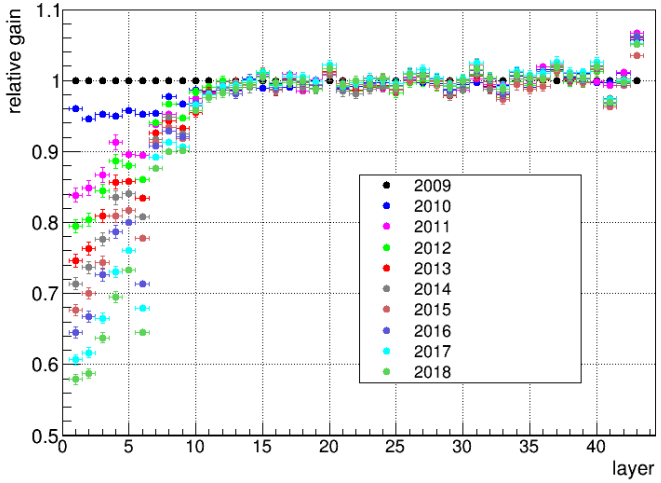
- Running since 2009 at **BEPC-II** (Beijing e^+e^- collider, IHEP)
  - τ-charm factory (E_{cm} = 2 – 4.6 GeV)
  - Broad physics program: charm, charmonium and exotic states spectroscopy, light hadrons, tau physics
- 2016: **luminosity increased to** $1 \cdot 10^{33}$ $cm^{-2}s^{-1}$

Feb 2019: BESIII accumulated a sample of **10 billion J/ψ events** (largest data sample produced directly from e^+e^- annihilations)

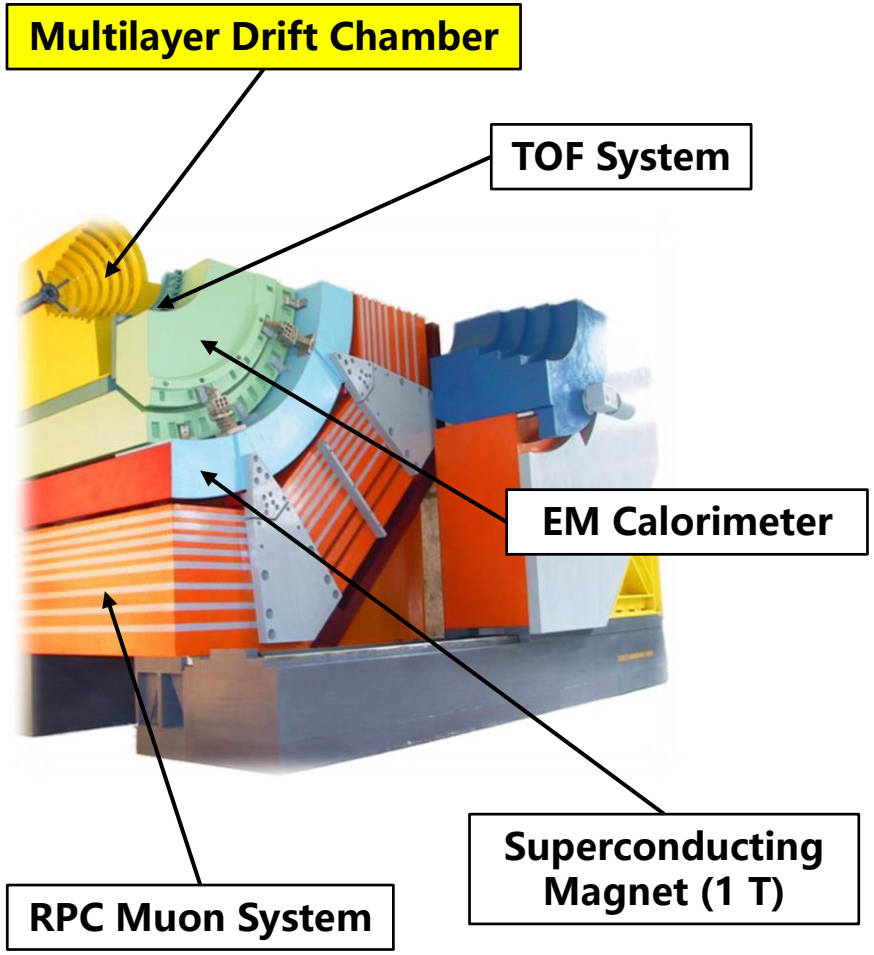
The CGEM-IT upgrade

New inner tracker: 3 layers of **Cylindrical Gas Electron Multiplier** detector to replace the 8 innermost layers of the MDC (summer 2021)



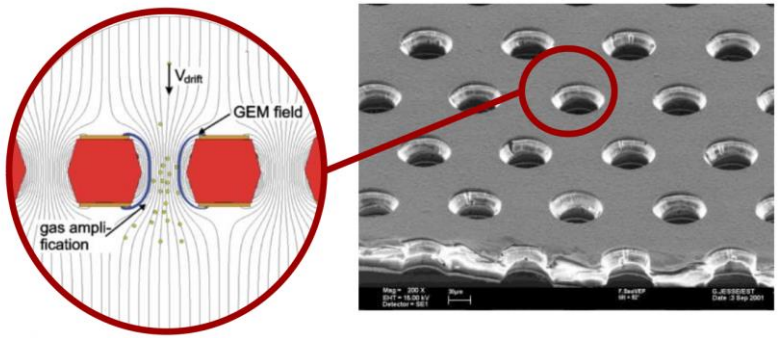


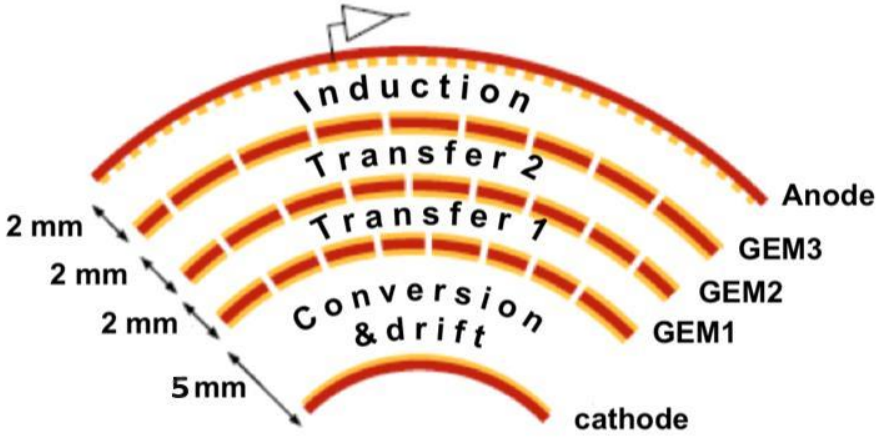
- **MDC** inner layers **aging** due to radiation damage: gain loss ~ 4% per year
- CGEM-IT features: **low material budget** (X_0 < 1.5%), good **radiation tolerance** and **high rate capability** (10 kHz/cm^2)

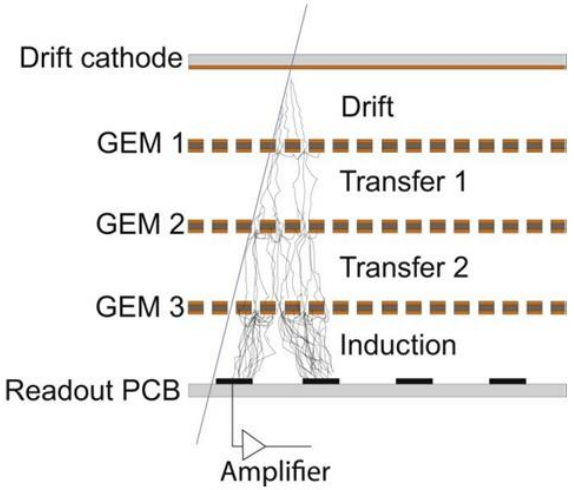


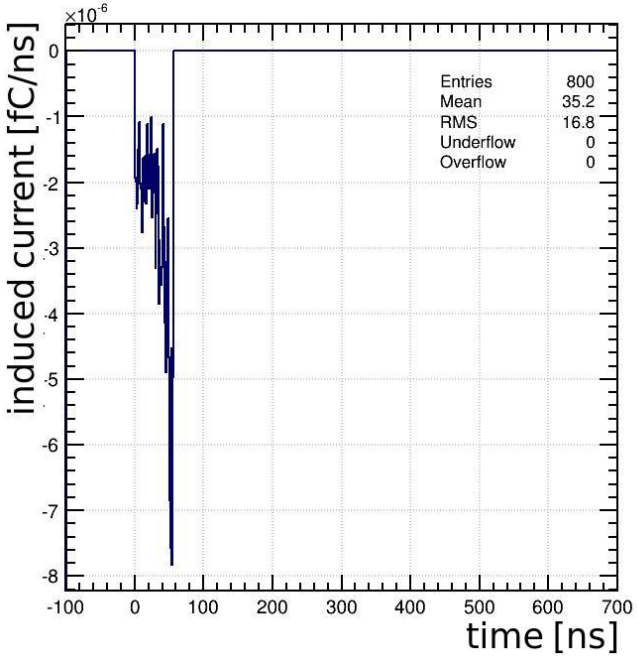
Gas Electron Multiplier

- Thin Kapton foil (50 μm), copper-clad on both sides (3-5 μm), with high density of holes (diameter = 50 μm)
- Voltage gradient between the two electrodes (hundreds of Volts) → electric field (tens of kV/cm) inside the holes: electrons released on the top side drift into the hole and multiply in avalanche
- Charge collected at the anode by 2D segmented readout strips
- Cascaded GEMs allow larger gains (10^4 - 10^5) and low discharge probability









CGEM-IT Project

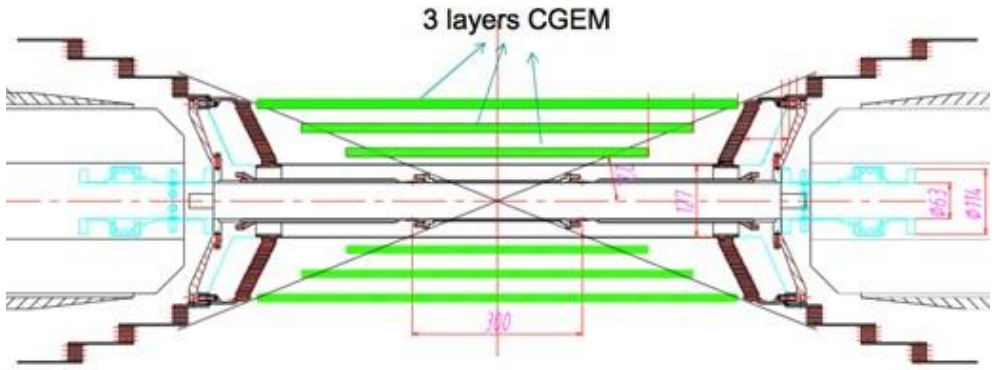
Institute of High Energy Physics
Chinese Academy of Sciences

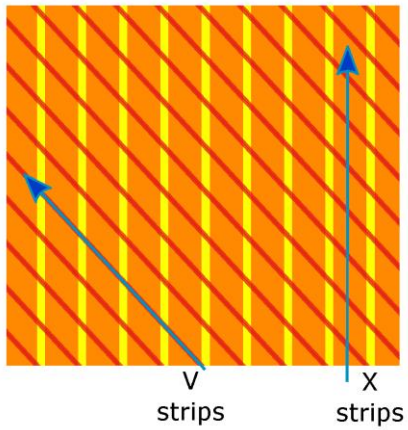
JOHANNES GUTENBERG UNIVERSITÄT MAINZ

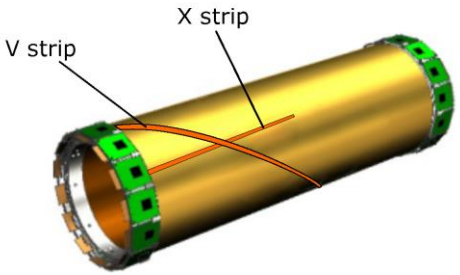
UPPSALA UNIVERSITET

INFN
Istituto Nazionale di Fisica Nucleare

- European Community funded the CGEM-RISE project (proposed by INFN together with JGU-Mainz, Uppsala and IHEP).
- Angular coverage: 93%
- Low material budget: X_0 < 1.5%
- High rate capability: 10^4 Hz/cm^2
- Segmented anode readout plane: X and stereo V strips (ϕ and z coordinates)
- Measurements with triple GEM in magnetic field & with analogue readout with charge and time information
- Momentum resolution 0.5% @1 GeV/c, r-ϕ spatial resolution 130 μm, z resolution 1 mm, better secondary vertices reconstruction



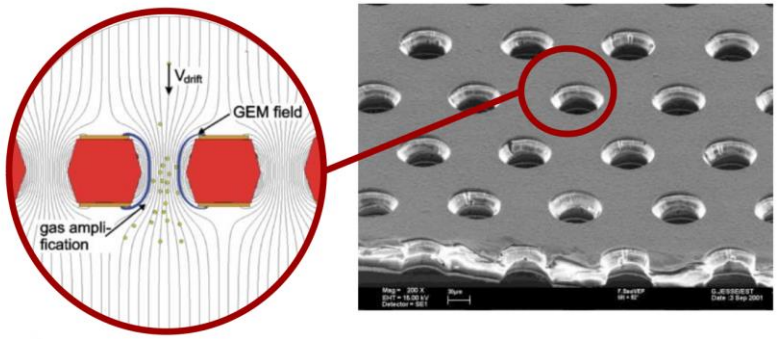




CGEM readout

TIGER has been designed for the readout of the **CGEM-IT**

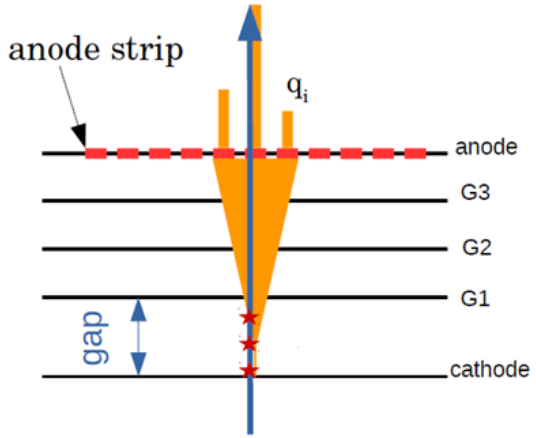
- new inner tracker of BESIII Experiment (summer 2021)
- 3 layers of **Cylindrical Gas Electron Multiplier** detector



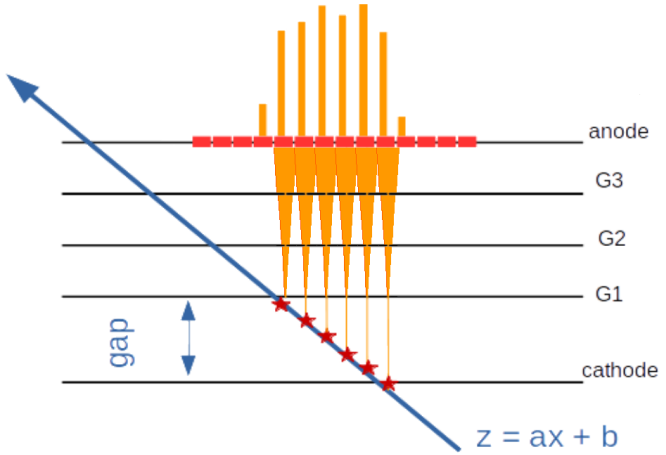
ANALOGUE READOUT

- **Charge centroid** and **µ-TPC** algorithms
- 130 µm spatial resolution with strip pitch of 650 µm
- Total number of channels reduced to ~ 10 000 (*vs* 25 000 of binary readout)
- Apply threshold on collected charge to cut noise-induced events

Charge centroid



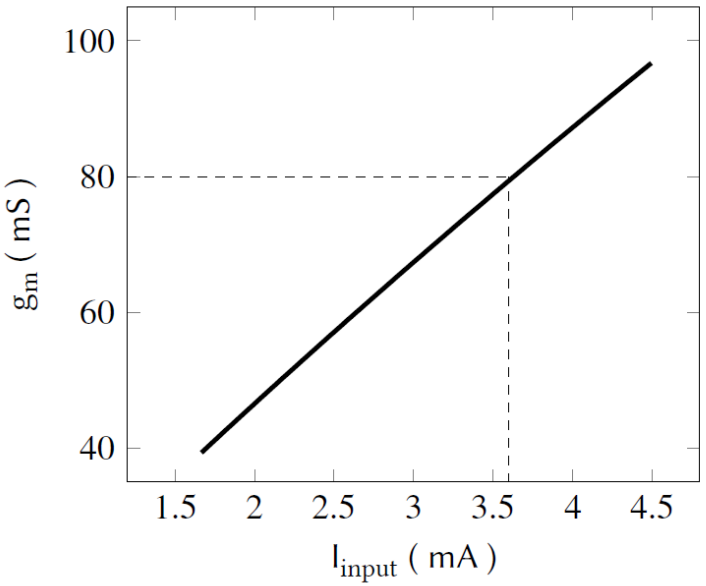
µTPC

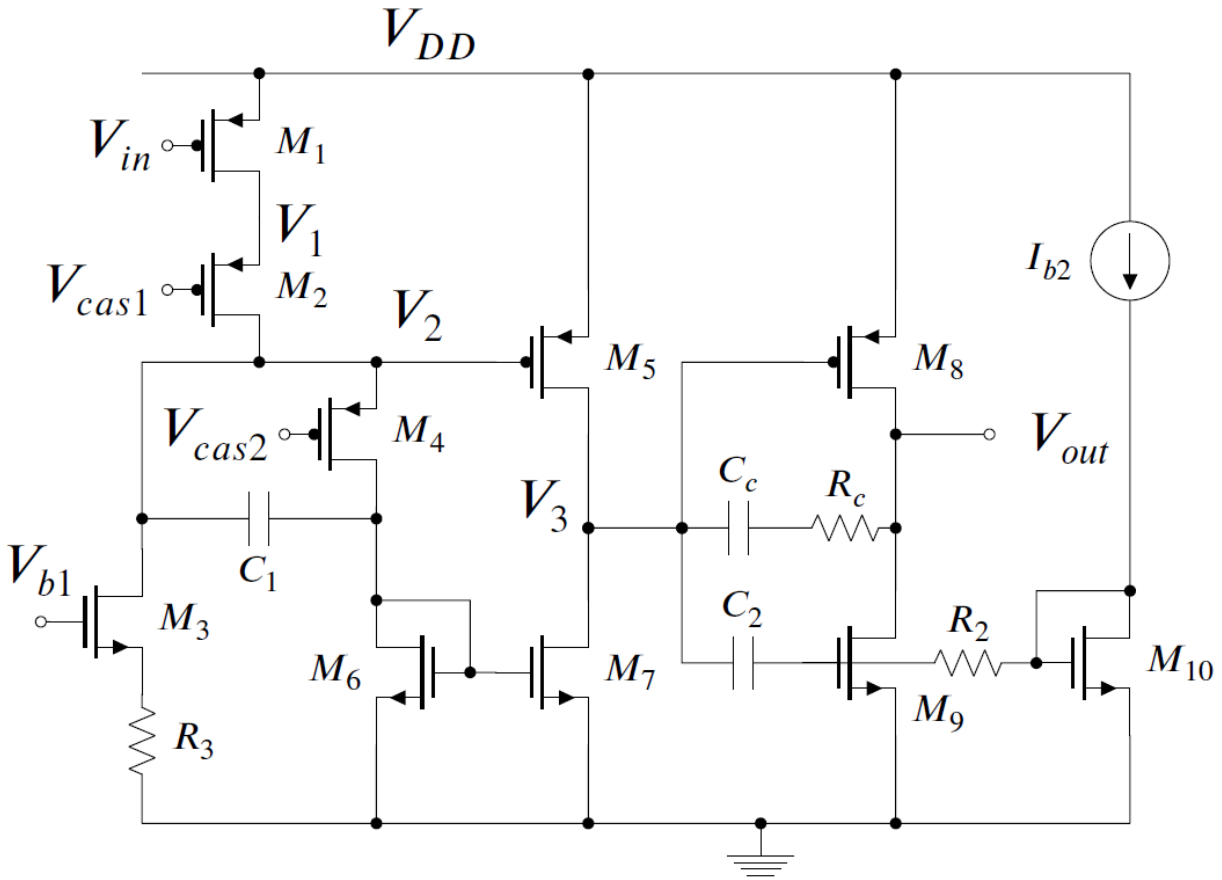


Triple-GEM for larger gains (10^4 - 10^5) and low discharge probability

FrontEnd – CSA core amplifier

- ENC target < 2000 e^- @ C_{in} = 100 pF
- Q_{in} = 2 - 50 fC
- 6-bit DAC to set the input transistor bias current





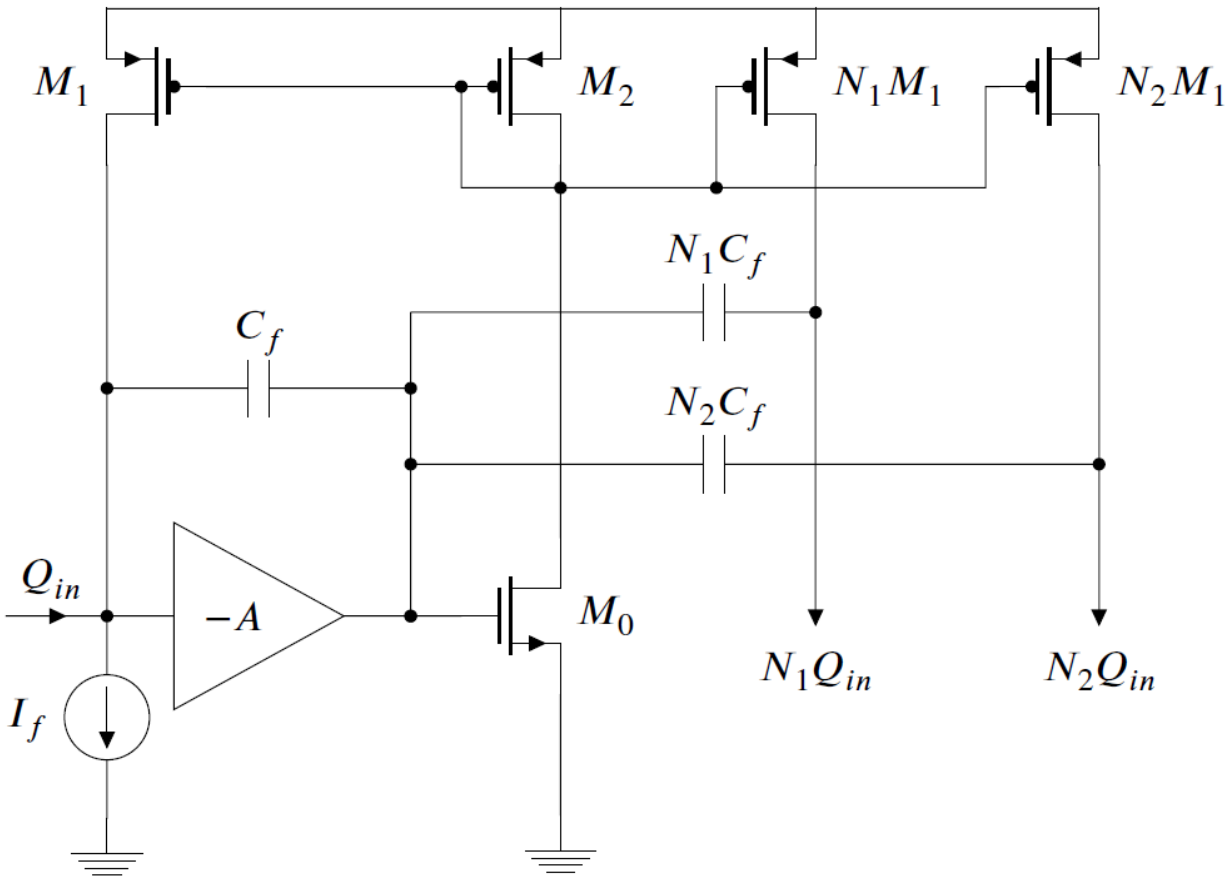
g_{m1} ≈ 80 mS (3.6 mA bias current)

FrontEnd – CSA feedback network

- C_f = 150 fF provides a gain of 6.7 mV/fC
- Current-mirror feedback resistor

$$R_f = \frac{1}{g_{m0}} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \approx 10\ M\Omega$$

- CSA output amplified by a factor of N (N = 20) and split into two branches feeding the two shapers

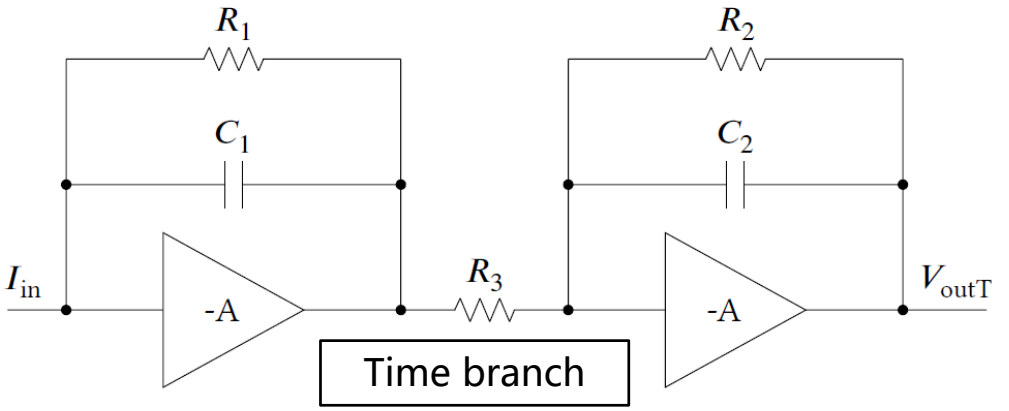


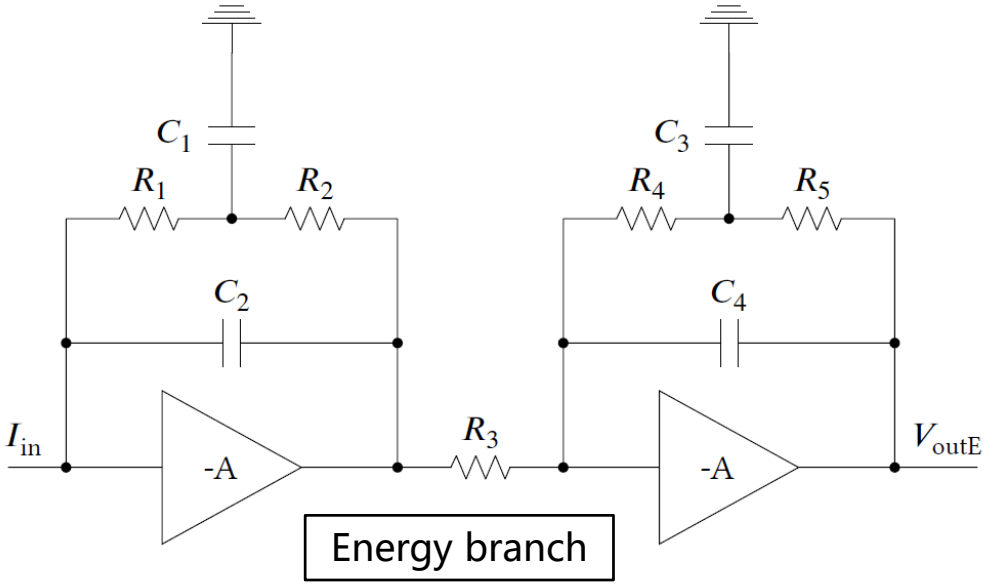
FrontEnd – shaper stage

1. **Time-branch**
   - Simple CR-RC shaper
   - 60 ns peaking time for low-jitter timing measurement

2. **Energy-branch**
   - 4 complex-conjugate poles shaper for a more gaussian signal shape to reduce pile-up probability
   - 170 ns peaking time for signal-to-noise ratio optimization

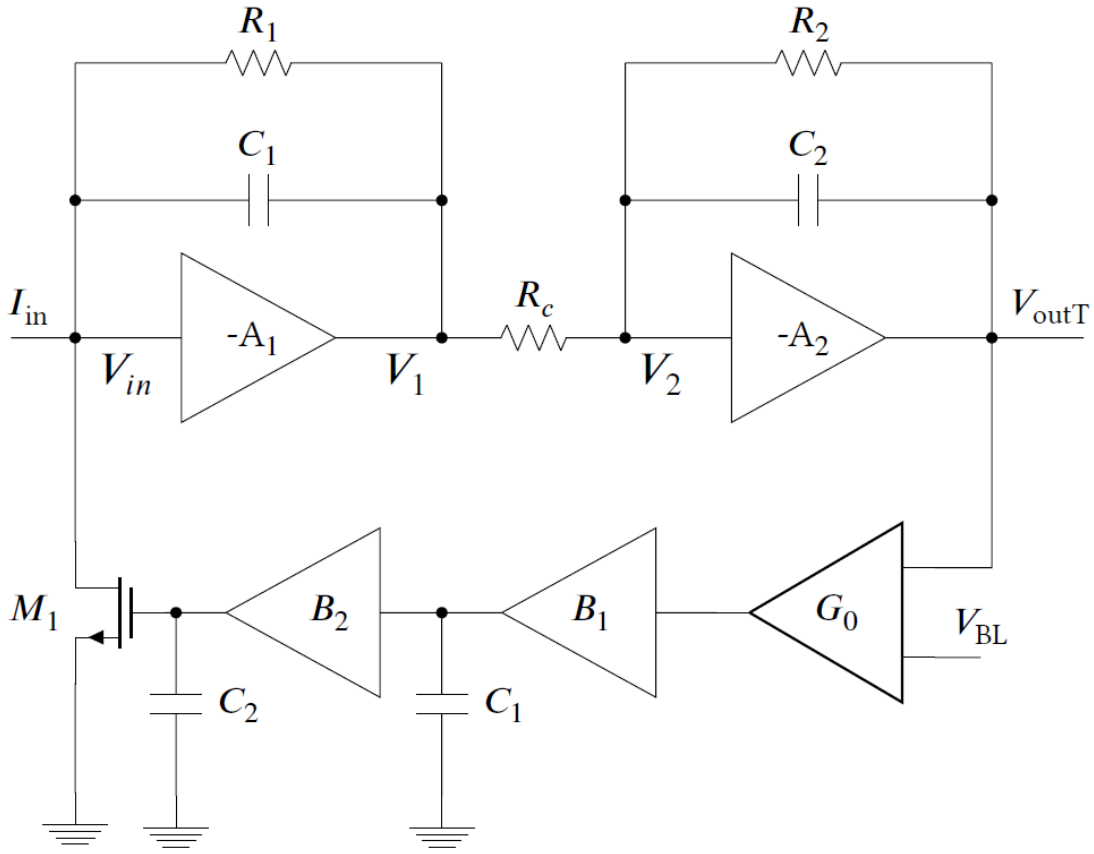
Shapers core amplifiers employ the same topology of CSA, but with reduced bias current (100 μA)



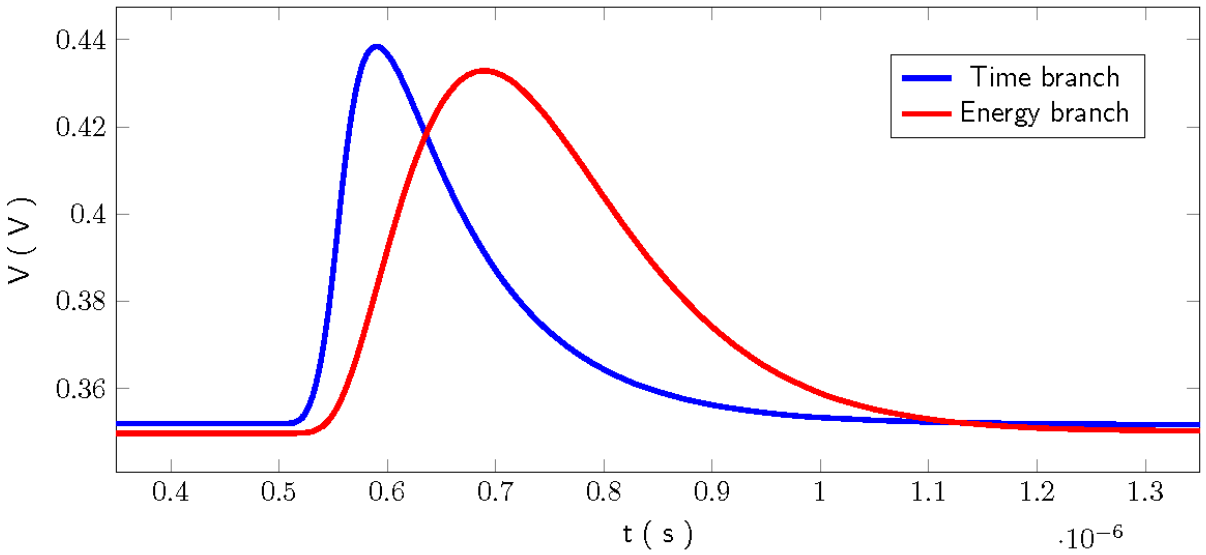


FrontEnd – baseline holder

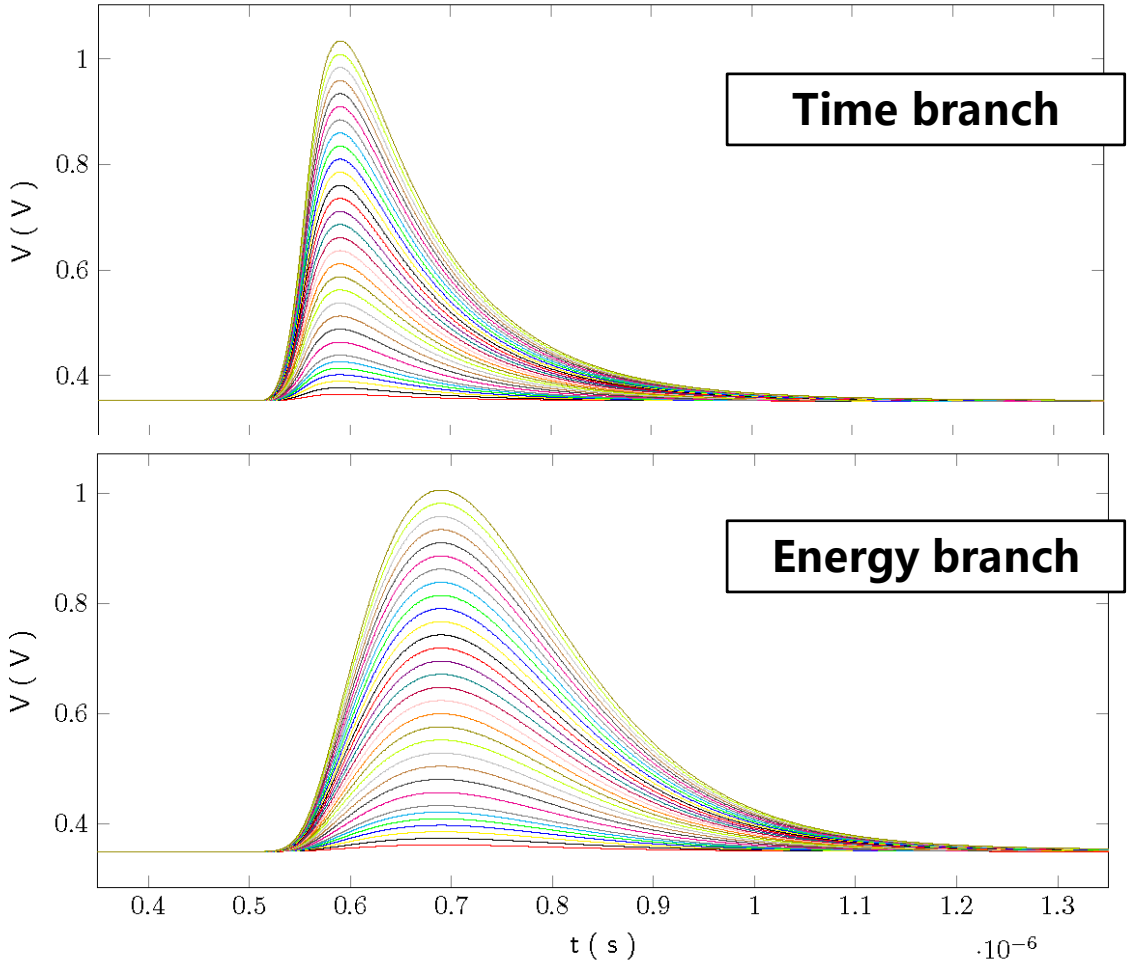
- **BLH** to lock the shapers output DC to an external reference value (V_{BL} = 350 mV)
- Current-starved buffers (B_1, B_2) and load capacitors (C_1, C_2) allow to affect only the DC component of shaper signal



Front-end simulations



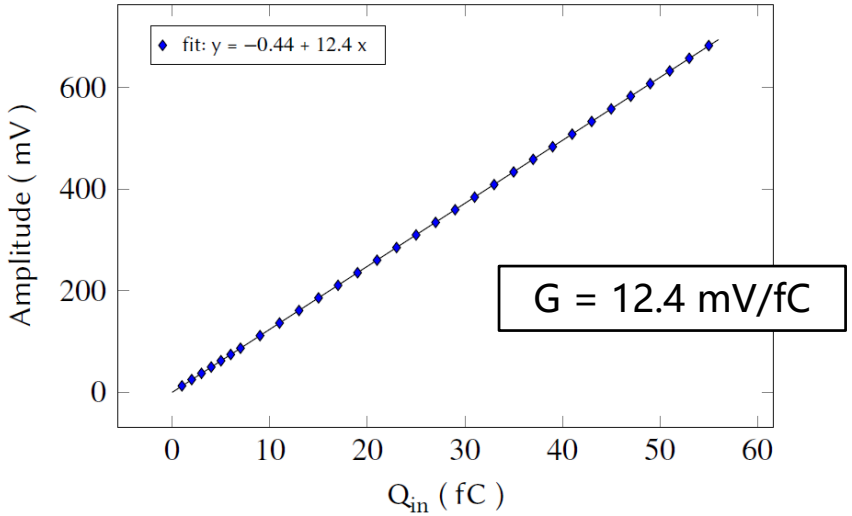
Front-end response to a 7 fC input signal

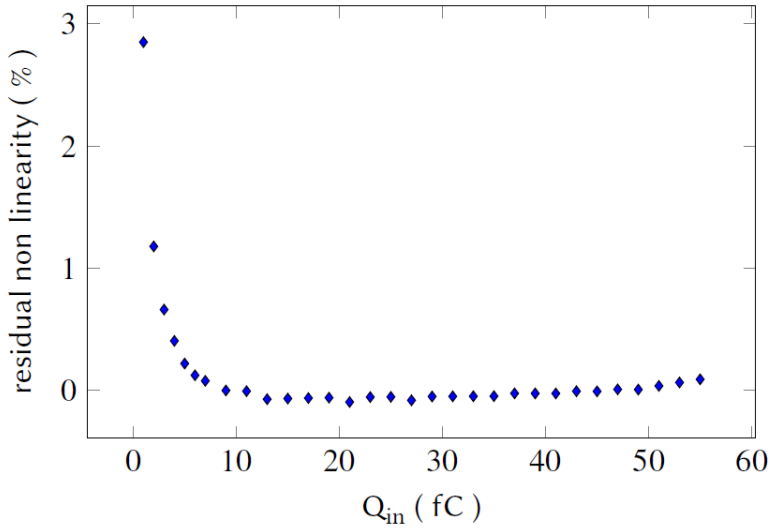


1-50 fC input signal sweep

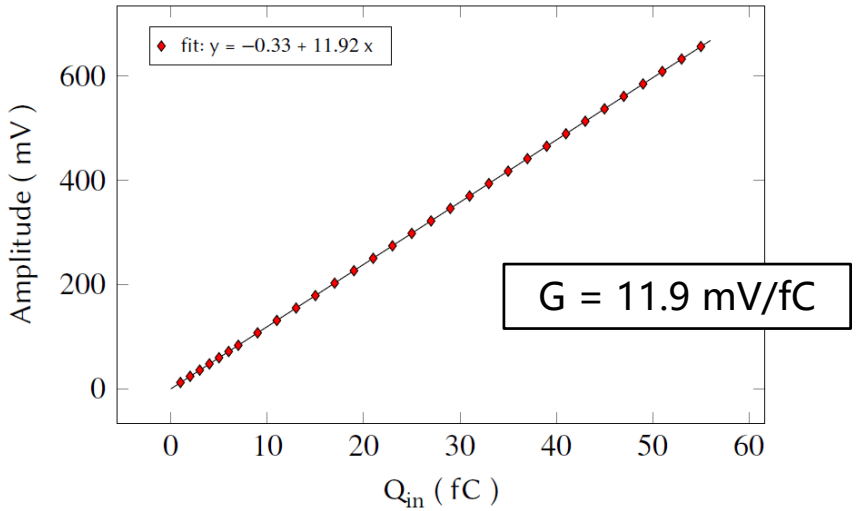
Front-end gain and linearity

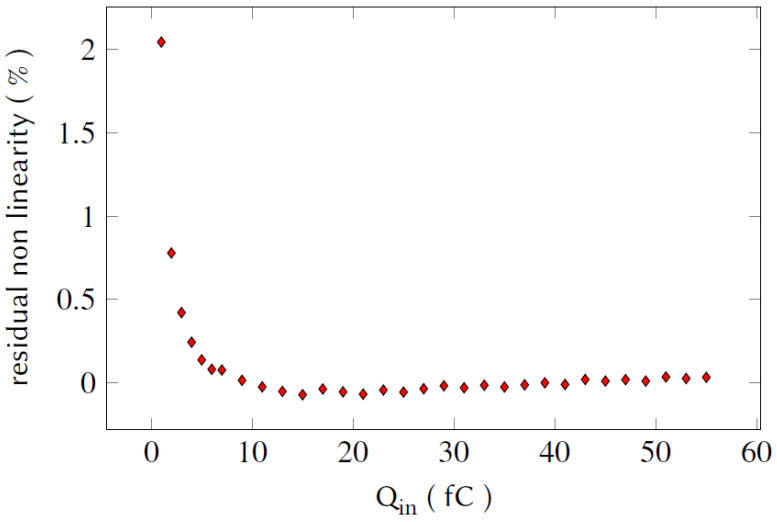
Time branch



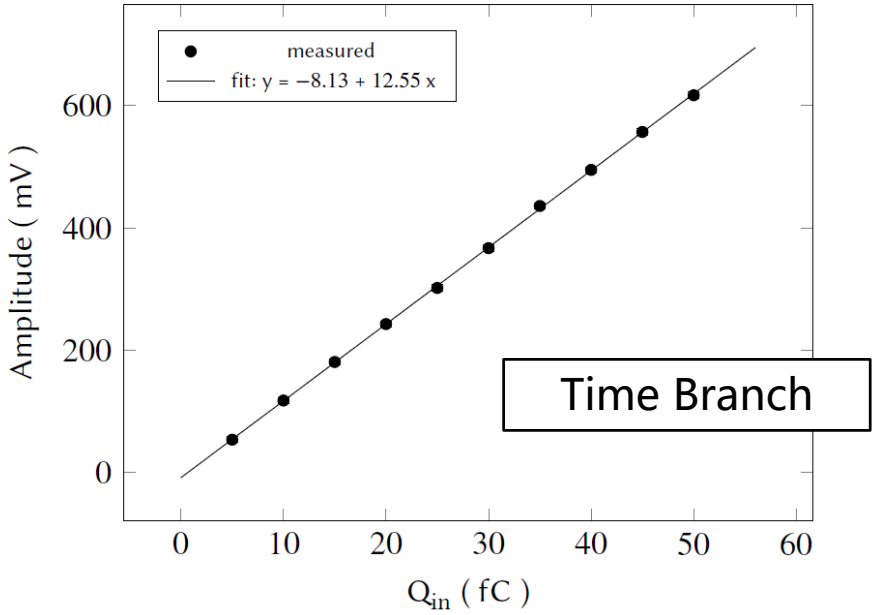


Energy branch

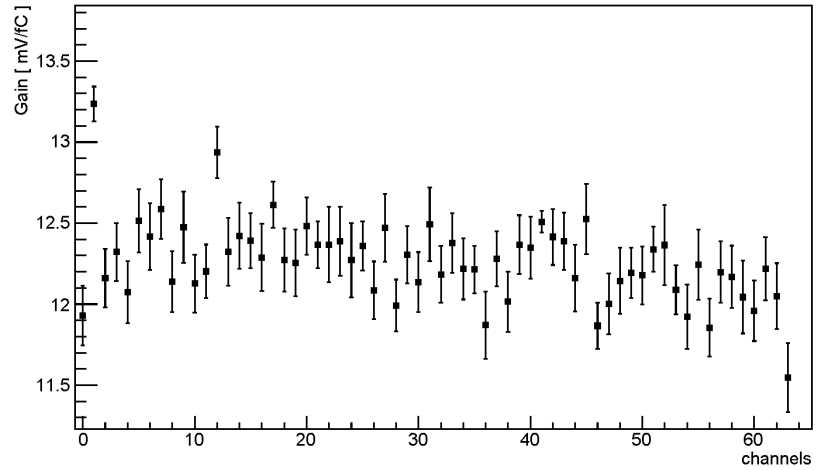


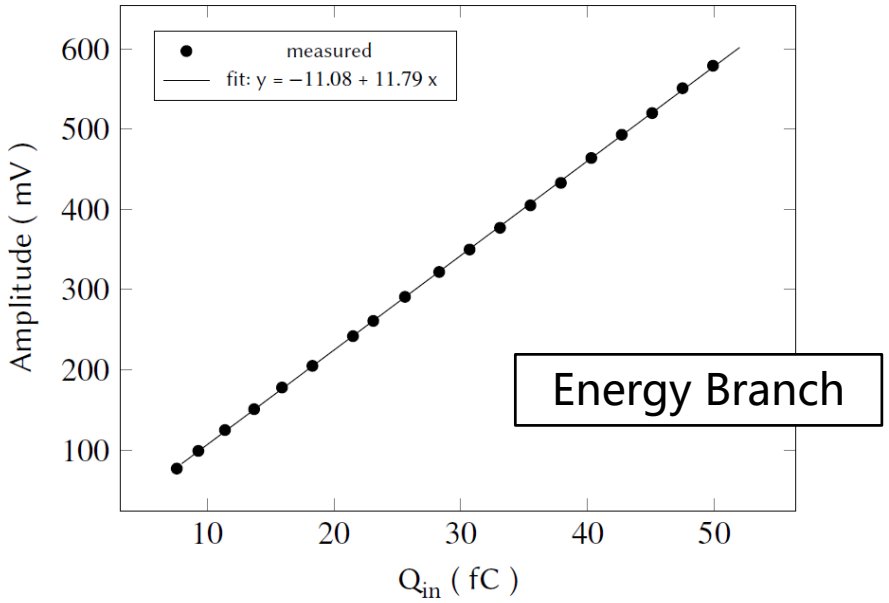


Gain dispersion

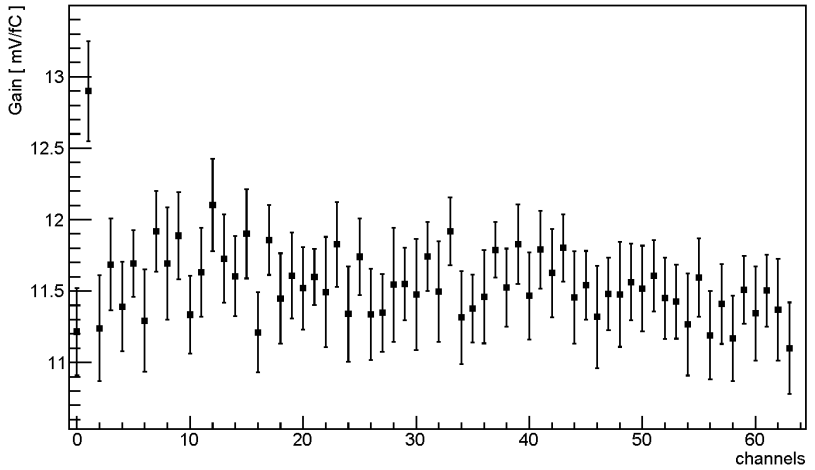


Time Branch



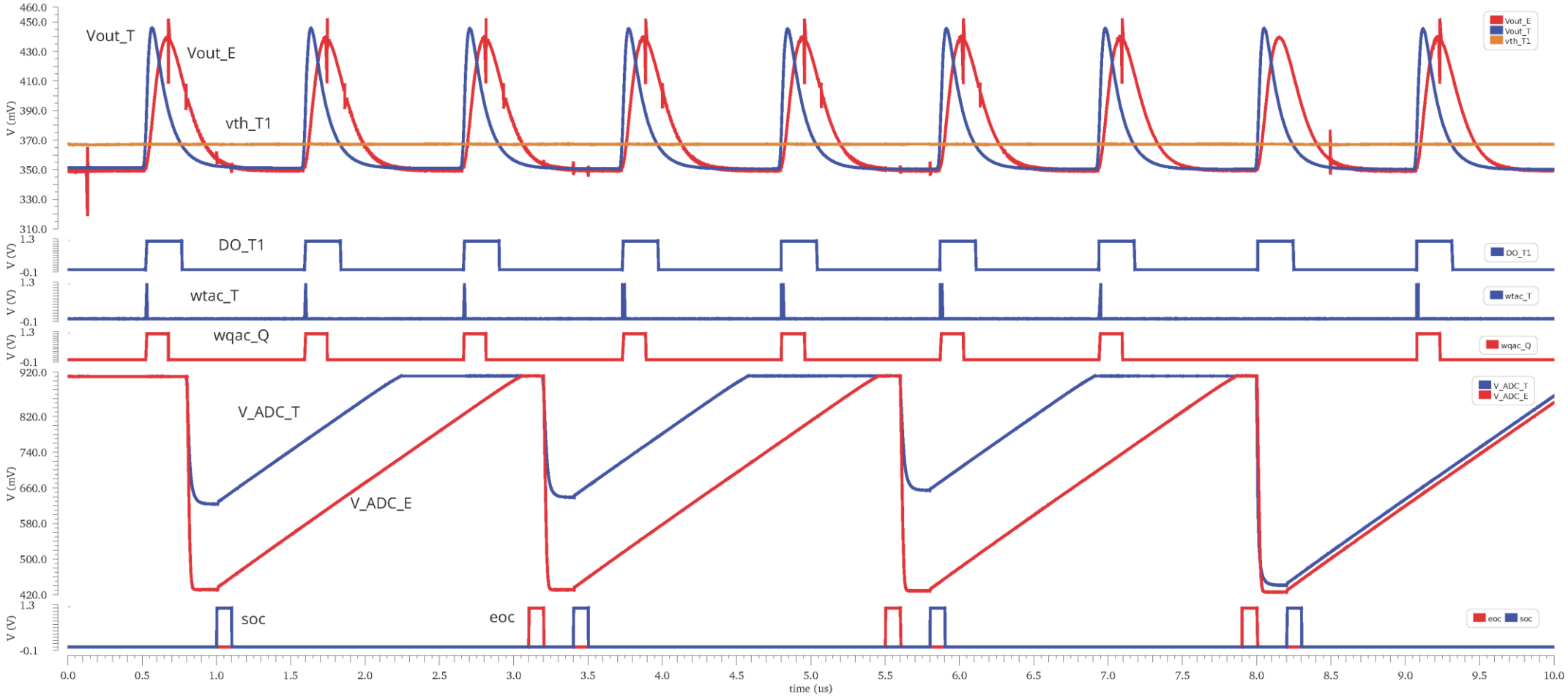


Energy Branch



High rate simulation

1 MHz input rate to simulate a burst of events and validate the buffers event de-randomization



Channel control logic

- Single or dual-threshold mode set by 4 channel configuration registers
  - Trigger_T: time measurement
  - Trigger_Q: start of S&H circuit
  - Trigger_E: event validation and ToT measurement
  - Trigger_B: end of event

Value	Trigger_T
0b00	do_T1
0b01	do_T1 AND do_T2

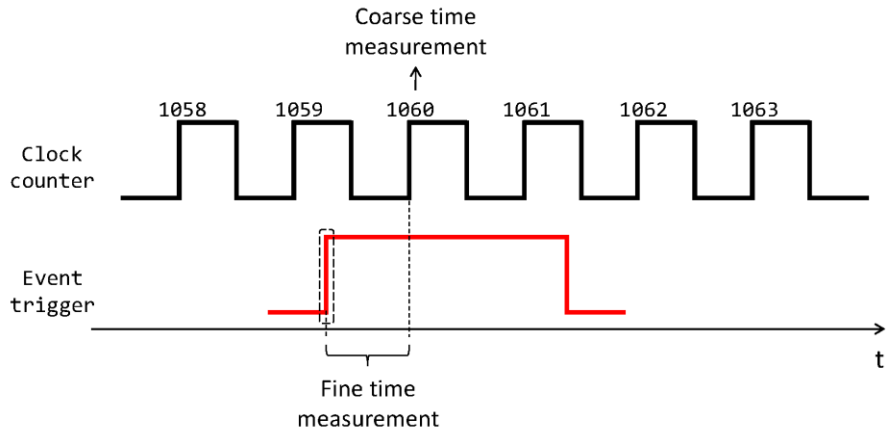
Value	Trigger_Q
0b00	do_T1
0b01	do_T2
0b11	test pulse

Value	Trigger_E
0b000	NOT(do_T1)
0b001	NOT(do_T2)
0b011	NOT(do_T1 AND do_T2)
0b101	do_T1
0b110	do_T2

Value	Trigger_B
0b000	do_T1
0b001	do_T2
0b011	do_T1 OR do_T2
0b110	test pulse

When the end of an event is flagged by the Trigger_B signal the event can be validated (sent to digitization) or discarded, according to the values of the other 3 trigger signals

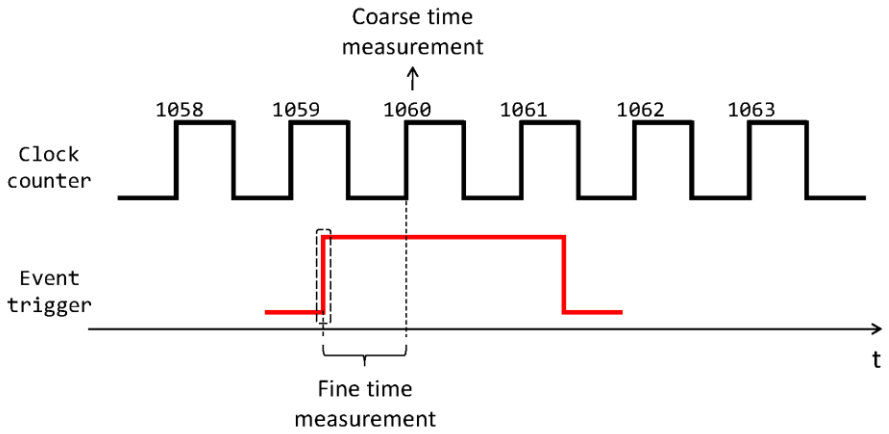
TDC operation

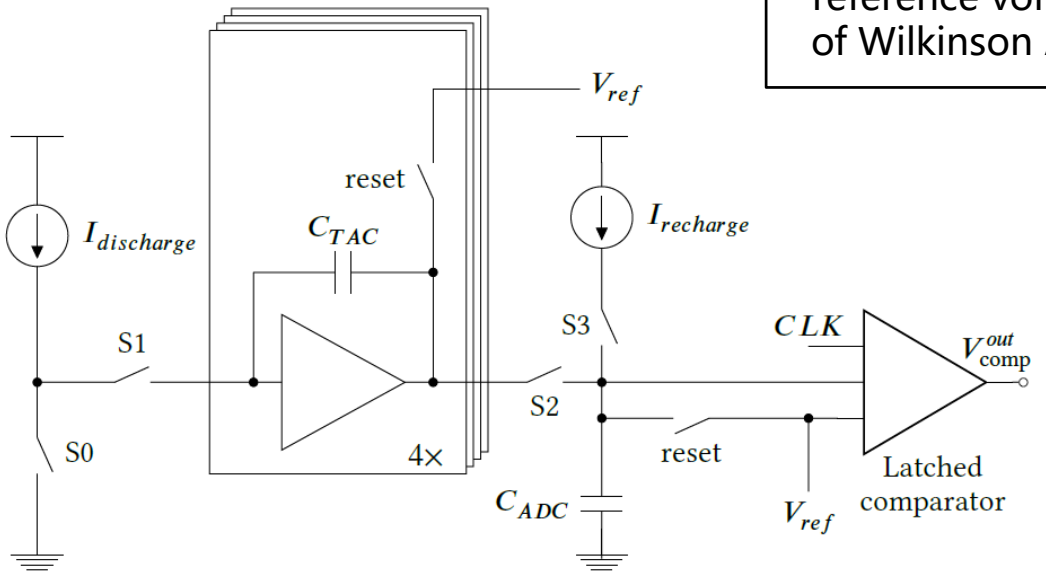


- **Coarse time measurement** from the chip master clock counter

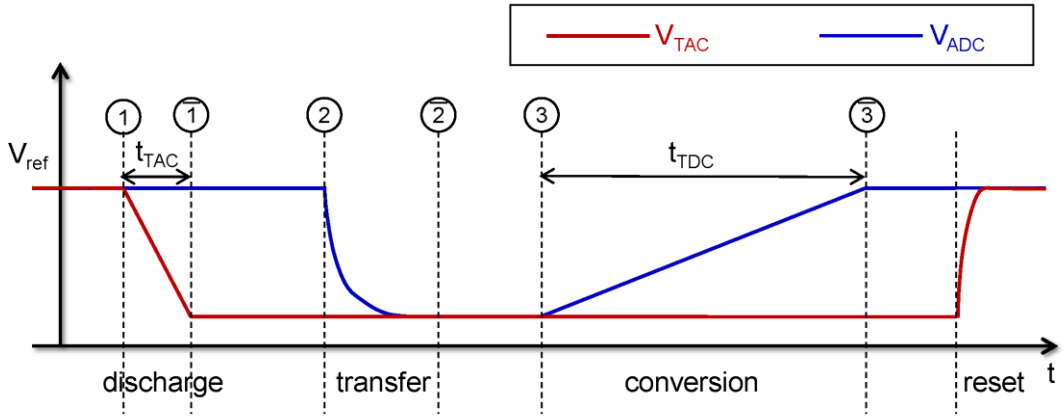
TDC operation

$\mathbf{V_{ref}}$ = external reference voltage of Wilkinson ADC



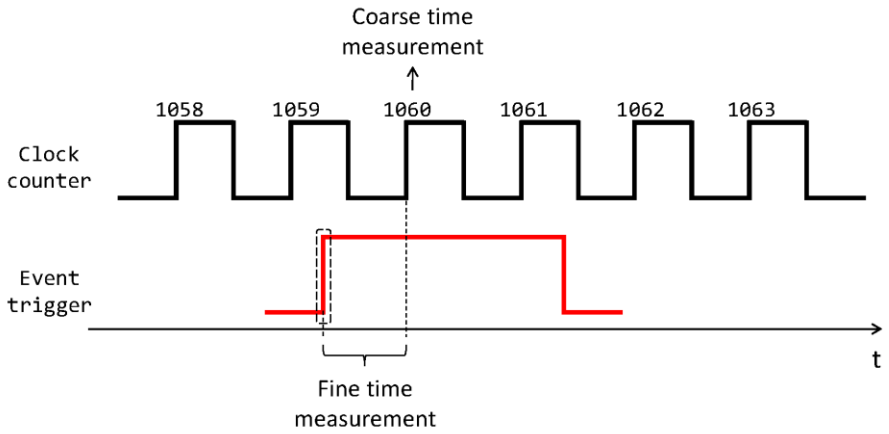


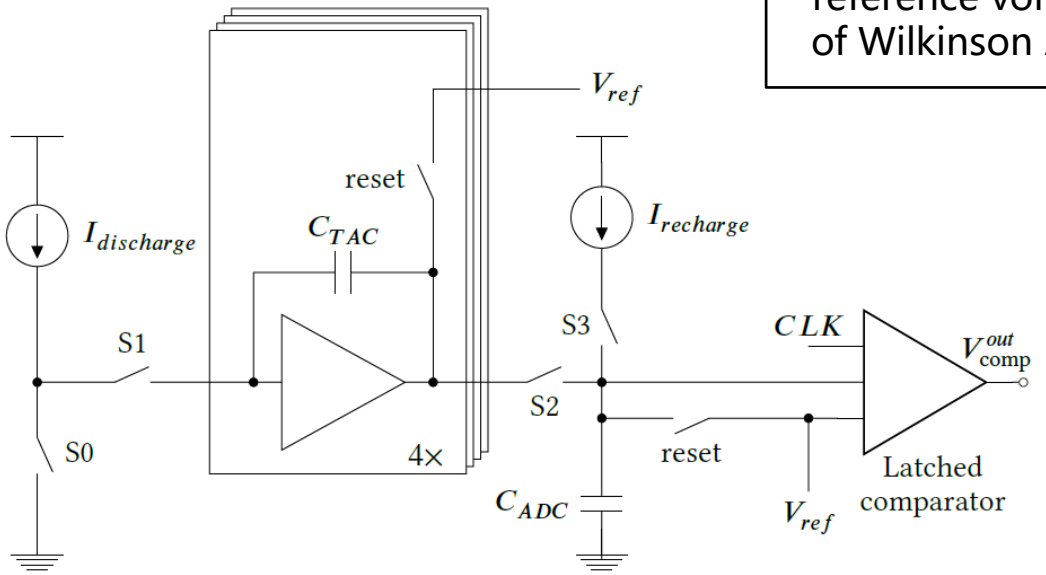
- **Coarse time measurement** from the chip master clock counter
- **Fine time measurement** with low-power analogue TDCs based on time interpolation

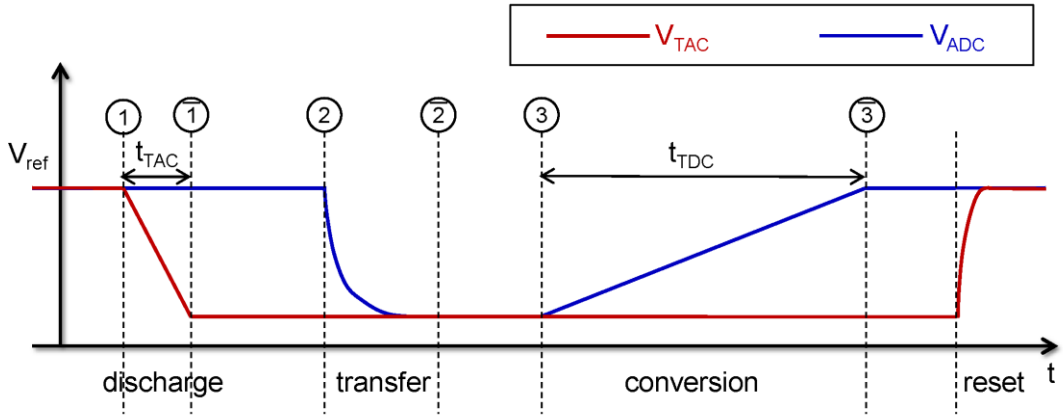


TDC operation

$\mathbf{V_{ref}}$ = external reference voltage of Wilkinson ADC



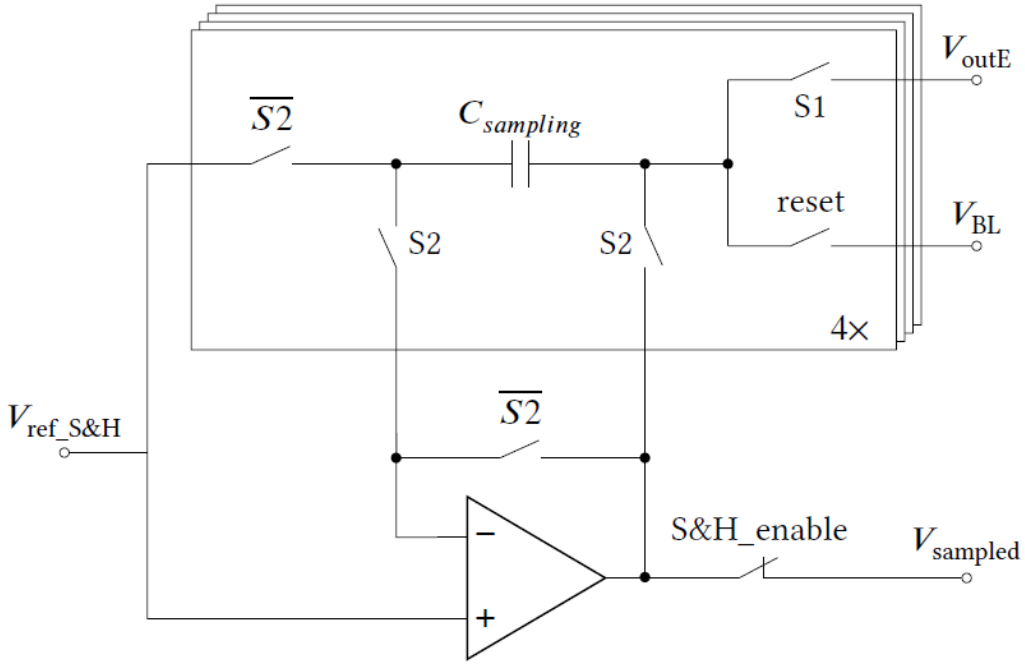


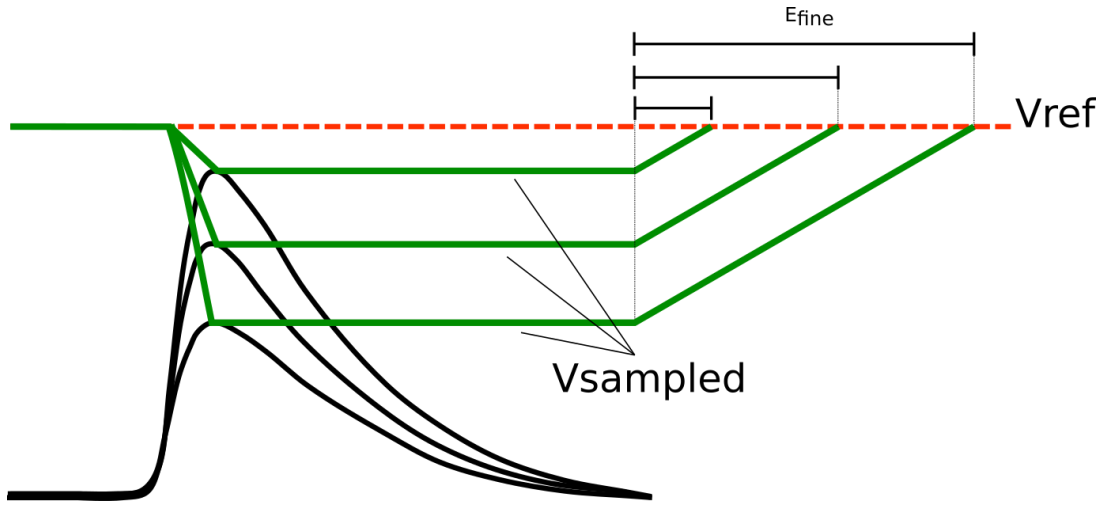


- **Coarse time measurement** from the chip master clock counter
- **Fine time measurement** with low-power analogue TDCs based on time interpolation
- Interpolation factor = $\frac{I_{discharge}}{I_{recharge}} \cdot \frac{C_{ADC}}{C_{TAC}} = 128$
- 50 ps time binning @ 160 MHz
- Quad-buffered TACs for **event de-randomization**
- TAC buffers with refresh scheme to avoid off-chip correction algorithm for leakage

Sample-and-Hold circuit

- **Charge measurement** with S/H circuit sampling the E-branch shaper output
- Programmable sampling time targeting the **signal peak**
- Digitization with **Wilkinson ADC** shared with the TDC
- Quad-buffered sampling capacitors for **event de-randomization**





Sample-and-Hold circuit

- **Charge measurement** with S/H circuit sampling the E-branch shaper output
- Programmable sampling time targeting the **signal peak**
- Digitization with **Wilkinson ADC** shared with the TDC
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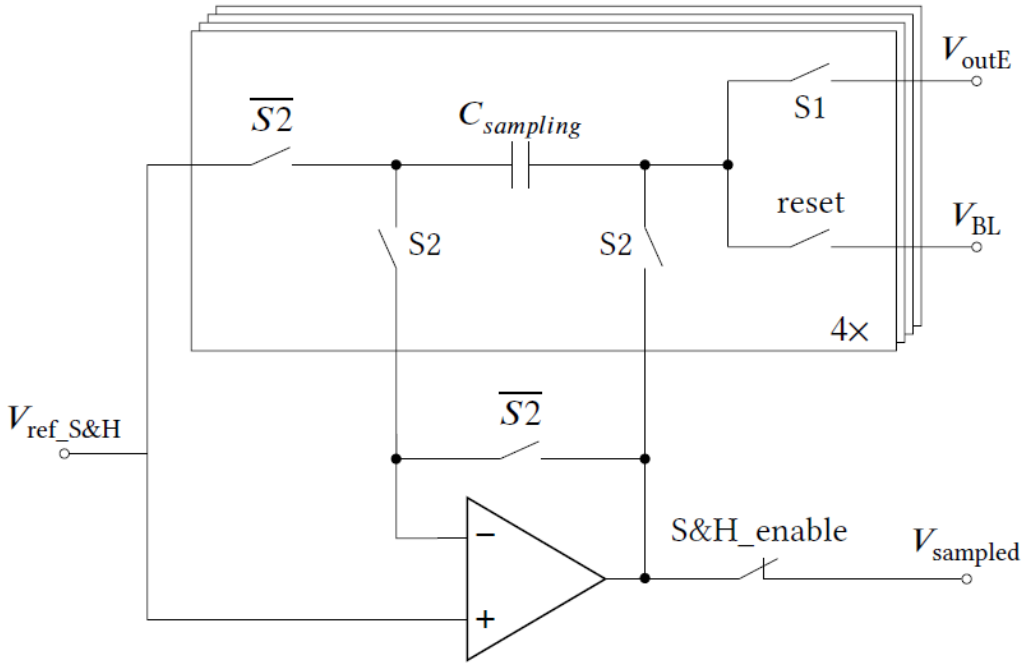
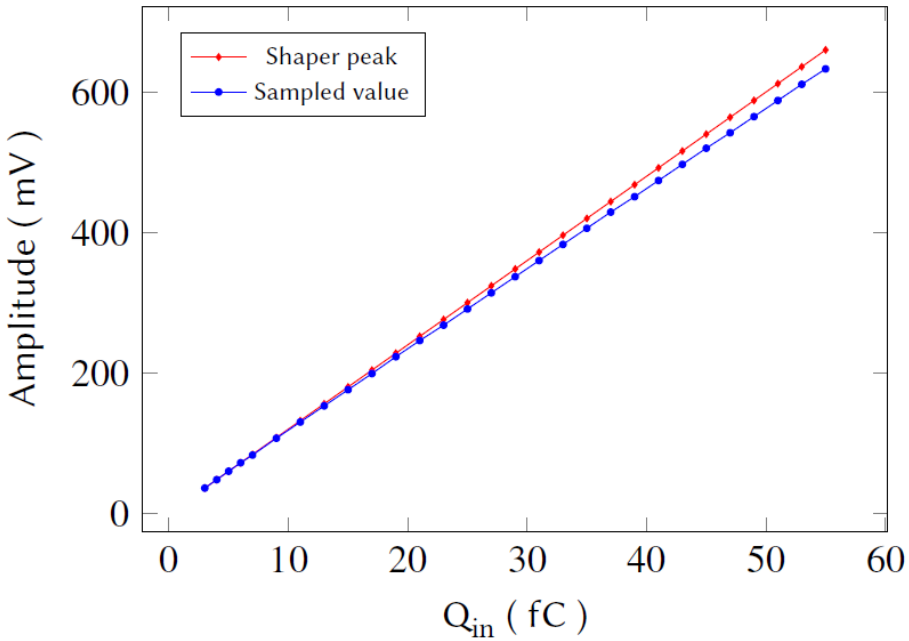


S&H peak sampling offset



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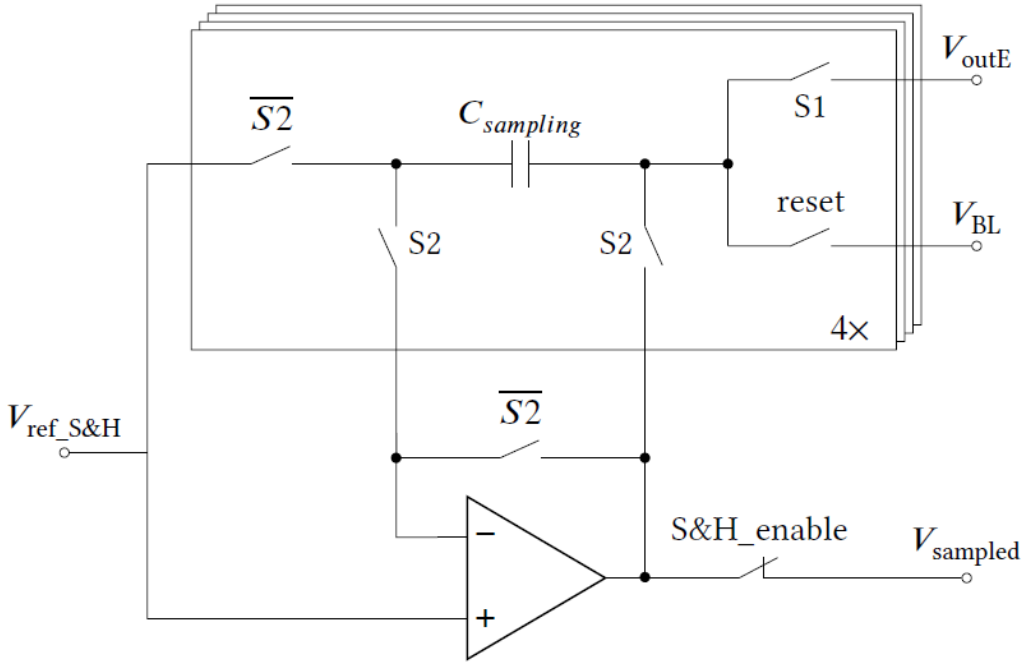
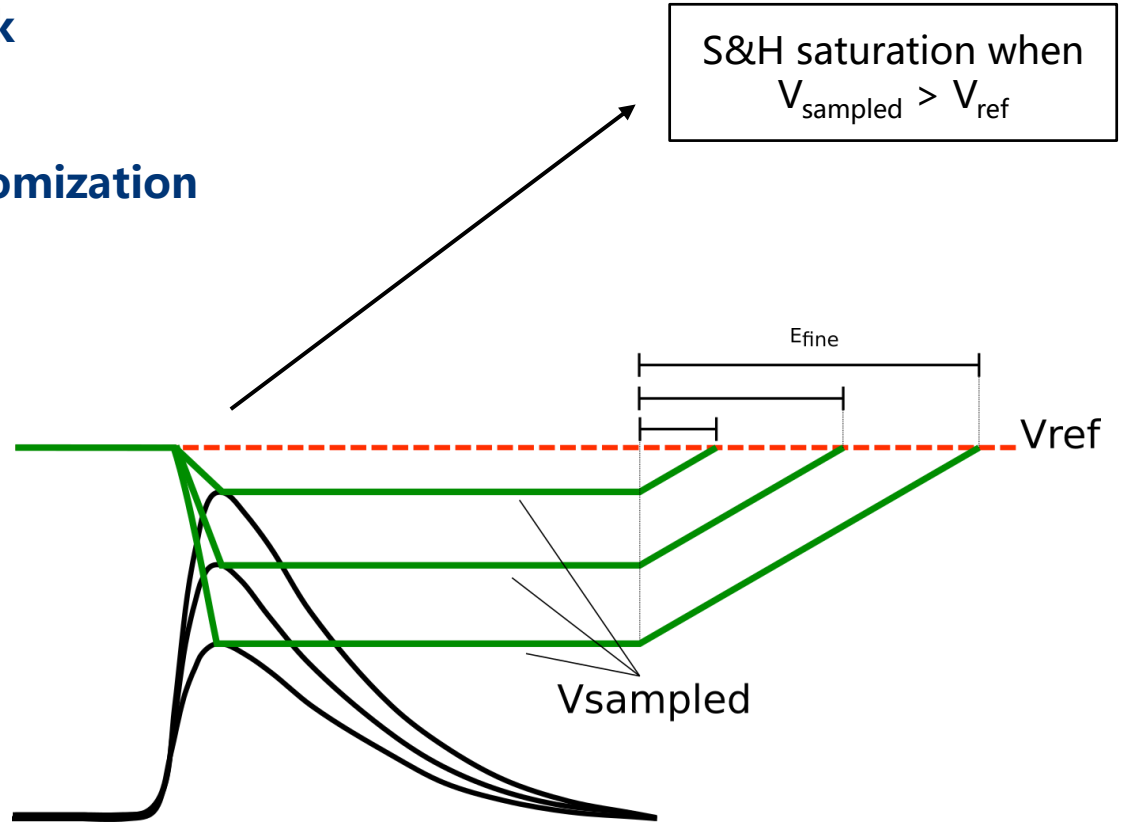
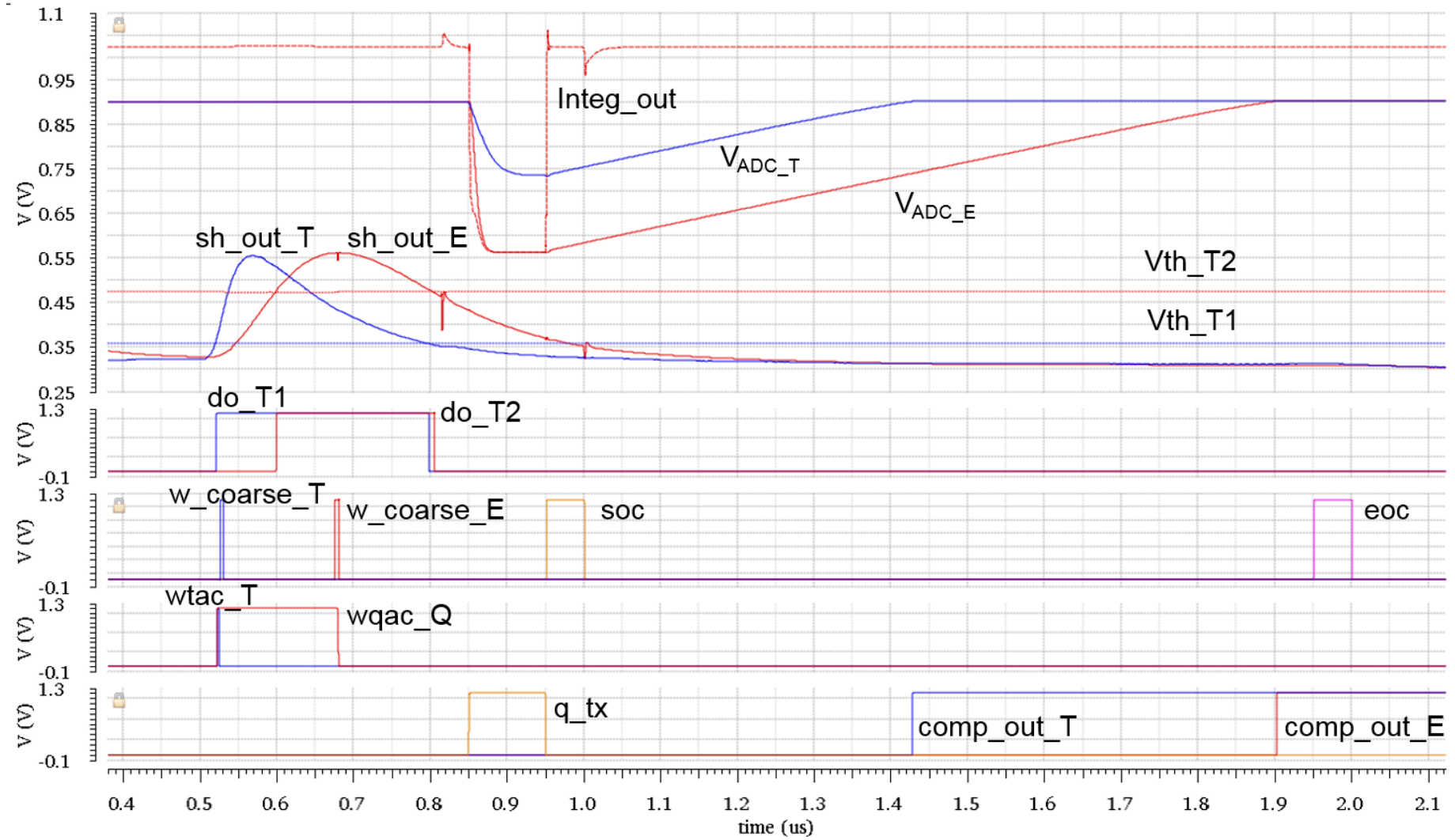




Full channel simulation



TIGER output words

1. **Event word**
   - contains raw hit information from the ASIC (channel, TAC, time, charge)
2. **Frame word**
   - generated every 2^{15} clock cycles (half of the Tcoarse counter range) and transmitted off-chip with top-priority
   - contains frame count number and the SEU count registered during that frame period
3. **Count word**
   - contains information about the number of events registered by on-chip counters
   - user can select valid/invalid/all events for debug purposes

EVENT WORD

K28.1	0b10	ch_id 6 bits	TAC	Tcoarse 16 bits	Ecoarse 10 bits	Tfine 10 bits	Efine 10 bits

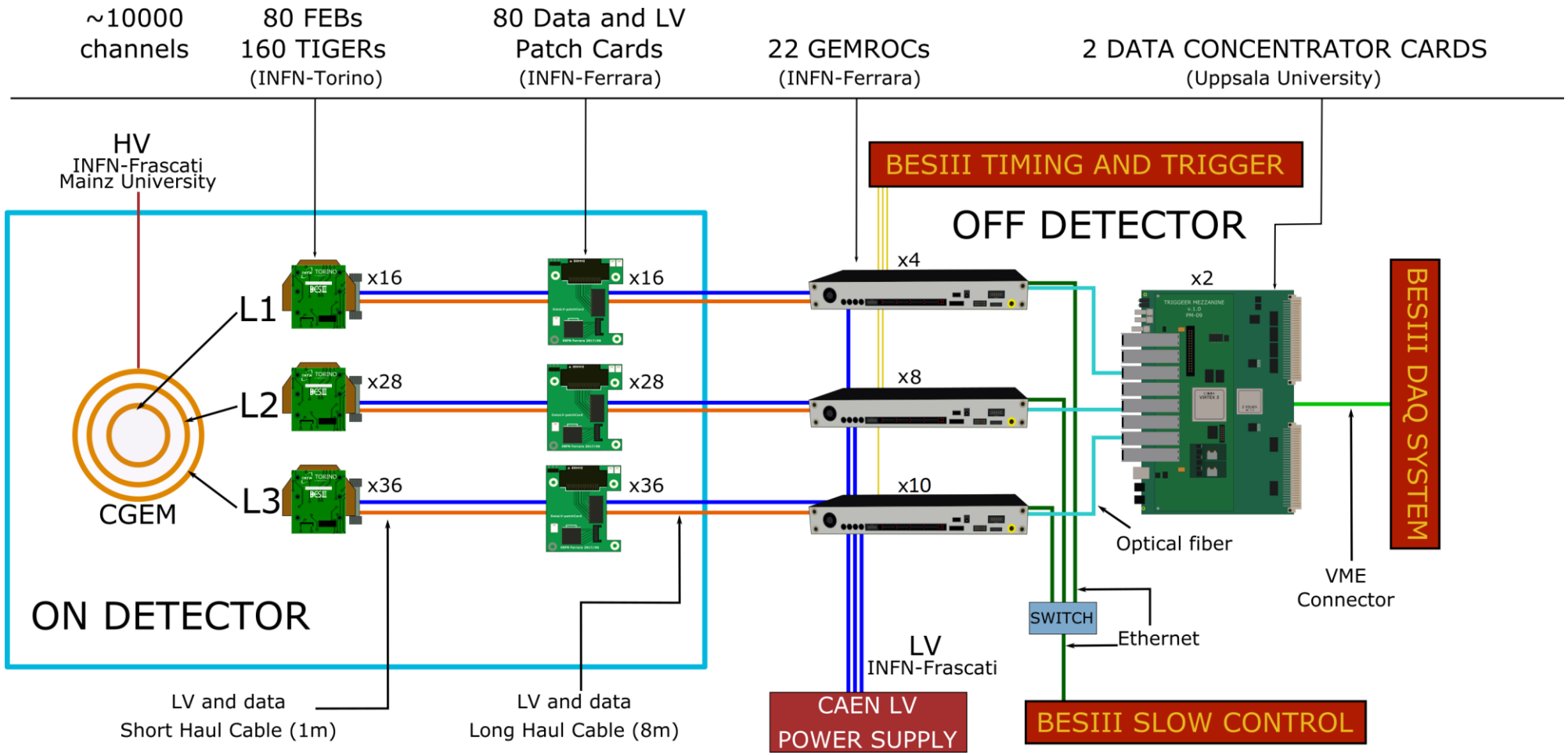
FRAME WORD

K28.1	0x00	reserved	frame count 16 bits	SEU count 15 bits

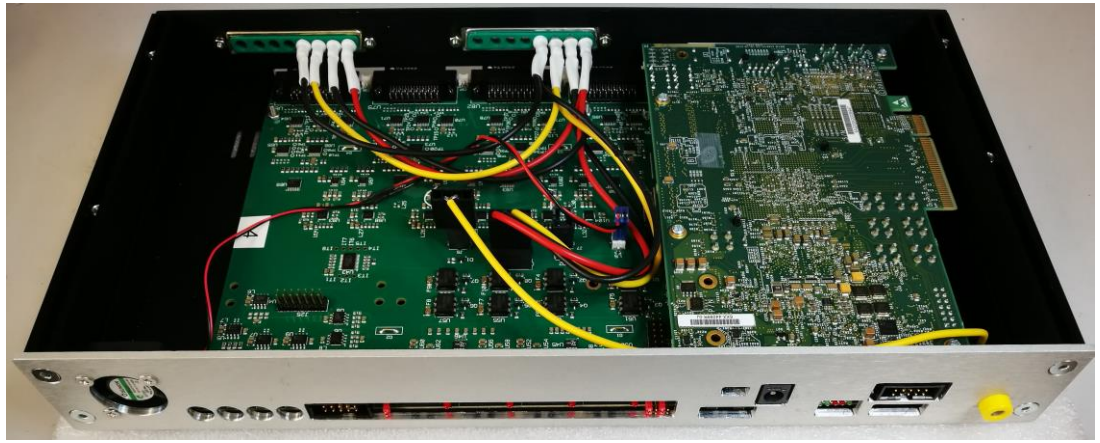
COUNT WORD

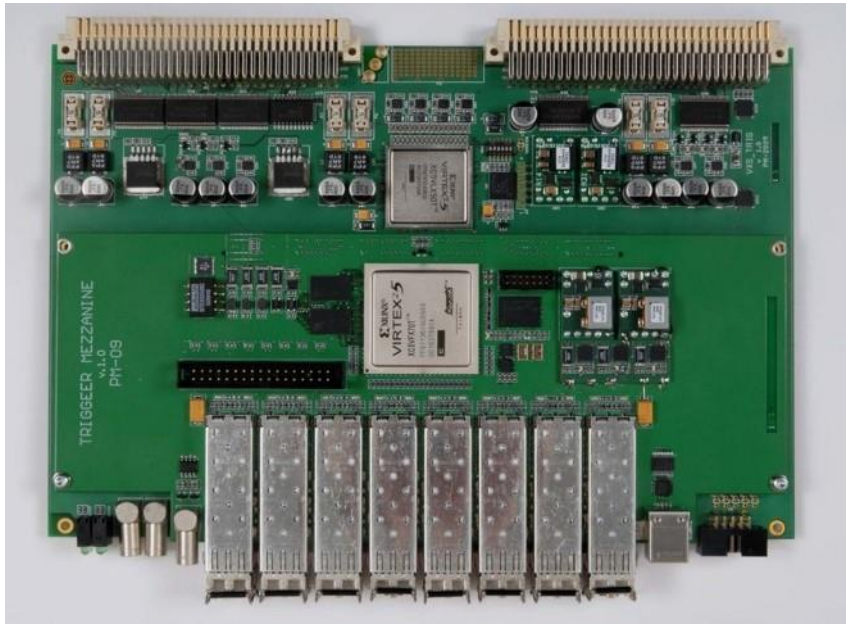
K28.1	0x01	reserved	ch_id 6 bits	counter value 24 bits

CGEM-IT electronics overview



Off-detector electronics





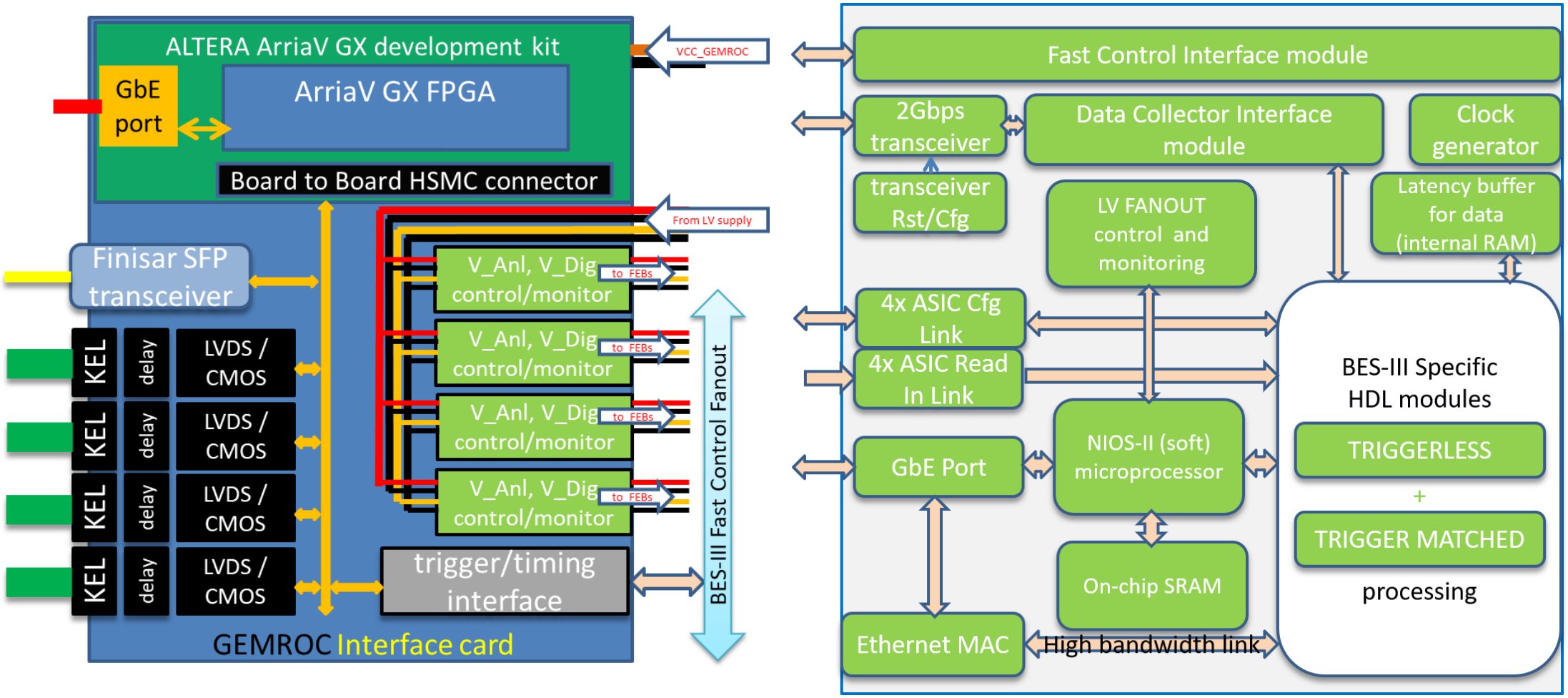
GEMROC (GEM ReadOut Card)

- Power, configuration and data interface with the on-detector electronics (8 TIGER for each GEMROC)
- **Trigger-Matching** operations

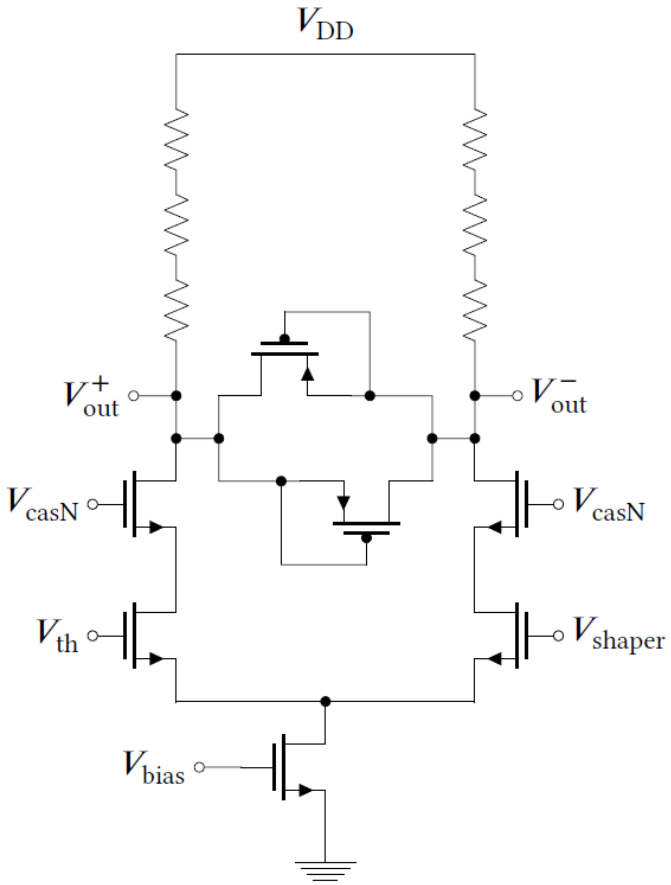
GEM-DC (GEM Data Concentrator)

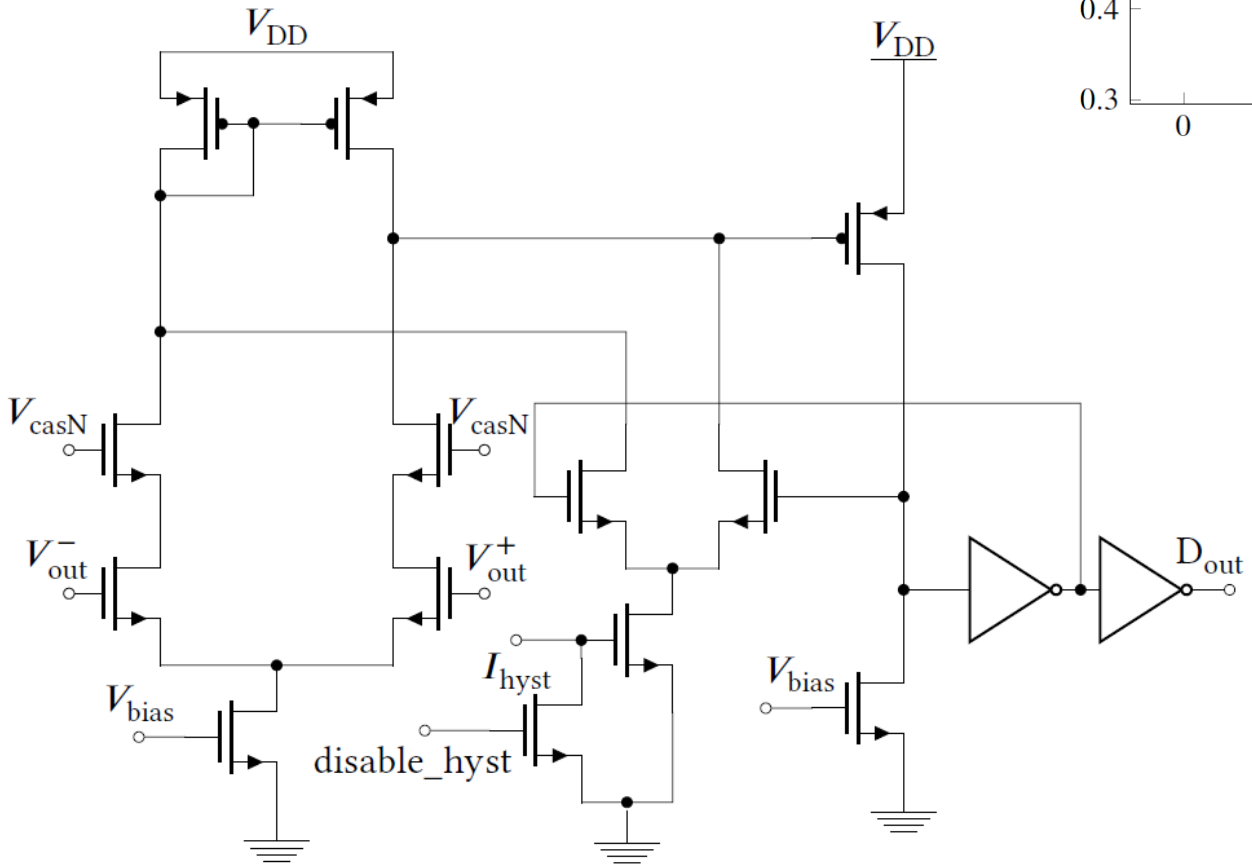
- Event merging operations
- Interface between the CGEM-IT electronics and the BESIII DAQ system

GEMROC hardware and firmware

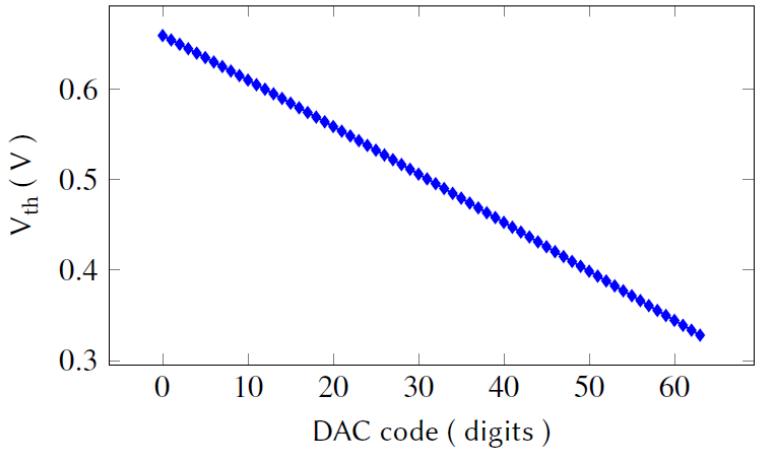


Discriminators



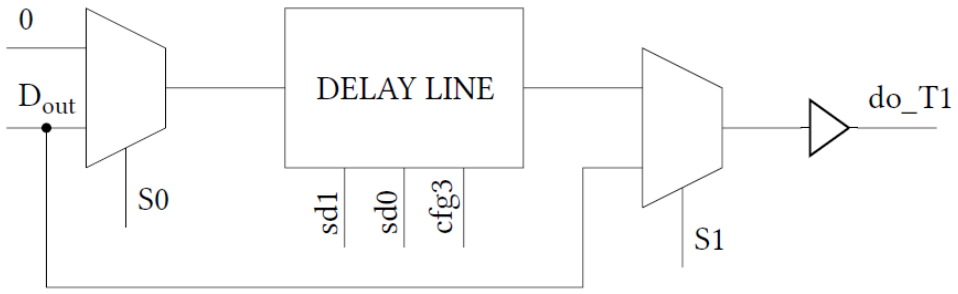


Threshold 6-bit DAC linearity



Delay line

A programmable delay line implemented at the output of the Time branch discriminator allows to delay its output in order to always use this discriminator (better timing performance) as the reference for the time measurements, even when the dual-threshold mode is enabled



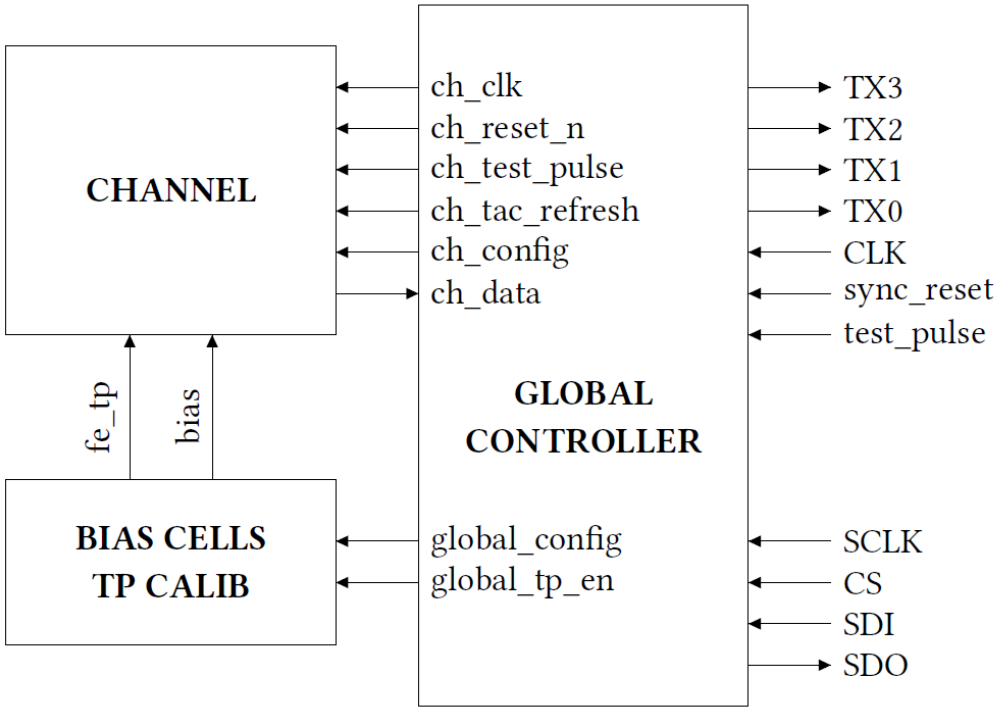
Value	Trigger_T
0b00	do_T1
0b01	do_T1 AND do_T2

Value	Trigger_Q
0b00	do_T1
0b01	do_T2
0b11	test pulse

Value	Trigger_E
0b000	NOT(do_T1)
0b001	NOT(do_T2)
0b011	NOT(do_T1 AND do_T2)
0b101	do_T1
0b110	do_T2

Value	Trigger_B
0b000	do_T1
0b001	do_T2
0b011	do_T1 OR do_T2
0b110	test pulse

Global controller and output words



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COUNT WORD

K28.1	0x01	reserved	ch_id 6 bits	counter value 24 bits

Test-pulse calibration circuit

- Allows to test the ASIC without the sensor (debug, calibration, etc.)
- Deployed on chip periphery
- Allows to generate an analogue test-pulse (both polarities) with programmable amplitude to be sent at the channels input
- A programmable switch allows to select which channel is receiving the test-pulse