NoAmpTPC: read-out of a TPC without gaseous amplification

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The NoAmpTPC read-out project

Interest of direct read-out of ionization electrons

- Better energy resolution if very low noise level
- Less constraints on choice of the gas mixture
- Simplified read-out → robust TPC
- No ion production
- Large segmentation of the read-out → good spatial resolution
- Could be interesting for several TPC project
- ATTRACT application in 2019 but failed...

6400 µm

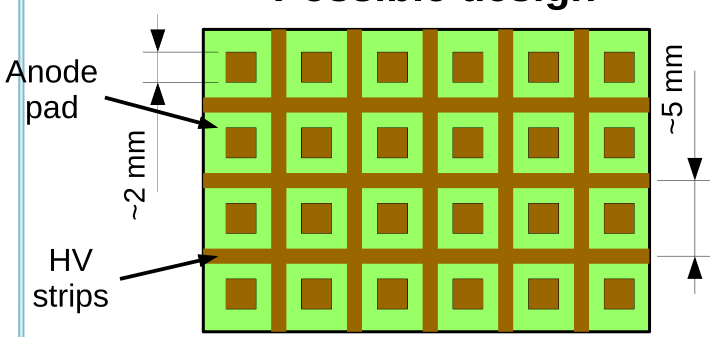
2800 µm

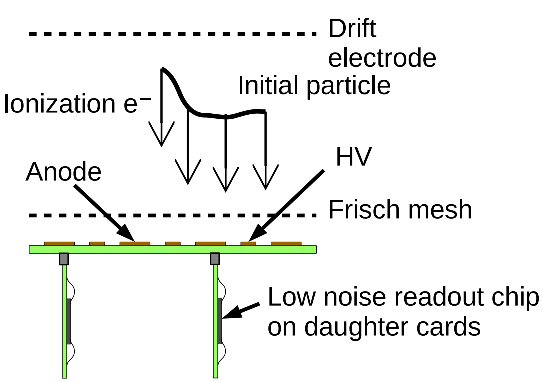
IDeF-X HD LXe chip
32 channels
$33e^- + 6e^-/pF$ noise
with 12µs peaking time

Principle of the read-out

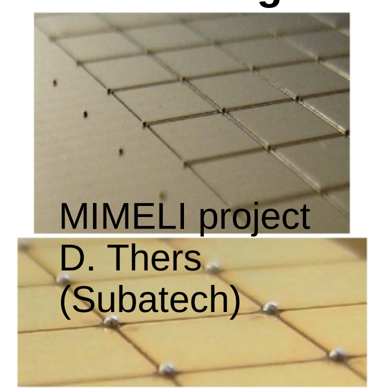
- Read-out board with large segmentation and very low-noise electronics
- Small read-out pads with Frish grid + focusing by polarized strips
- Very low-noise front-end chips → IDeF-X LXE (100 e^- with 10 pF capacitance) mounted on board or on daughter cards on the back side
- Electronics chain based on Dream chip

Possible design





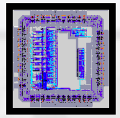
Other designs



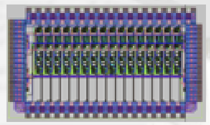
IDeF-X ASIC family

Very low noise chips for solid detectors, to be considered for ionization detection

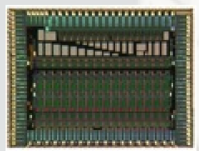
AMS 0.35µm — **IDeF-X :spectrometry channel**



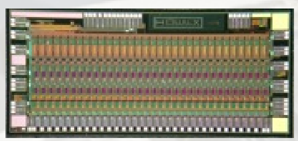
V0, Chip test, CSAs



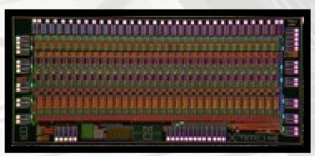
V1.0 Full analog chains



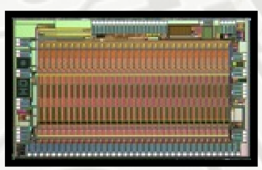
V1.1 Analog + Mux / Caliste64
System approach
Radiation evaluation



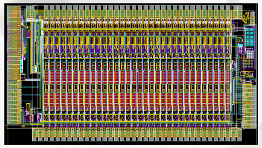
V.2 – ECLAIRs / Caliste 256
Fully programmable
Space qualified



BD – SSL/CINEMA
Fully programmable
Si or DSSD adapted

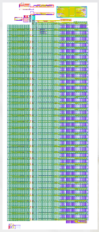


HD – Caliste HD
Low Power
Fully programmable
HD-BD upcoming



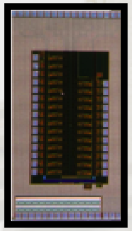
HD-LXE–
Low Power
Fully programmable
// outputs

ADC

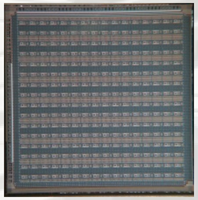


OWB-1 – ADC //
32 channel
13 bits
Low power
SEL hardened

XFAB 0.18µm — **IDeF-X :spectrometry channel**

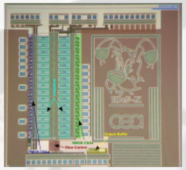


Caterpylar
Chip test
Very low noise
Very low power



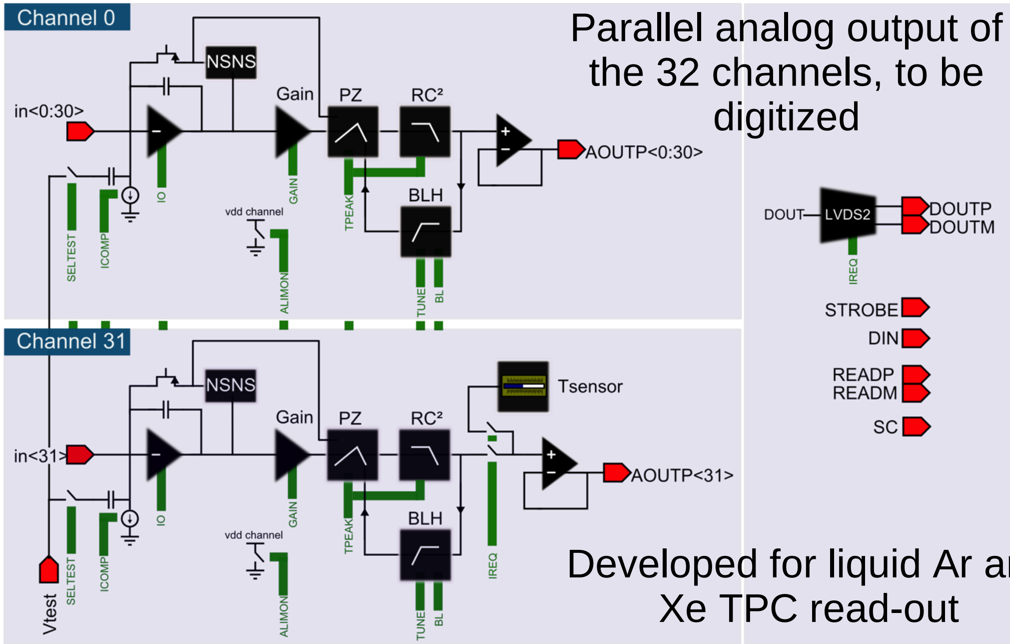
D^2R_1, 256 Pixels
300×300 µm²
Auto-trigger
very low power.

AMS 0.18µm



Caterpylar AMS
Chip test
Very low noise
Very low power

IDeF-X HD LXE version



Parallel analog output of the 32 channels, to be digitized

Developed for liquid Ar and Xe TPC read-out

- 32 channels. Parallel analog output
- CSA (new concept)
- Gain (50, 100, 150, 200mV/fC)
- PZ cancellation
- RC² filter (T_{PEAK}=1 to 10µs)
- Base Line Holder (switchable)

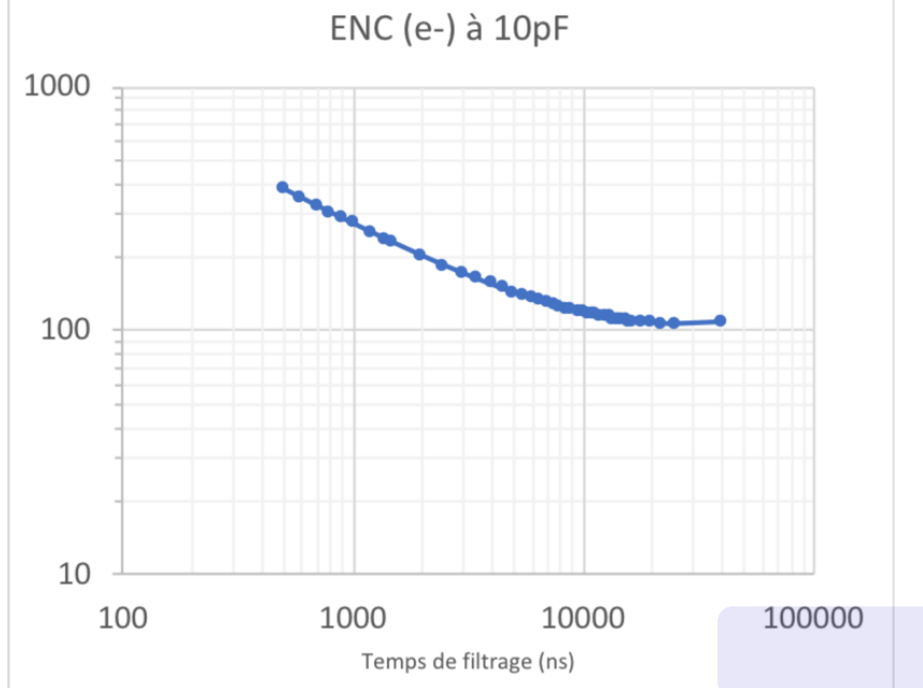
- Embedded temperature Sensor with absolute resolution of 0.5°C.
- Slow Control
  - Multi ASIC interface
  - Gain
  - T_{PEAK}
  - I_{CSA}(23-100µA)
  - I_{LEAK}
  - Channel mask
  - Test mask
  - AlimON
- Power on reset
- “smart” LVDS input/output
- Hardened digital standard cell
- Low power: 0.8mW /channel

IDeF-X HD (LXE) performance

6400 µm

2800 µm

LXE version used for XEMIS project (liquid Xenon TPC, D.Thers, Subatech) for 3 gammas medical imaging.



Noise levels :

- $80\ e^- + 15\ e^-/pF$ with 1 µs peaking time
- $33\ e^- + 6\ e^-/pF$ with 12 µs peaking time

Dream electronics chain

Constraints

IDeF-X chips only do amplification and shaping

Triggering, sampling, digitization and recording to be done by other electronics + DAQ

Need to record signal amplitude, time, optionally signal shape

Possible electronics chain

Several front-end chips can be considered:

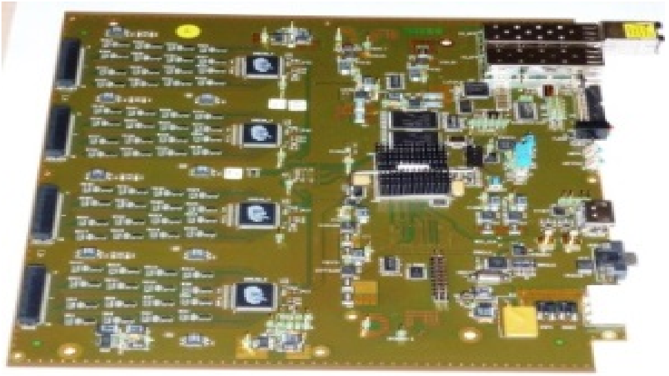
- AGET and DREAM (IRFU + others): 64 channels, auto-triggable, analog sampling on SCA capacitor array (512 samples 1 to 50MHz), to be combined with ADC, front-end stages can be by-passed
- SAMPA (ALICE TPC): 32 channels, integrated ADC (10 bits 10-20 MS/s) and DSP, triggerless continuous read-out mode, 10 x 320Mb/s data links
- VMM (ATLAS NSW): 64 channels, auto-triggable, peak and time measurements, integrated ADC (10 bits), triggerless mode
- Other solutions ?

Choice for NoAmpTPC proto

DREAM "FEU" (front-end unit) card with 8 chips → 512 channels

ADC chips integrated to the card

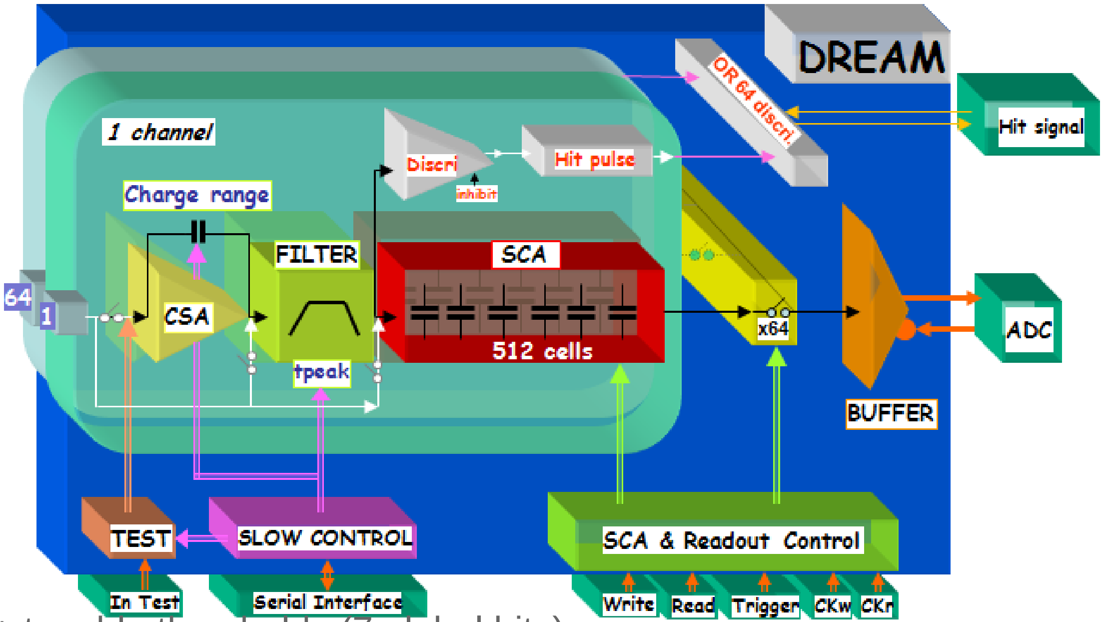
Standalone DAQ



DREAM front-end chip

Irfu
cea
saclay

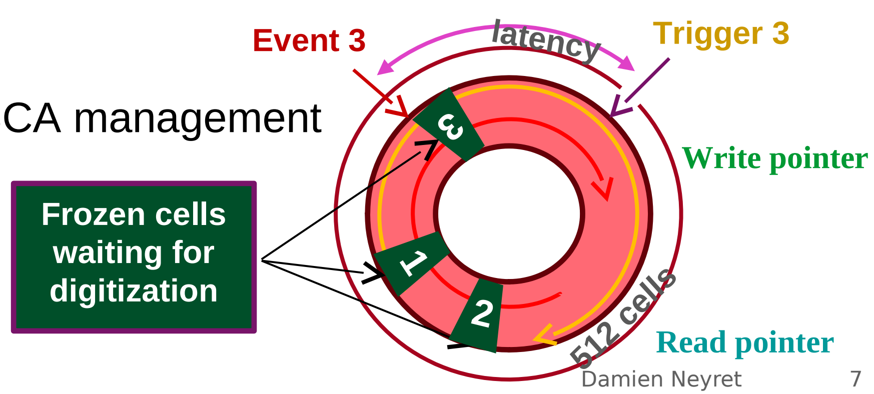
- 64 channels
- 4 gains / channel: 50 fC, 100 fC, 200 fC, 600fC
- 16 peaking times: 50 ns to 1 µs
- **512**(511) analog memory cells
- Sampling rates: 1MHz to 50 MHz
- Read-out rate: 20 MHz



- Auto trigger: discriminator + tunable thresholds (7 global bits)
- Multiplicity information: digital signal (LVDS); 8 multiplicity levels
- SCA read-out: only "trigged" cells of the 64 channels
- Possibility to short the CSA and input directly into RC2 filter or into SCA

DREAM ASIC
- developed for CLAS12 Micromegas
- stand high input capacity (> 200pF)
- large trigger and counting rates

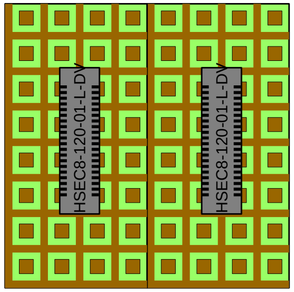
SCA management

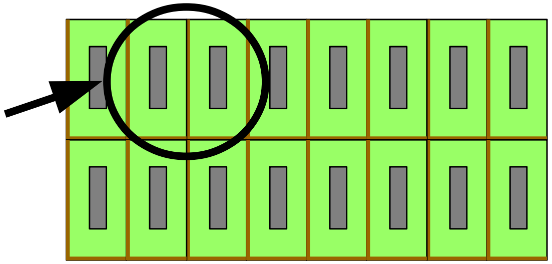


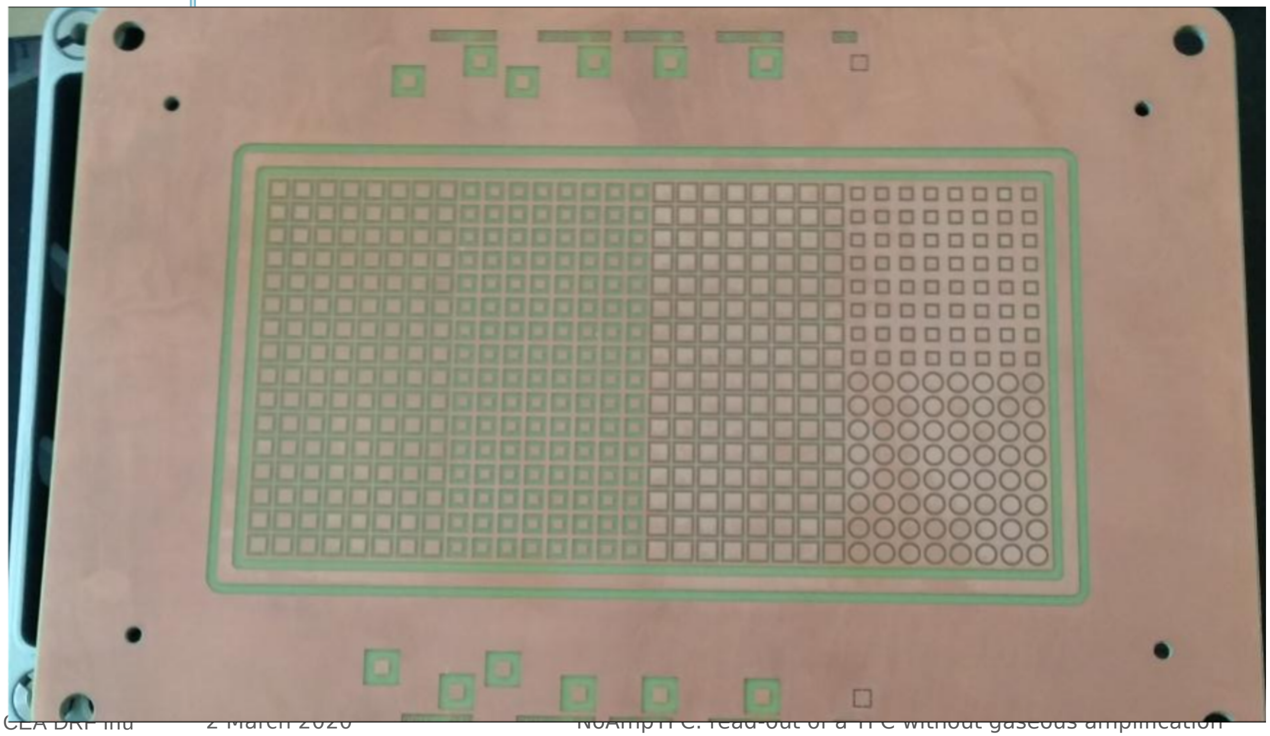
NoAmpTPC prototype design

Read-out board

- 512 pads within 8x16cm active area
- 5mm pitch, several pad sizes
- HV guard strips to focus electrons on pads
- Pad geometry optimization using Garfield++ simulation
- Produced in FR4 material, production with low ε_R material failed up to now
- Integration in progress



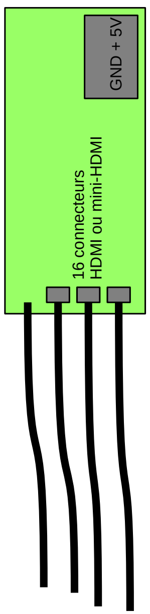


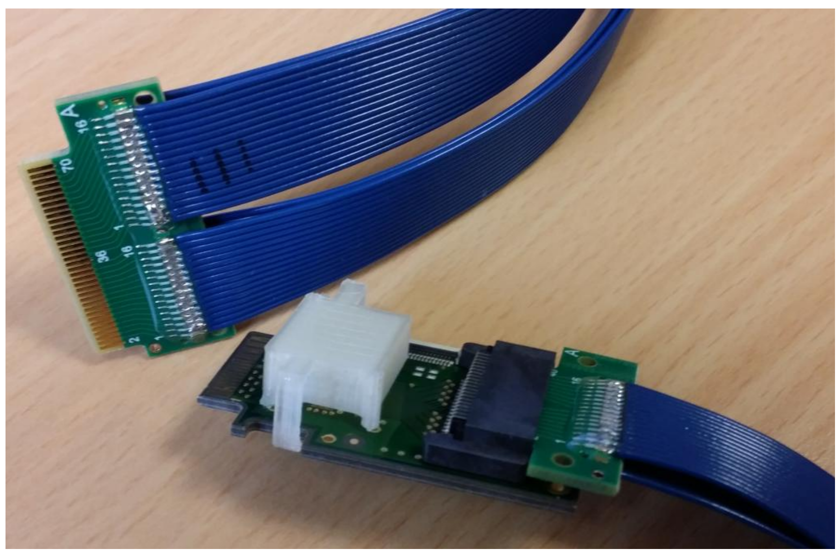


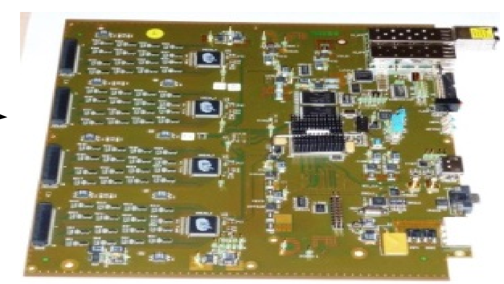
Prototype design at Saclay

IDeF-X daughter cards

- Holding the IDeF-X chip
- Samtec HSEC8 connectors
- Powered and controlled by an external service card
- Connected to DREAM FEU card by micro-coax flat cables
- 20 cards produced with low ε_R material (RO5880)
- Power/control service card still in production



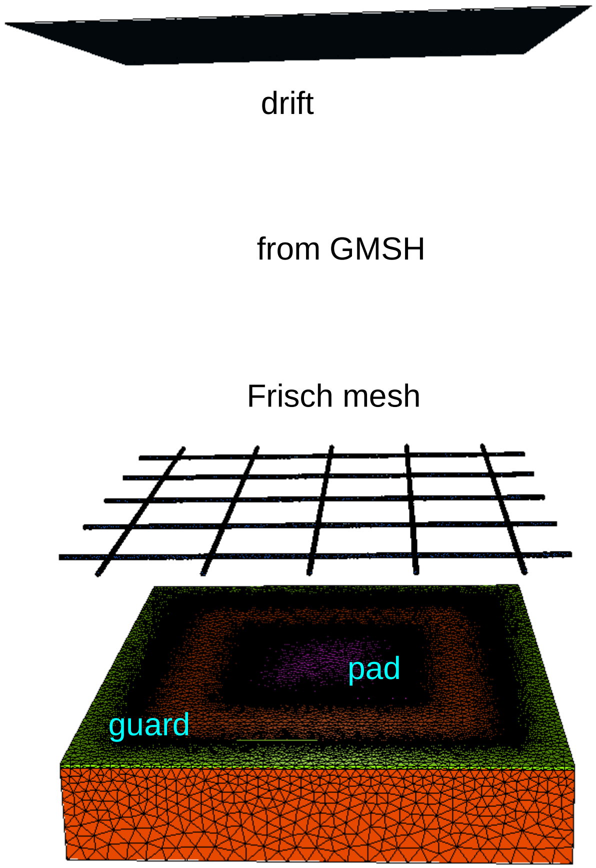


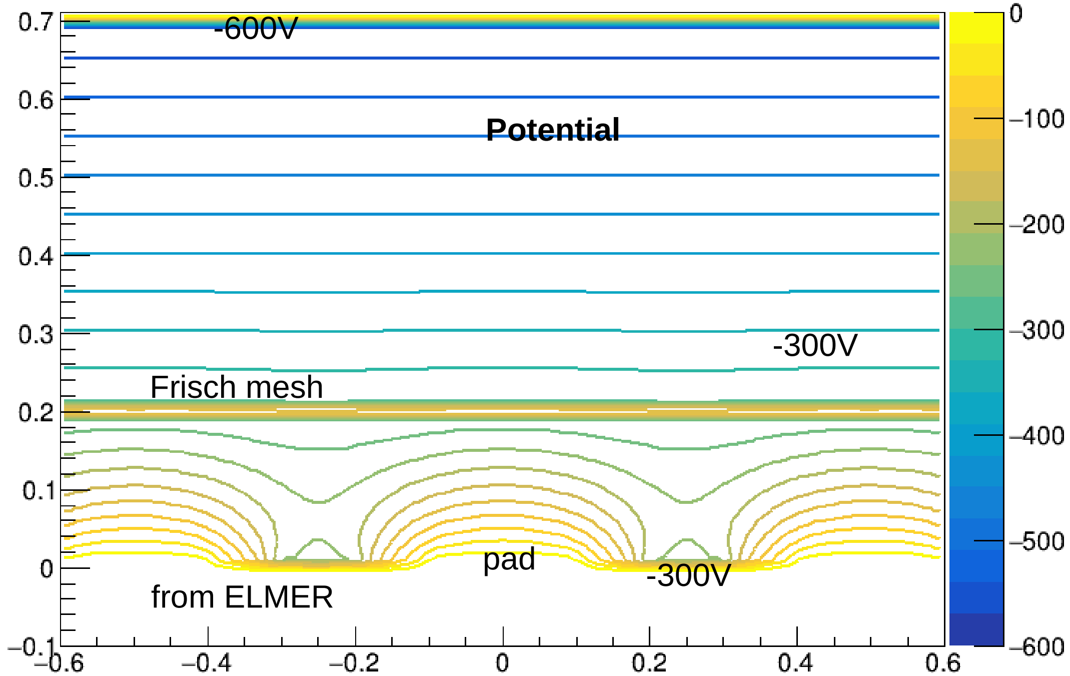


Garfield simulation of the read-out plane

Simulated design

- Read-out plane with electrode pads and focusing HV guard strips
- Amplitude of signal, electrons lost on Frisch mesh and on FR4
- Goal: optimization of pads/focusing guard strips geometry, evolution vs electrodes HV
- Method: GMSH (geometry, 2D/3D meshing) + ELMER (electric field) + Garfield++ (electron and ion drift), Ar+5% isobutane gas mixture 1 bar





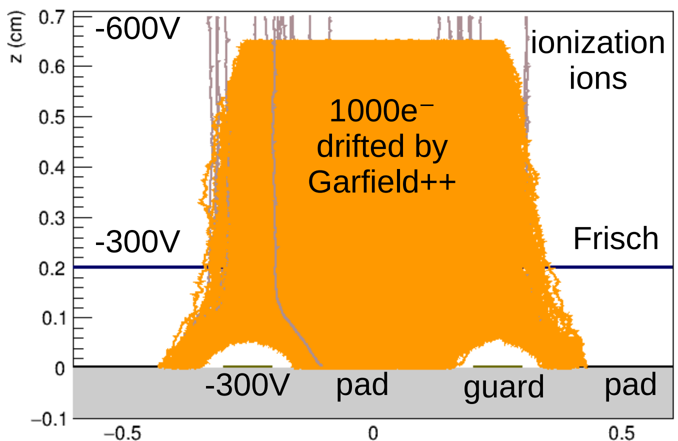
Garfield++ simulation of the read-out plane

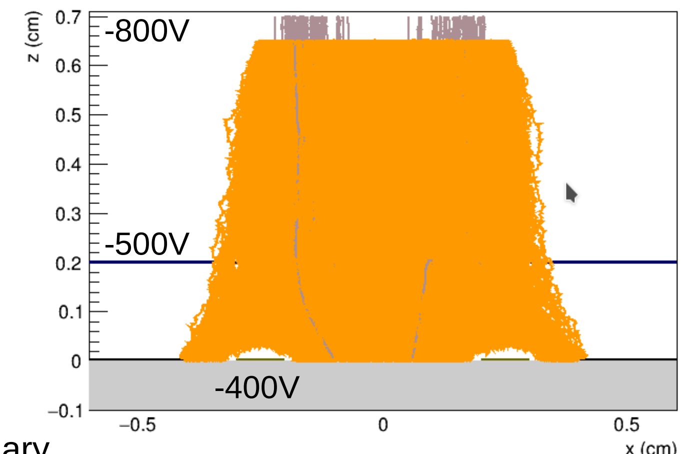
Dependence to the electrode voltage

Capture of electron by the Frisch mesh

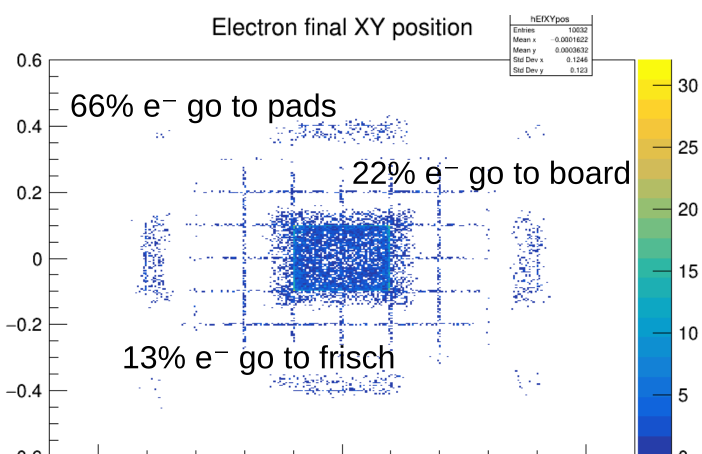
Efficiency of the guard electrodes to avoid e⁻ going to board insulator

Ion production at larger HV

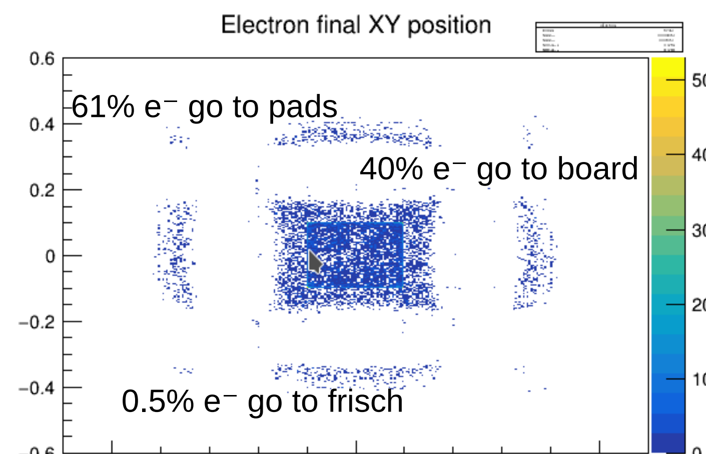




Very preliminary



2mm pad, -600V/-300V/-300V



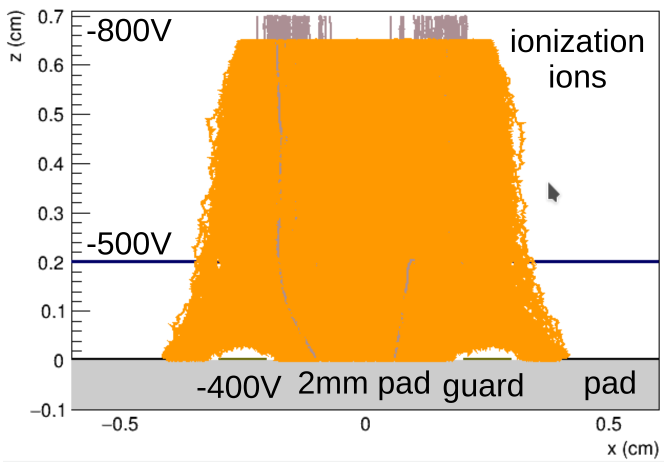
2mm pad, -800V/-500V/-400V

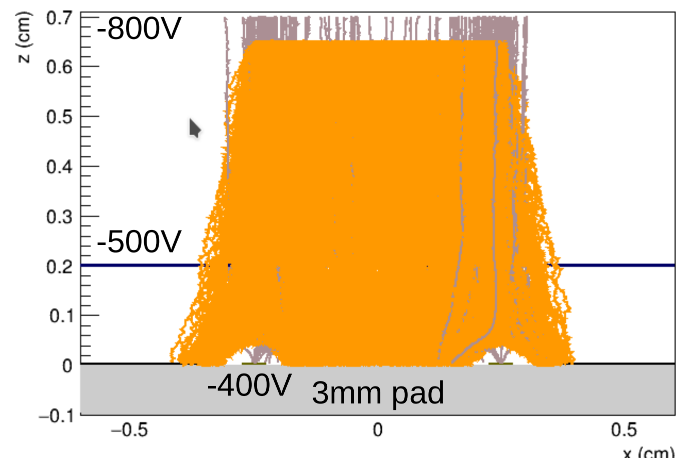
Garfield simulation of the read-out plane

Dependence to the read-out plane geometry

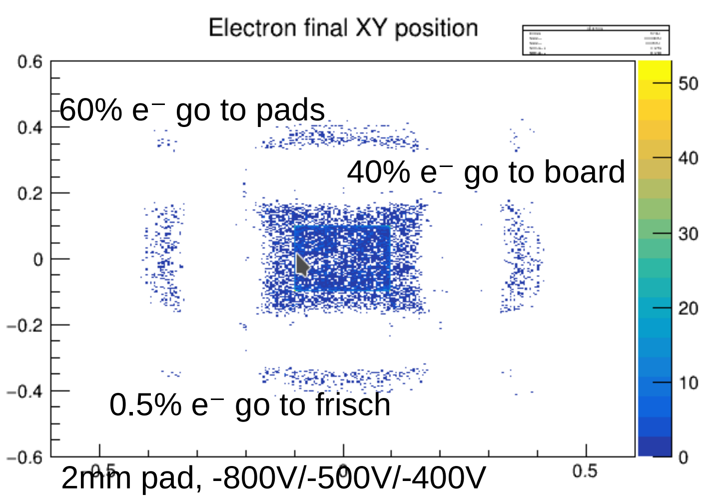
Larger pads to collect more electrons

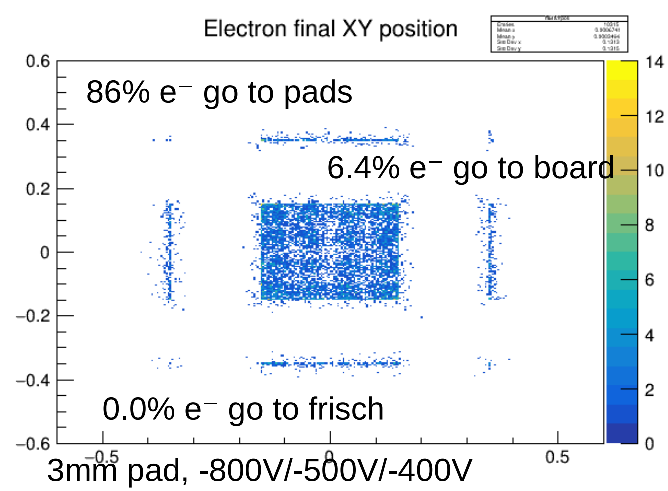
But also larger capa → more noise ?





Very preliminary





Garfield simulation: overview of performance

Several pad sizes tested

Better electron collection with larger sizes
Not clear effects of Frisch vs guard voltages
Further studies needed

Geometry (5mm pitch)	Voltages drift/frisch/ guard	% e⁻ on pad	% e⁻ on board	% e⁻ on Frisch	% event with signal integral = 1	% events with 1 ion or more	% event with signal integral < 1
2mm pads 1mm guard	600/300/300	66 %	22 %	13 %	65 %	0,3 %	34 %
	800/500/400	61 %	41 %	0.4 %	57.9 %	1.3 %	40.8 %
	700/400/500	83 %	3.6 %	16 %	80 %	1.3 %	19 %
2mm pads 2mm guard	600/300/300	74 %	0.1 %	27 %	72.5 %	0.7 %	26.7 %
	800/500/400	107 %	1.6 %	4.3 %	82.1 %	9.4 %	8.4 %
	800/500/500	100 %	0 %	10.5 %	82.6 %	6.8 %	10.6 %
3mm pads 0.5mm guard	600/300/300	88 %	1.5 %	6.3 %	92 %	0.2 %	7.4 %
	800/500/400	86 %	6.4 %	0 %	91.8 %	2.5 %	5.7 %
	700/400/400	93 %	1.1 %	1.4 %	96.9 %	0.8 %	2.2 %
3.5mm pads 0.5mm guard	600/300/300	96 %	0 %	4.1 %	95.7 %	0.1 %	4.1 %
	800/500/400	100 %	0 %	0 %	98 %	1.9 %	0 %
	700/400/300	98 %	0.2 %	0.2 %	98.9 %	0.8 %	0.3 %

Conclusion and prospects

NoAmpTPC prototype

- Most elements produced, but the whole design/production process took a very long time…
- Last missing one (power/control card) under production
- First tests expected end of March

TPC simulation with Garfield++

- Small 2x2mm pads probably not large enough to collect all electrons
- Impact of 3x3mm (or larger) pad capacitance ?
- Voltage settings to be studied with the real setup

Prospects

- Performance to be studied with the real prototype with different pad and guard strip sizes: noise level, sensitivity, efficiency, energy and spatial resolutions
- Test in high pressure chamber considered
- If successful larger TPC demonstrator ? Very low noise chip with integrated digitization ?