

Free Running DAQ for COMPASS++/AMBER

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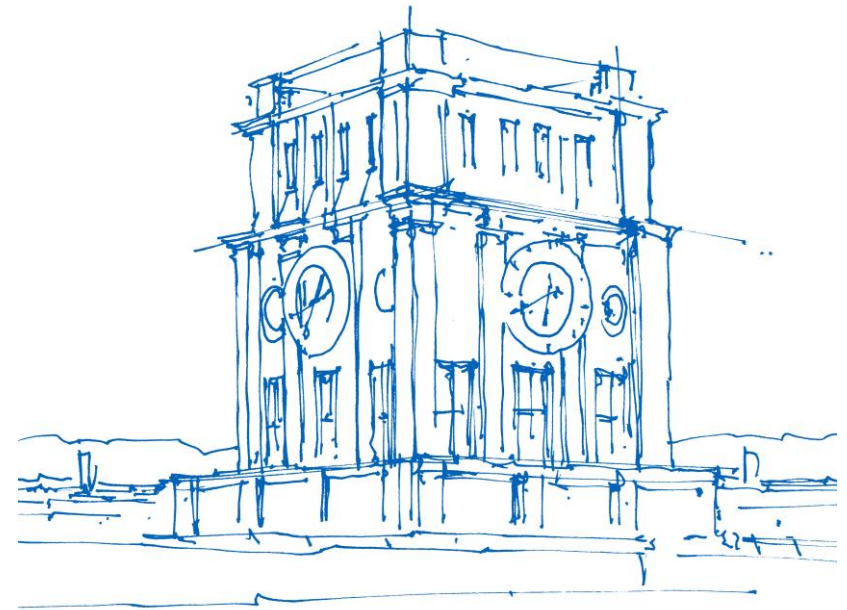
Institute for Hadronic Structure and Fundamental Symmetries (E18)

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COMPASS FETDAQ Workshop

CERN, March 2-3



Uhrenturm der TUM

Physics programs and Free Running DAQ

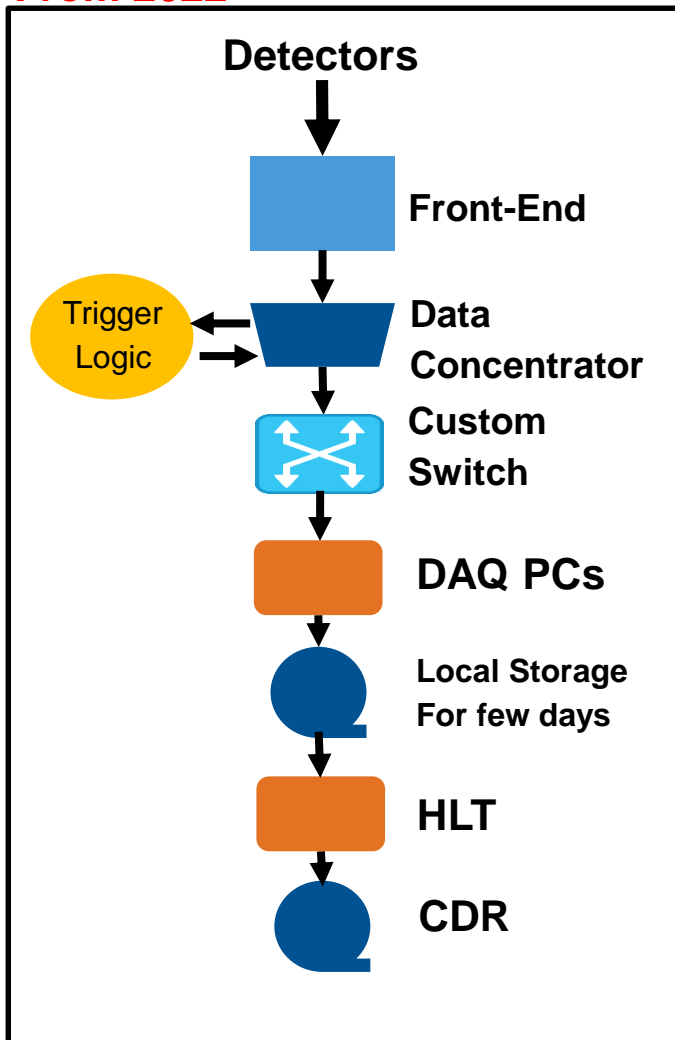
- Proton-radius measurement using elastic muon-proton scattering
- Drell-Yan and charmonium production using hadron beams
- Measurement of antiproton production cross sections for dark matter search

Why we choosed free running DAQ architecture?

- Flexible solution
- Combination of slow and fast detectors: TPC and others
- High quality trigger algorithm
 - Recoil-proton in TPC
 - Kink trigger with very low angular resolution using SciFi/Silicon detectors
 - “Unlimited” time for trigger decision
- High data rate capable DAQ
- Inexpensive with current technologies

Free Running iFDAQ

From 2022



Free running DAQ ?

- Capability to run without any data reduction
- Not efficient to store all data => data reduction needed
- **Triggerless FE electronics !!!**

Triggerless mode

- Alignment
- Hardware trigger verification
- Pilot run

Triggered mode

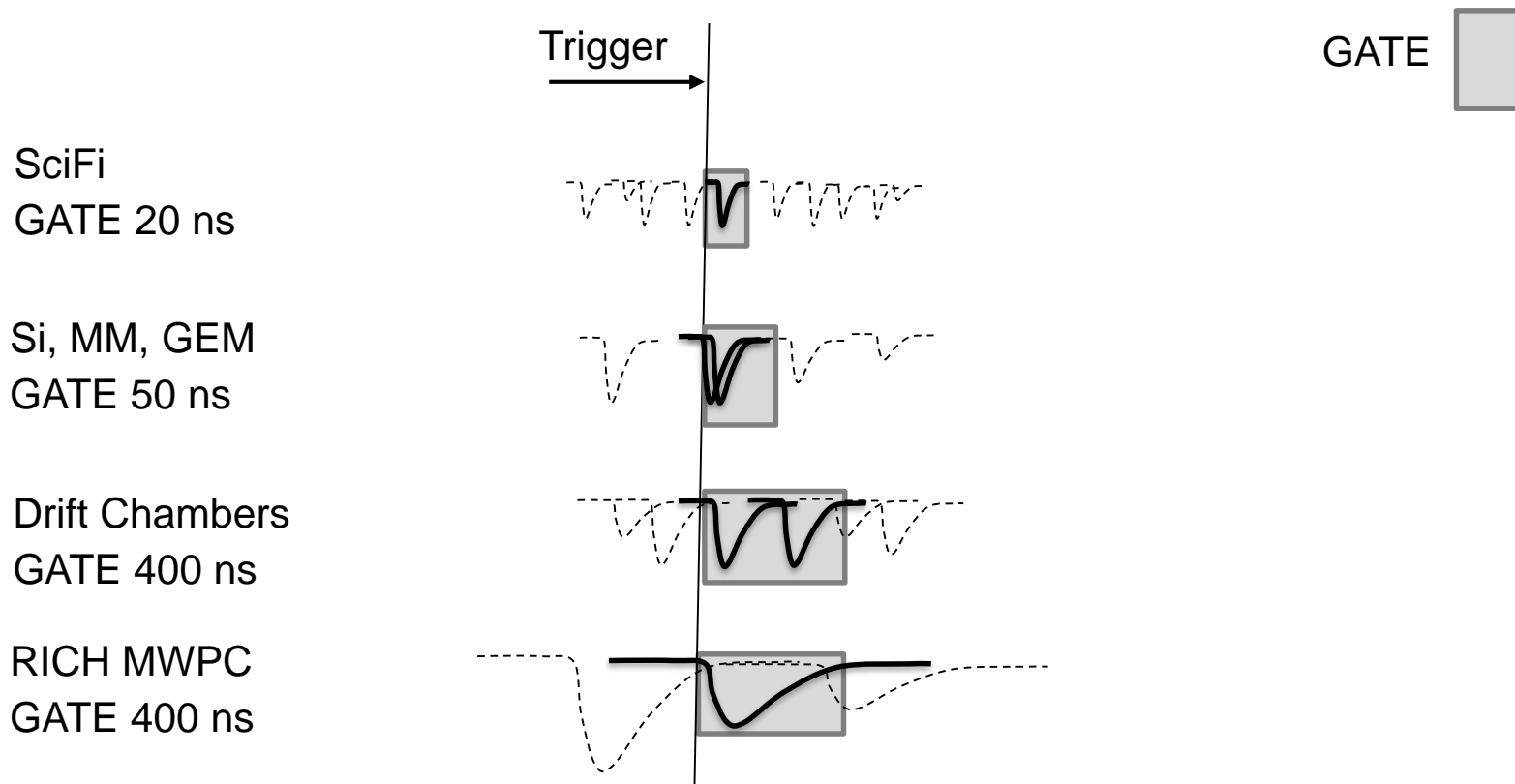
- HW trigger mutually exclusive with HLT
- HLT complementary to HW trigger

Tasks

- Concept of free running system
 - Data Structure, System architecture - OK
- Front-end electronics
 - MSADC, iFTDC, MuPix/Alpide, SISxx, VMM(?), TIGER(?) - only iFTDCs exist
- Feature extraction, data compression for ECAL
 - Fast MSADC readout - work started
- DAQ firmware development
 - DHmx, DHsw, Spill Buffer - new Spill buffer
 - TCS Controller - work in progress
- DAQ hardware
 - Kintex7 Ultrascale card - prototype produced
- Trigger processor
 - Hodoscope trigger - work in progress
 - Kink trigger - no man power
- DAQ Software
 - Software optimization to achieve maximum performance 1GB/s/PC - OK
- New Frame Work for Analysis software - being discussed

Free Running DAQ Data Structure

Data Structure of Standard Triggered DAQ



Data Structure of Trigger less DAQ before Trigger

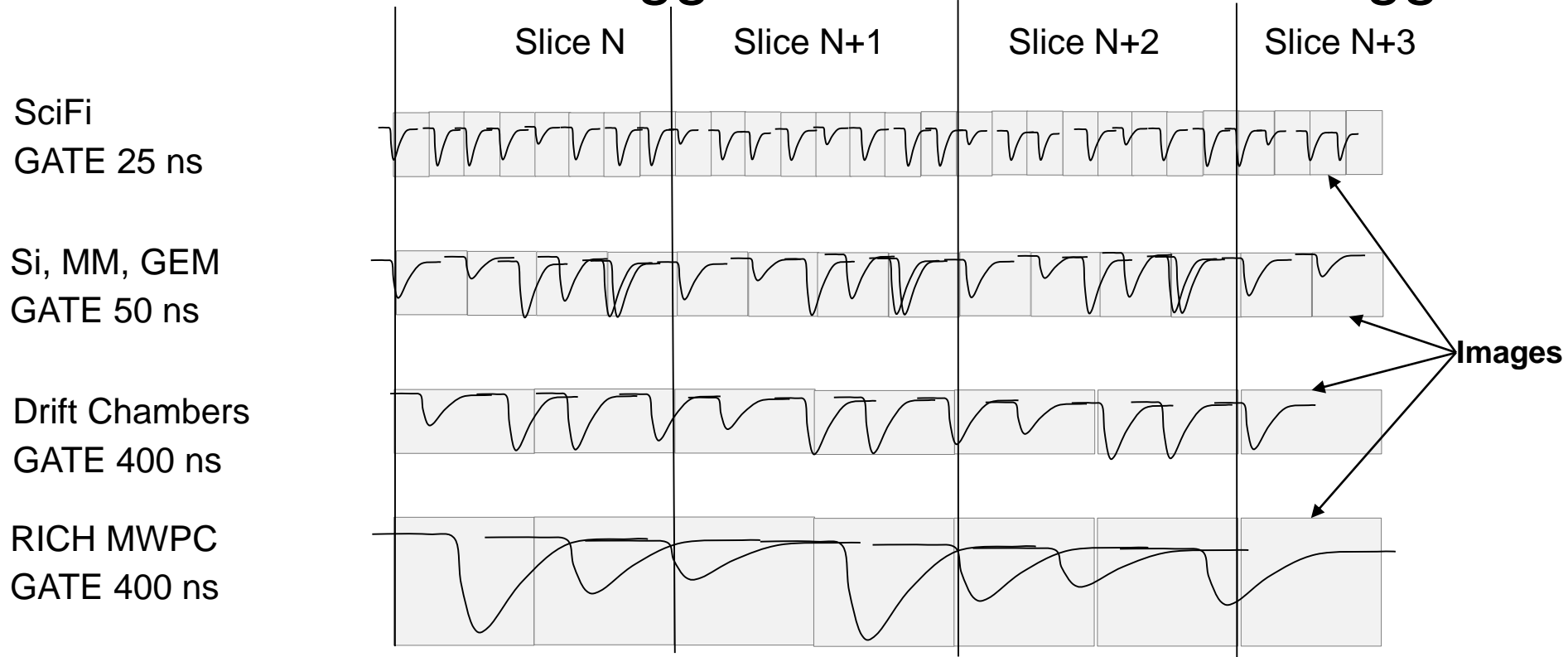
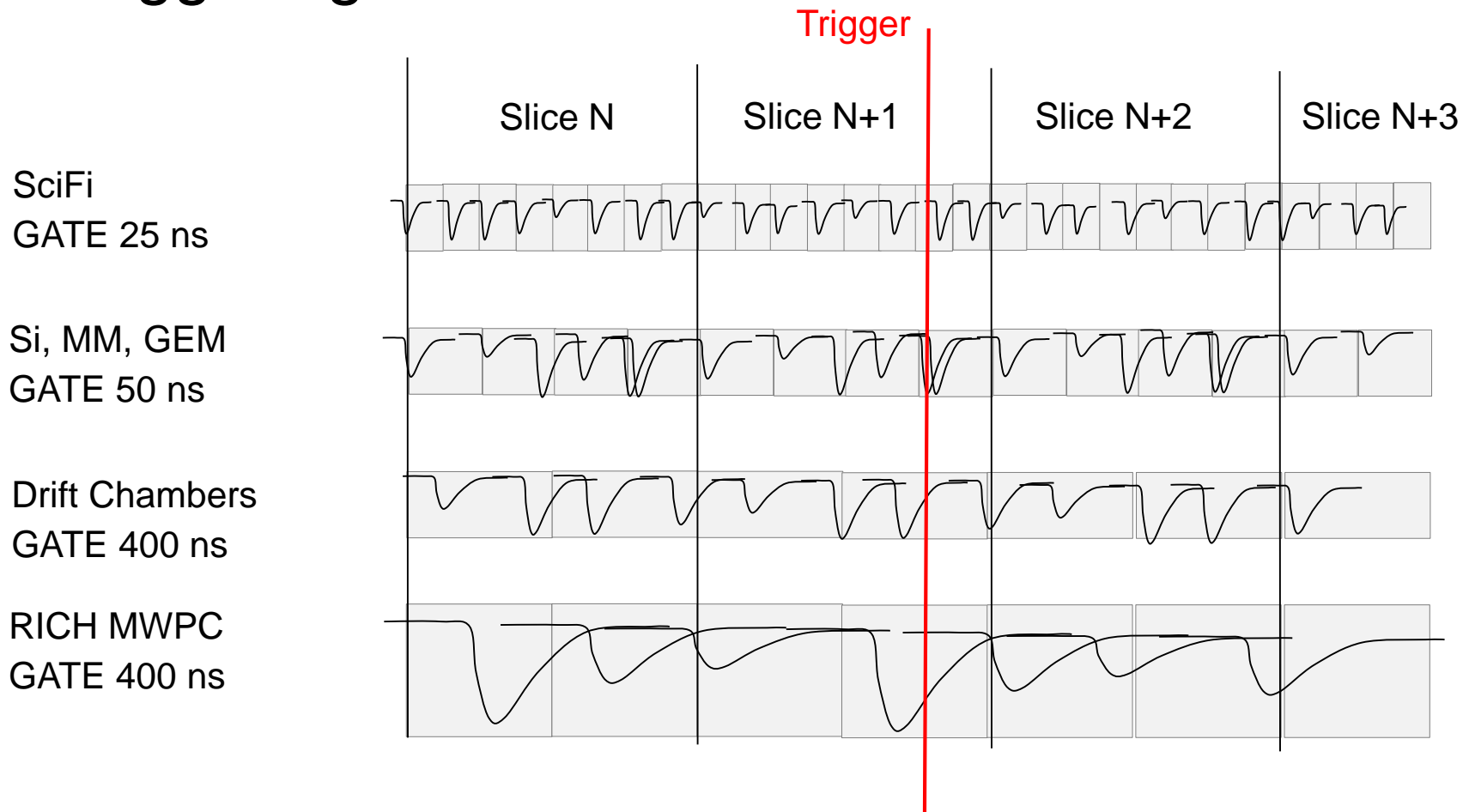


Image length optimized to minimize overhead and > 2 GATES

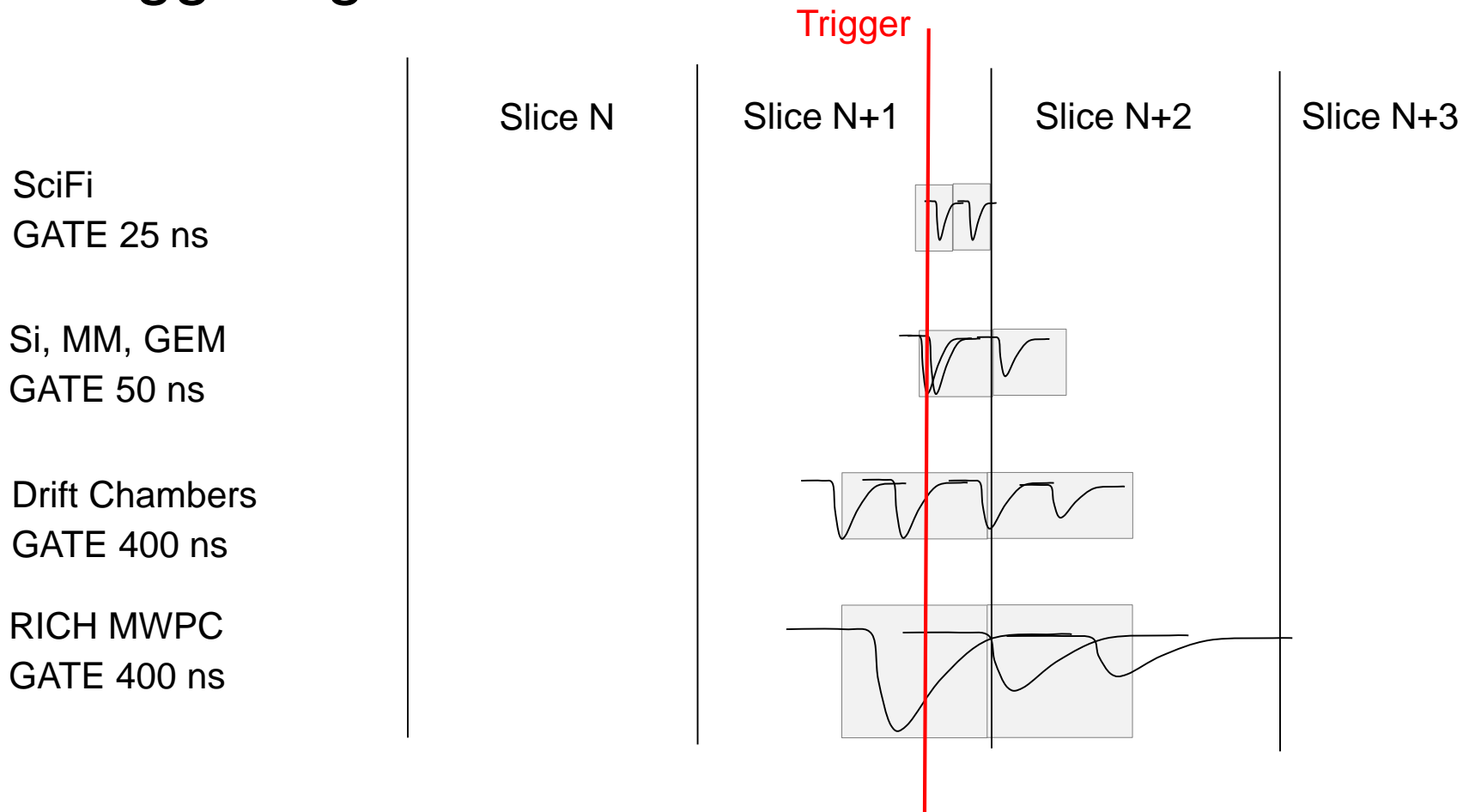
Example :

1. TPC drift time 60 us, TPC Image = 120 us
2. SciFi time resolution < 0.5 ns, SciFi Image = 100 ns

Triggering



Triggering



Two consecutive sub-slices are included in the event

Event Building Process

FEE

- Time sorted hits packed to IMAGES

DHmx first level

- Data buffering
- Organize hits plane wise
- Merging IMAGES belonging to one detector plane to new IMAGE
- Hits with IMAGE placed chronologically

DHmx second level

- Data buffering
- Merging SLICES: Multiplexing IMAGES in chronological manner, IMAGES keep format

DHsw

- Multiplexing SLICES with identical TIME TAG to single Servers
- Round Robin distribution of SLICES between Servers

Spill Buffer

- Data buffering
- DMA to Server memory

Data Rates wo Trigger

In spill :

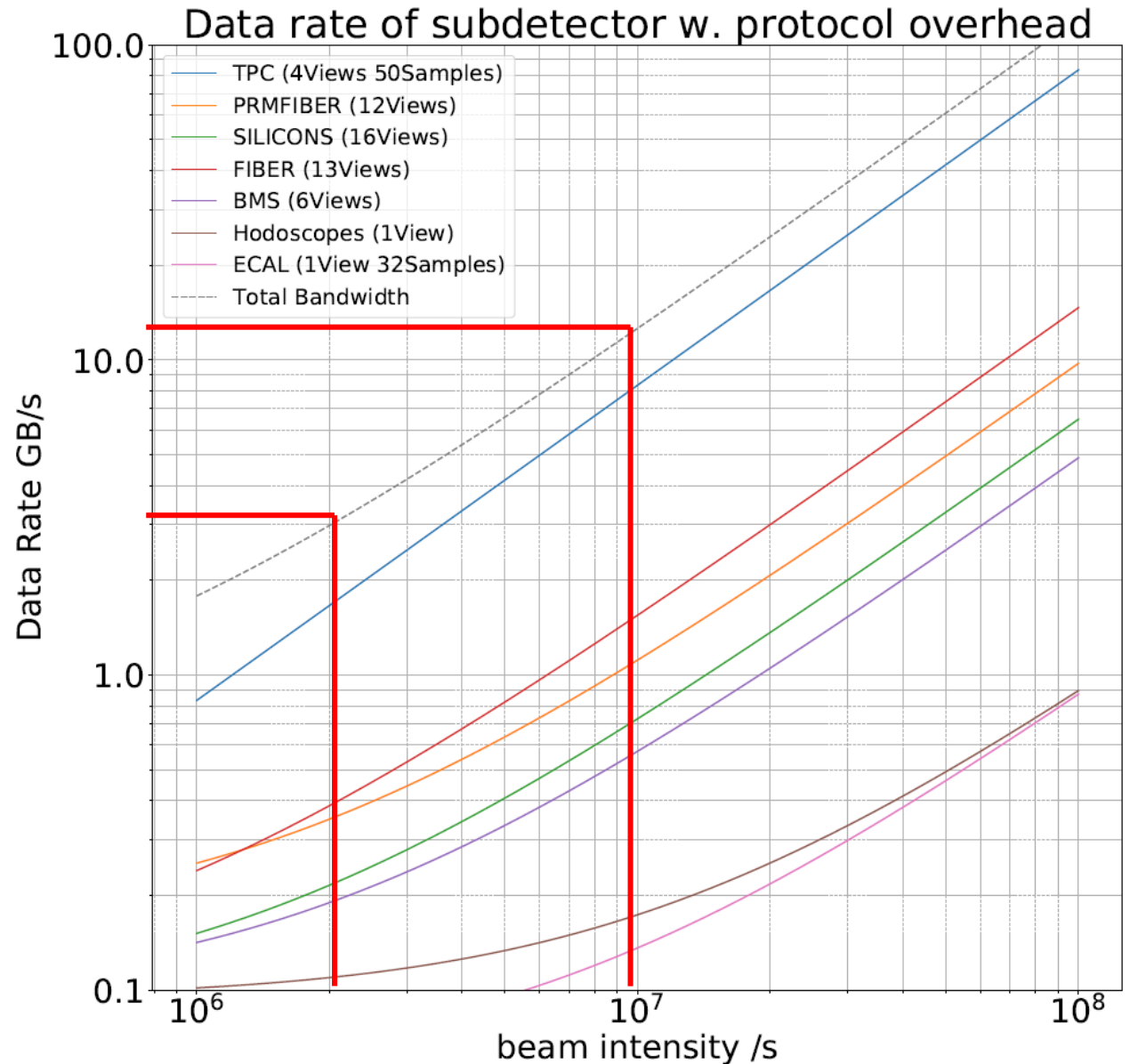
Beam 2 $10^6 \Rightarrow 3\text{GB/s}$

Beam 10 $10^7 \Rightarrow 10\text{GB/s}$

Sustained data rate:

Beam 2 $10^6 \Rightarrow 1\text{GB/s}$

Beam 10 $10^7 \Rightarrow 3\text{GB/s}$



Example of Detectors' Readout for PRM

PRM SciFi (4500 channels), 0.35-1GB/s

FE: NINO=> 70x iFTDC(A7) => 6 x DHmx(V6) => 2x DHmx(V6) => Switch P0,1

SciFi (800 channels), 0.4-1.5 GB/s

FE: NINO=> 30x iFTDC(A7) => 3 x DHmx(V6) => 2x DHmx(V6) => Switch P 2,3

H5 (64 channels), 0.1-0.2 GB/s

FE: NINO=> 2x iFTDC(A7) => DHmx(V6) => shared

BMS (512 channels), 0.2-0.6 GB/s

FE: NINO=> 16xiFTDC(A7) => 2 x DHmx(V6) => 1x DHmx(V6) => Switch P 4

PixSil (256 HS links), 0.2-0.7 GB/s

MuPix/Alpide => 32xFE(K7) => 3 x DHmx => 1x DHmx(V6) => Switch P 5

TPC, 1.7-8GB/s (no zero suppression)?

SISxx => ? => Switch P 6, 7

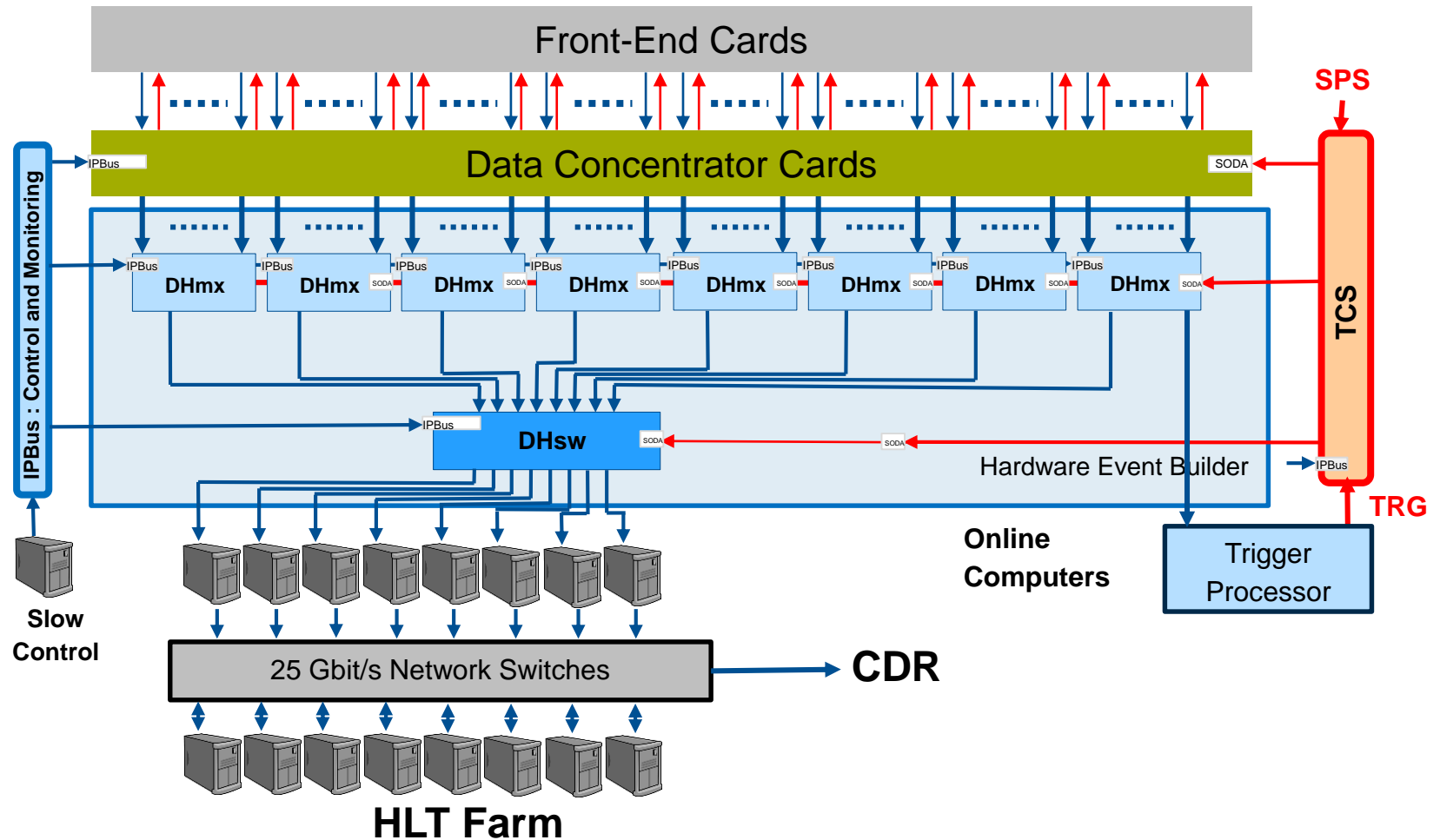
ECAL (100 channels), 0.05-0.15GB/s

MSADC => ?? => DHmx(V6) => shared

GEM

??

iFDAQ Architecture



Challenges of Free Running DAQ

- High data rate capability
 - 4 GB/s with V6 switch
 - 30 GB/s with Kintex 7 switch
- Provision of online alignment for triggering or HLT
- Developing trigger algorithms and trigger emulation
- Analysis software for new data format

THANK YOU