New Event Builder Algorithm

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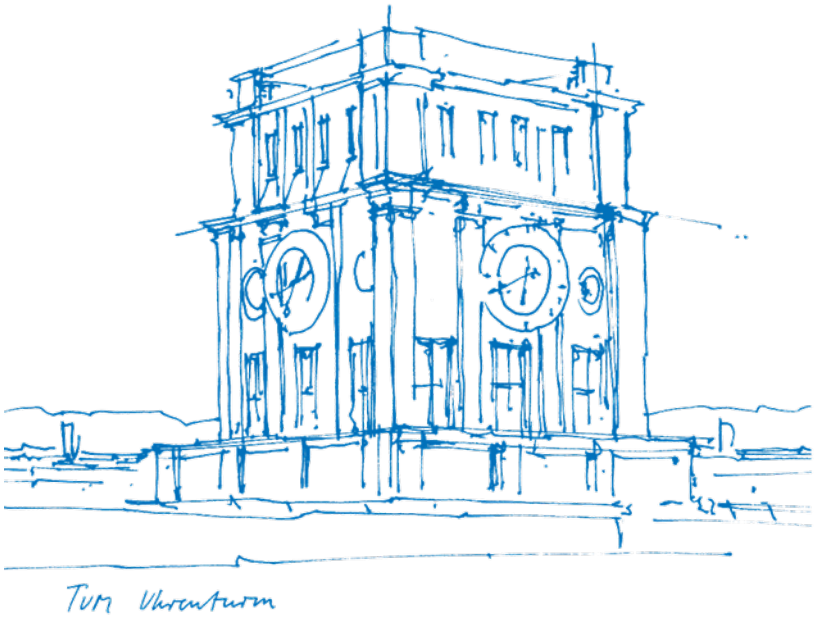
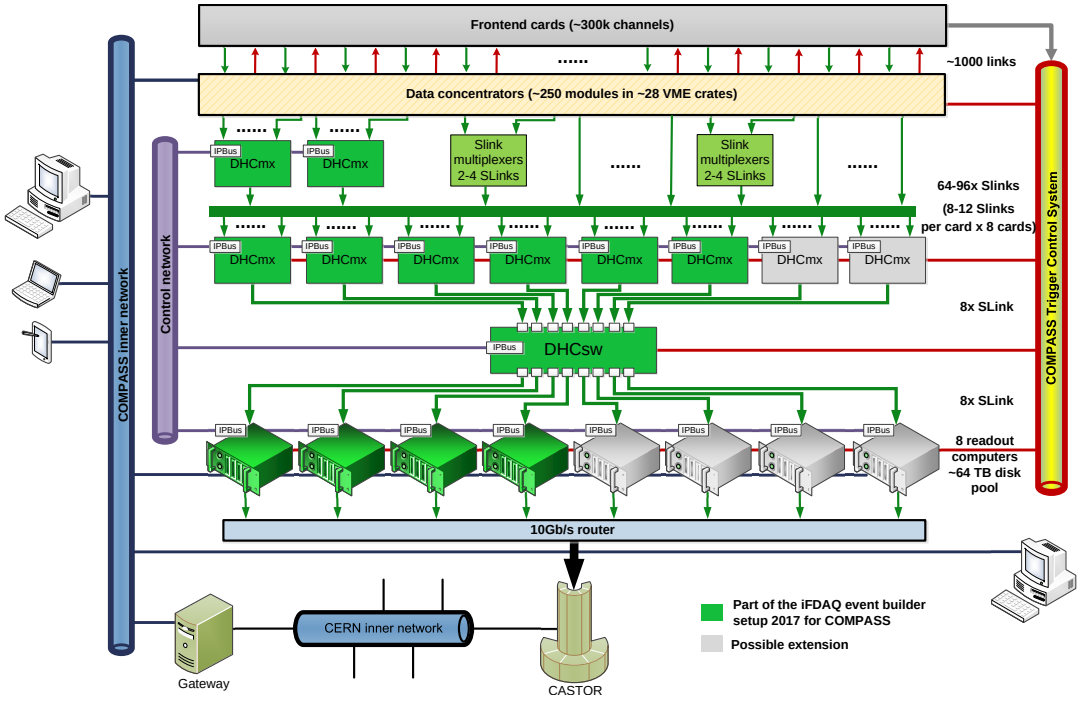
COMPASS Front-End, Trigger, and DAQ Workshop

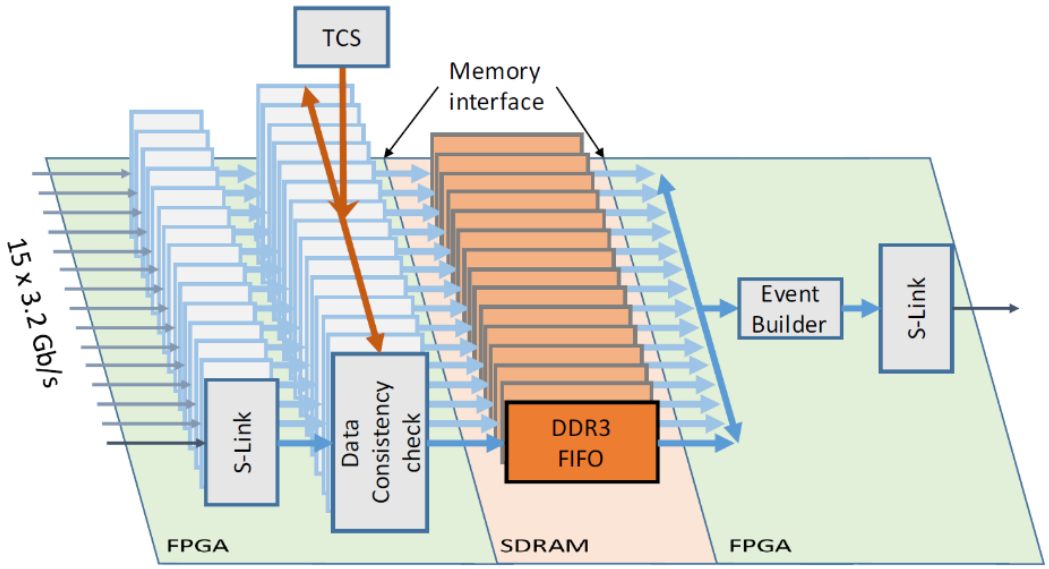


Current Event Builder Architecture



- Event builder
  - FPGA-based
  - events stored in external memory

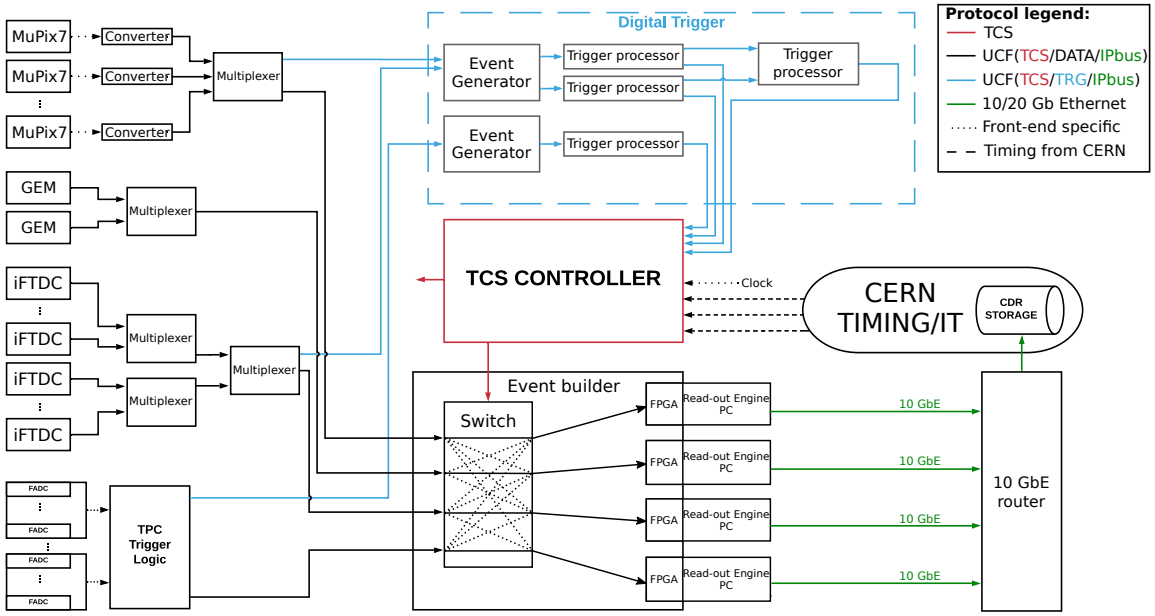
Current Event Builder Architecture



- Event builder
  - FPGA-based
  - events stored in external memory
- Memory throughput 3 GB/s
  - limits performance of the event builder
  - all events in the event builder

  $\Rightarrow$ not easy scalable

New Event Builder Algorithm



- **Pre-sort events** before event building
  - events routed to the same event builder
  - ⇒ increases number of event builders

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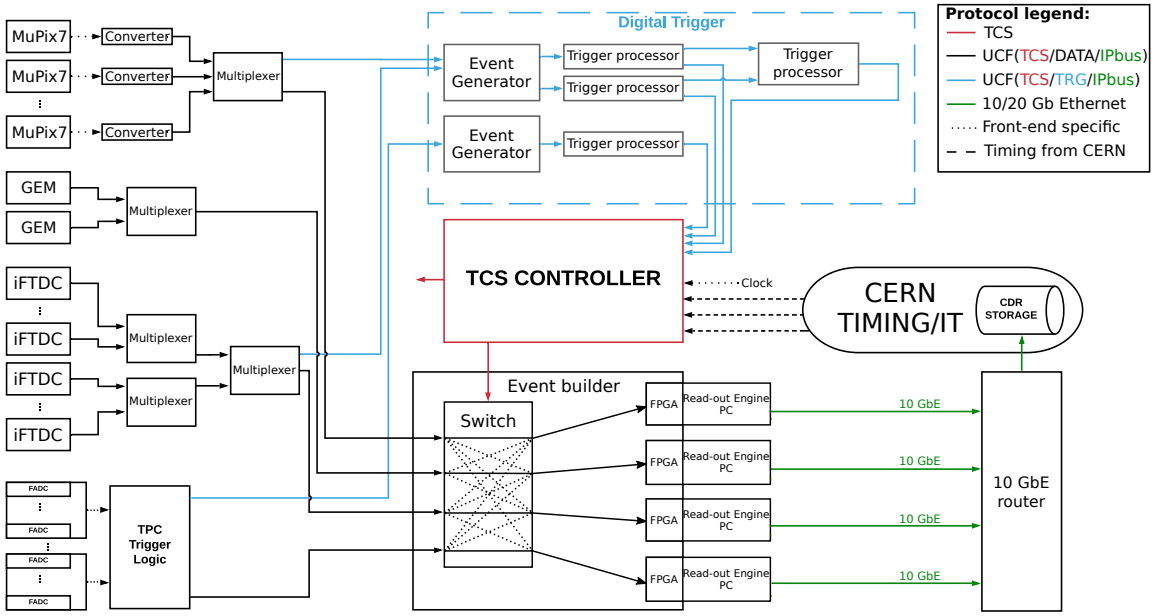
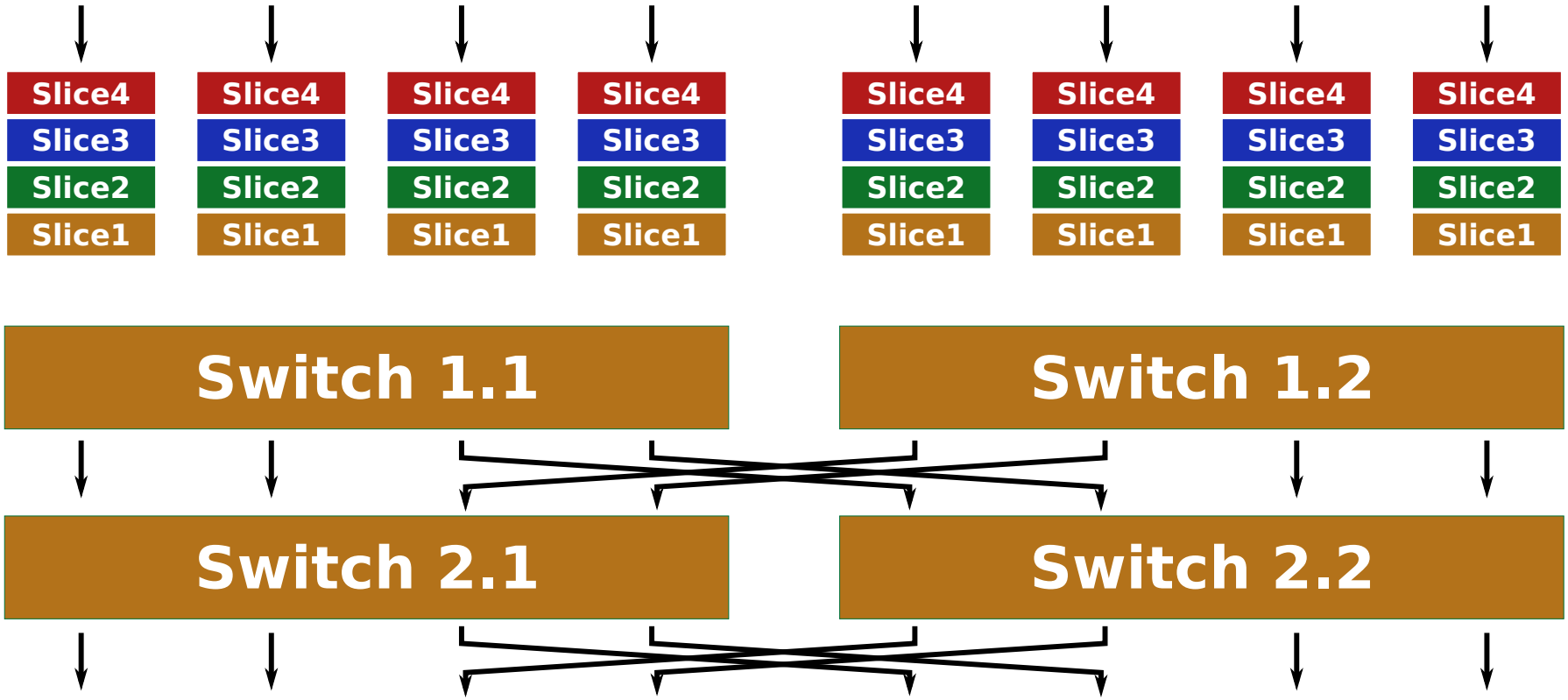


- **Pre-sort events** before event building
  - events routed to the same event builder
    - ⇒ increases number of event builders
- N-to-N switch in FPGA fabric
  - no external memory for data
  - **timeslice-based readout**
    - events
    - data frames

Switch Algorithm



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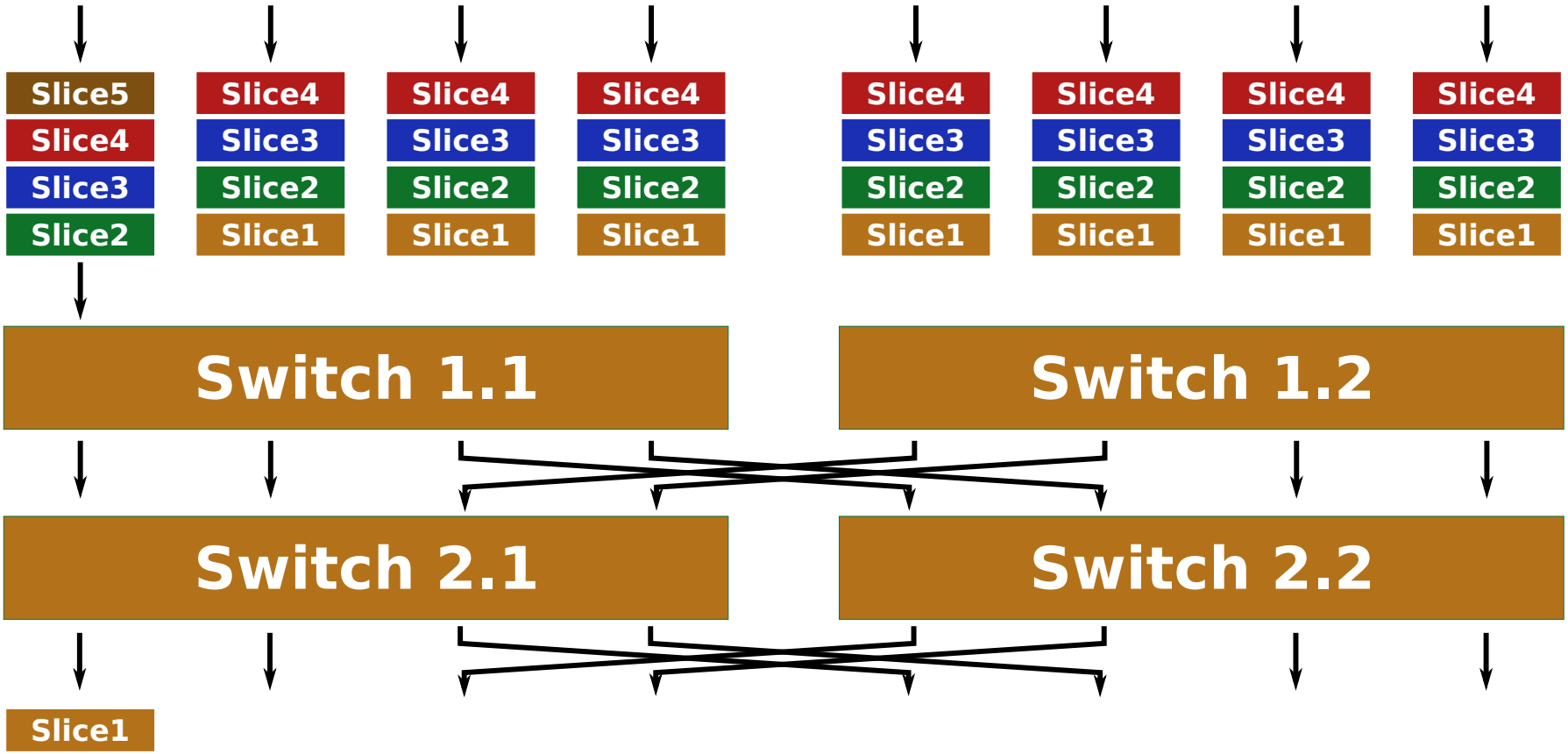

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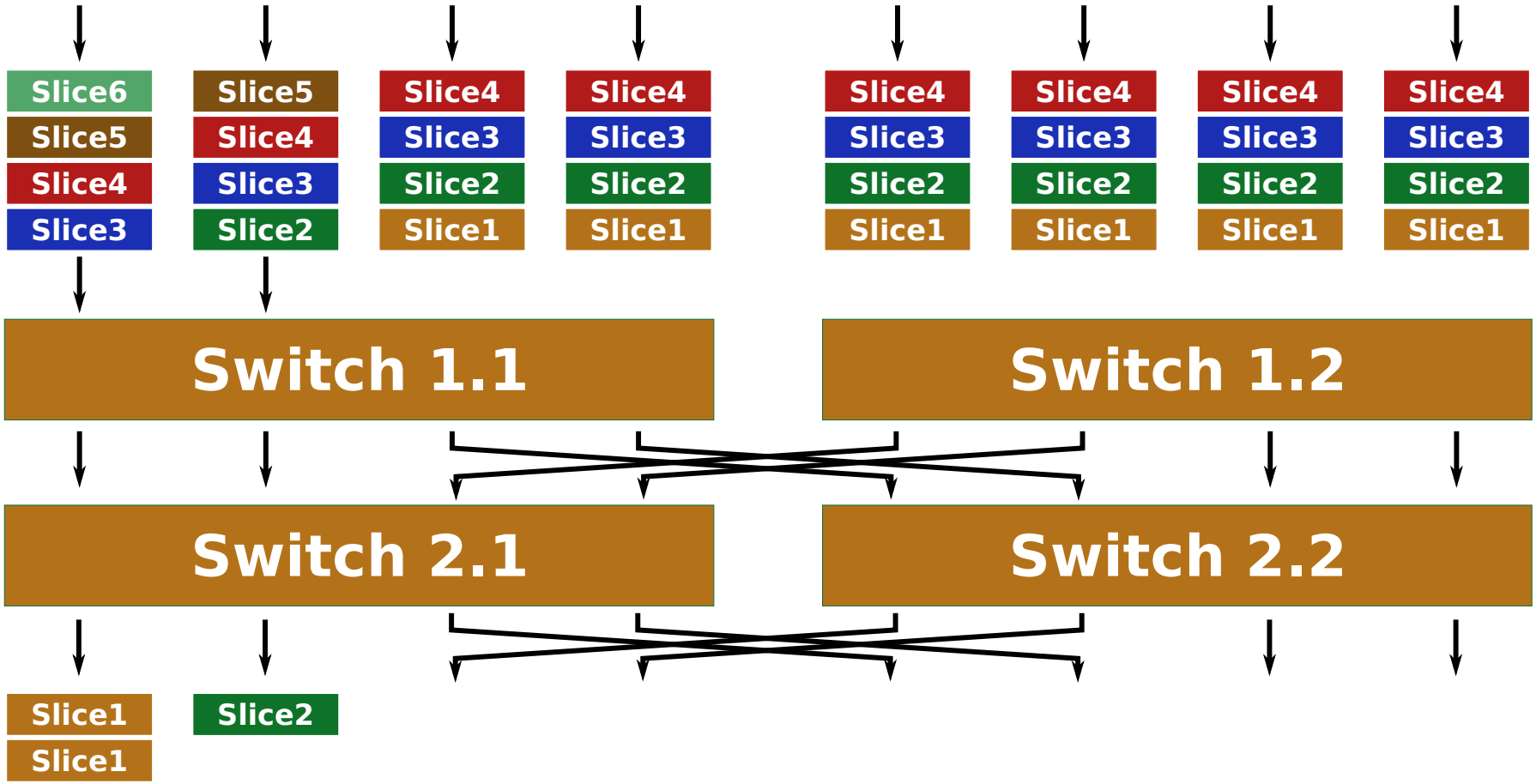

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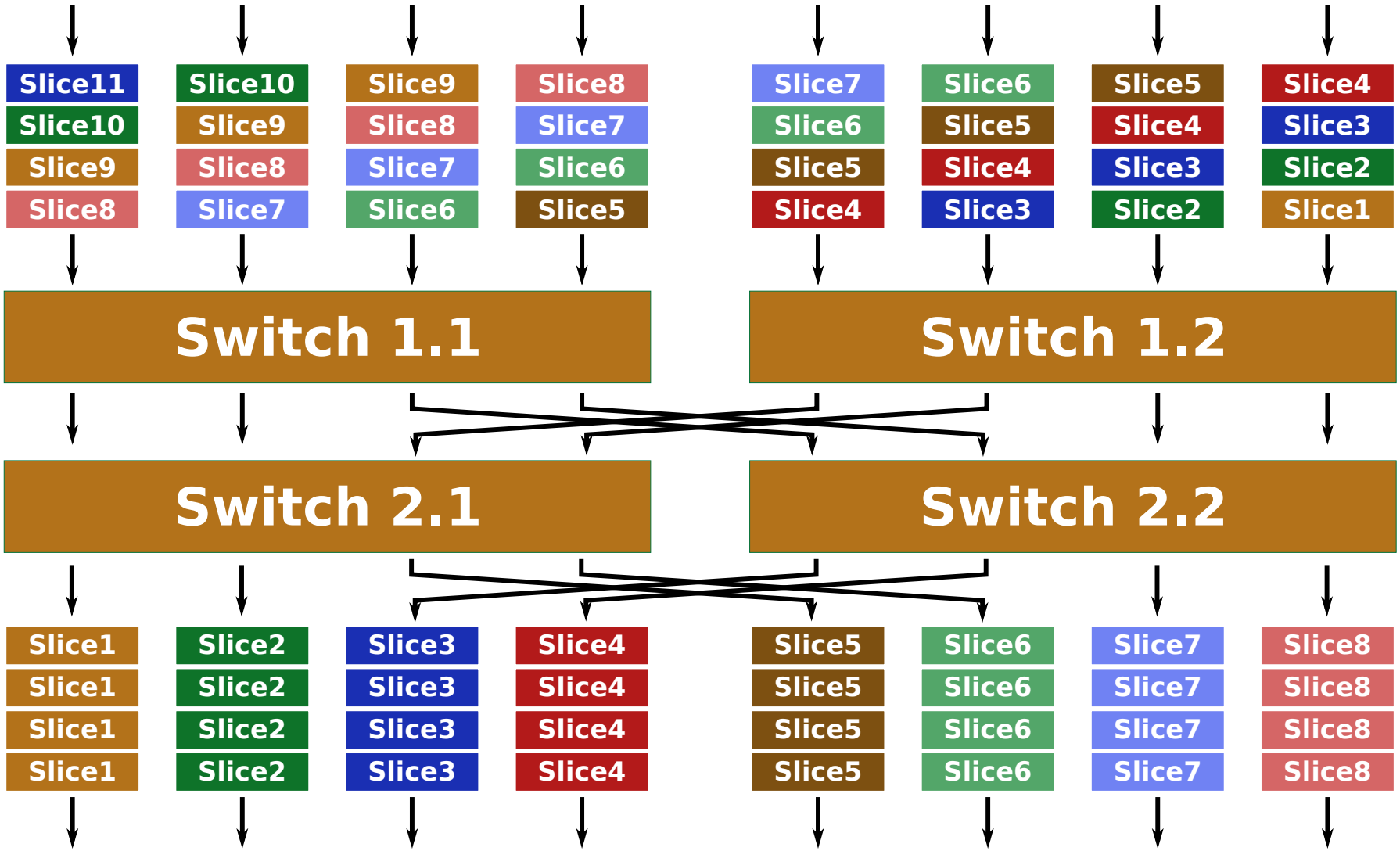
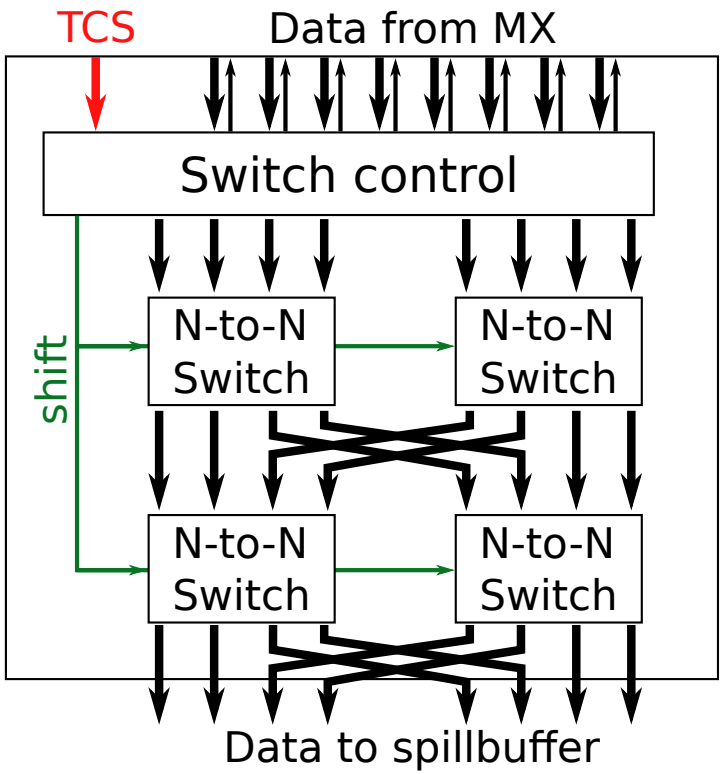
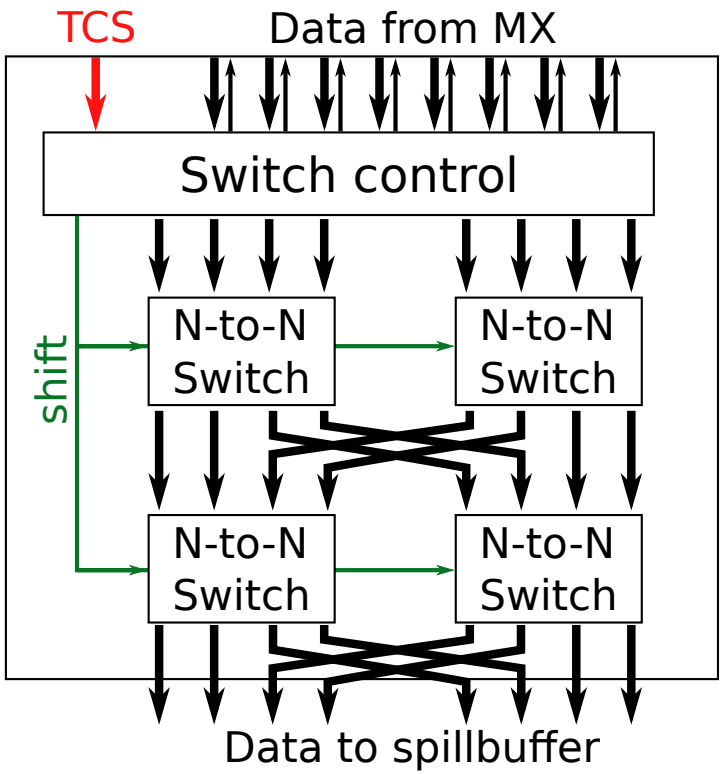


Switch Architecture



- Switch control
  - initiates change of the switch configuration if
    - all events/frames in a given timeslice transmitted
  - **deep FIFO** for storing trigger information
  - **backpreassure** to the MX cards

Switch Architecture



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  - routes frames from an input to a specific output
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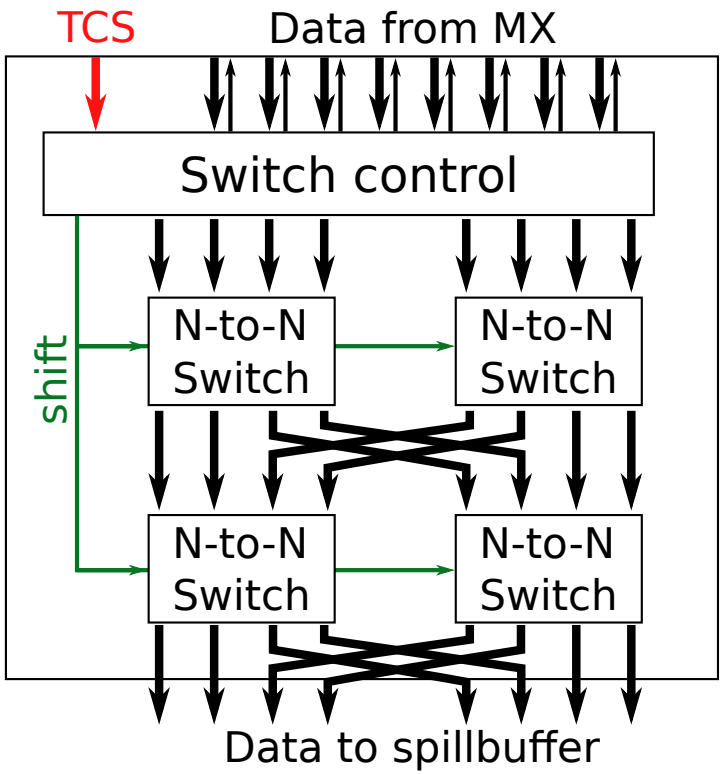

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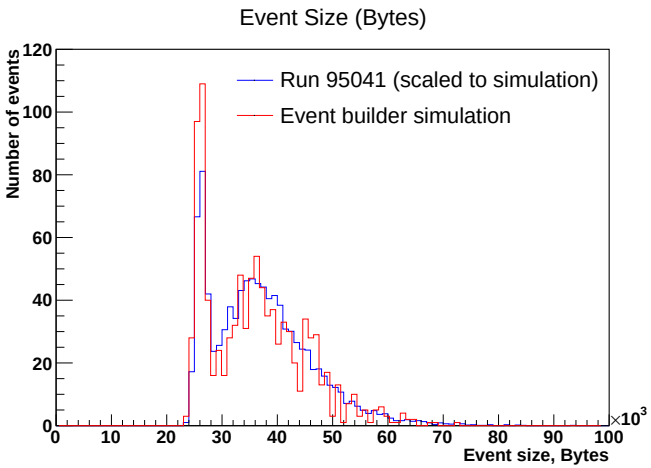
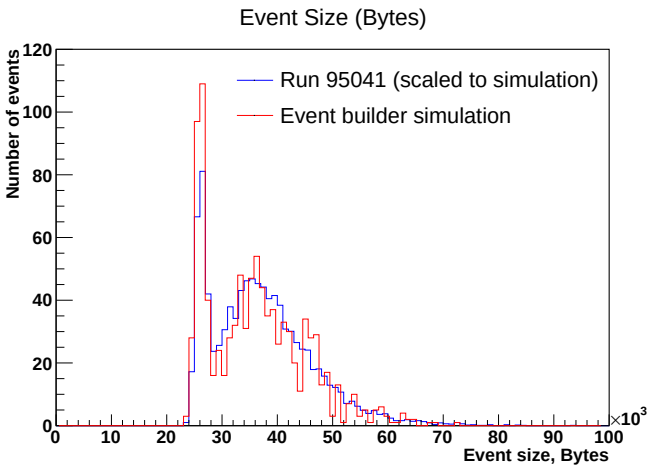
- configuration generation software
  - 32 configurations for 8x8 switch
  - uses graph theory to calculate configuration

Performance



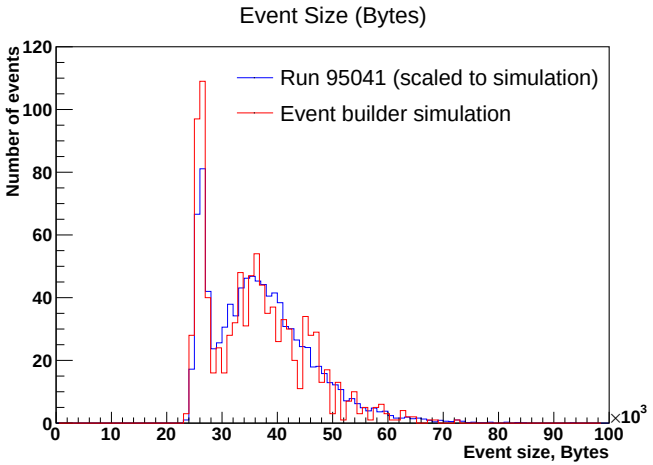
- Simulation of the **1000 events** with event size distribution as in the run 95014

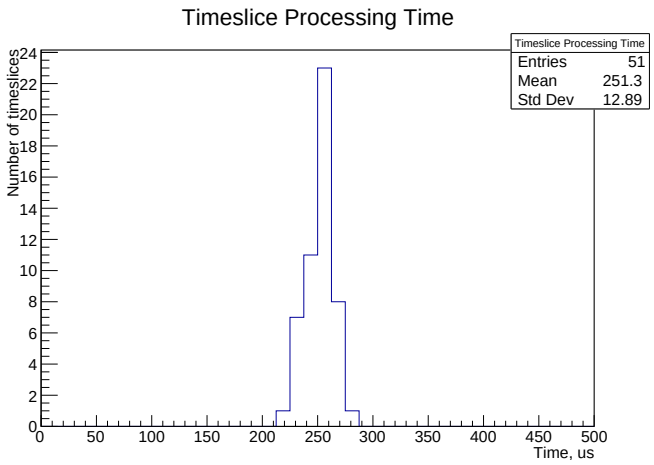
Performance



- Simulation of the **1000 events** with event size distribution as in the run 95014
- Assumptions:
  - only event size distribution is used
  - data already available in MX
  - **100 MHz clock; 4 Gbps link rate**
  - **40 kHz trigger rate**, Poisson distribution
  - timeslice period: **500 us**

Performance





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  - limited by the link bandwidth

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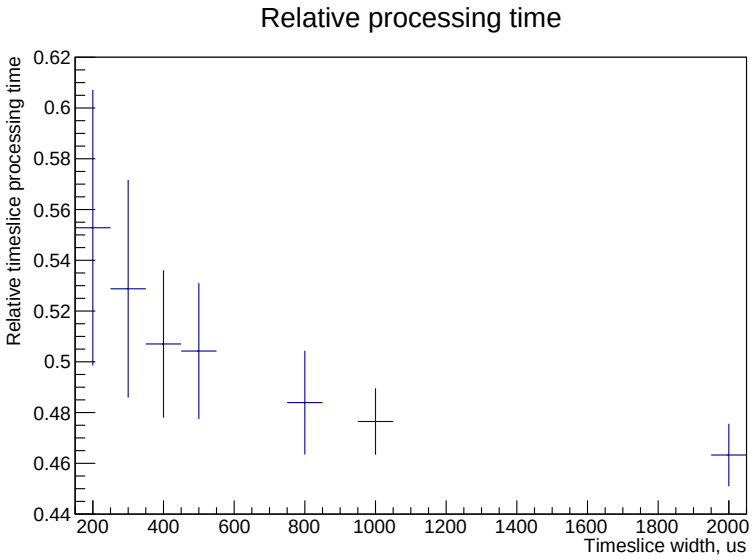

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- Relative processing time:
  - **decreases with increasing timeslice width**

Ressource Utilization

- Use modified CMX firmware
  - Virtex-6 VLX130T
  - 8 input S-links
  - 8 output S-links
  - **switch core** instead of EB, or **input to output connection**

Ressource	With switch, %	Without switch, %	Difference, %
LUT	24	21	3
FF	14	12	2
BRAM (36E1)	21	3	18

Summary

- First implementation of the algorithm
  - work in progress
  - data format decoder
  - TCS decoder
  - DDR3 FIFO for TCS data
- Preformance depends on
  - link data rate
  - timeslice width
- Low ressource utilization
- Full implementation until the dry run