MSADC to FMC adapter board, and FPGA firmware

Luis G. García O.

ICTP-MLAB/UNITS/INFN-TS
COMPASS-TS GROUP

COMPASS Front-End, Trigger and DAQ Workshop, 2-3 March 2020

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

Towards Trigerless system

Motivation

Moving towards a free running DAQ requires to adapt the original MSADC-FPGA design (ECAL2) to provide a continuous data stream from the analog channels.
This fast MSADC readout should provide continuous data streams for experimentation on online feature extraction and data compression.
An interposer board was designed to facilitate the communication between the MSADC board and multiple commercial FPGA-based carriers that use a standard FMC (ANSI/VITA 57.1) connector.

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

MSADC Board

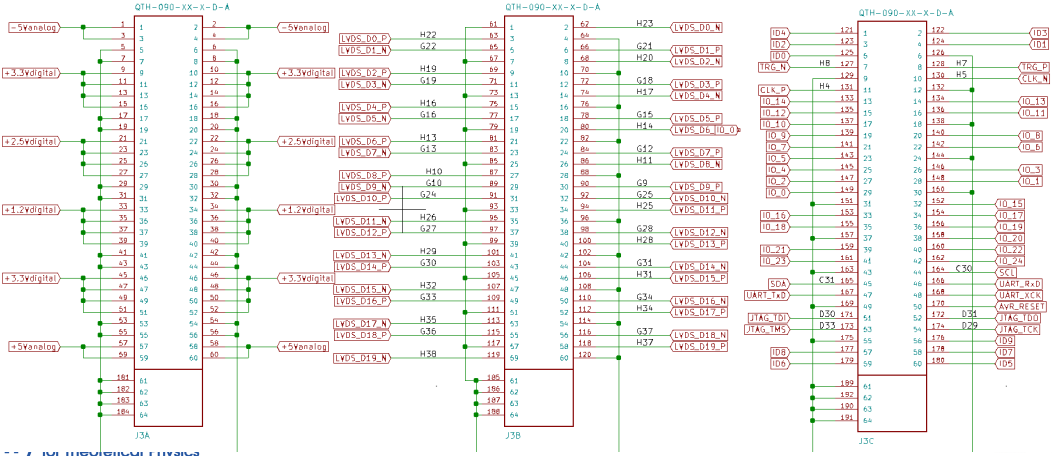
Features:

- 16 analog channels ADC board (12 bits, 80 MHZ)
- 4 x TI ADS5270 (32 logic channels @ 40MHz)
- Virtex 4 FPGA
- QSH-90 High Speed connector
- 6 Voltage power domains.
  - $\pm$5V analog
  - +3V analog/digital
  - +1.2 V digital

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

QSH-90 Connector Pin Mapping



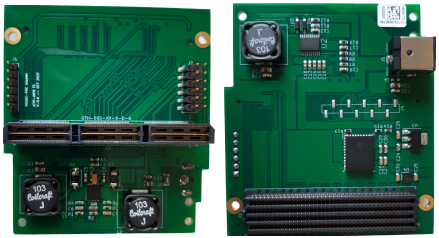
QSH-90 Connector Configuration

- 12 pins for Analog and Digital Voltage Inputs.
- 20 High speed LVDS I/O Interface
- Auxiliary I/O Connector
  - JTAG Programming lines
  - UART Rx/Tx Signals
  - 25 I/O Signals
  - CLK, TRIG, SPI and ID.

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

MSADC to FMC adapter board



Features

- 9V @ 3A input voltage
- Full mapped QTH-090-04-F-D (Qstrip) Connector
- ASP-134602-01 ANSI/VITA 57.1 (FMC).
- Power supply for the MSADC Board in six voltage domains.
- JTAG chain programming through FMC connector.
- UART Tx/RX pins.

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

MSADC to FMC Carrier Examples

CIAA-ACC (Zynq 7030)

ZCU102 Board (Zynq Ultrascale+)

MSADC Readout system for single channel data analysis

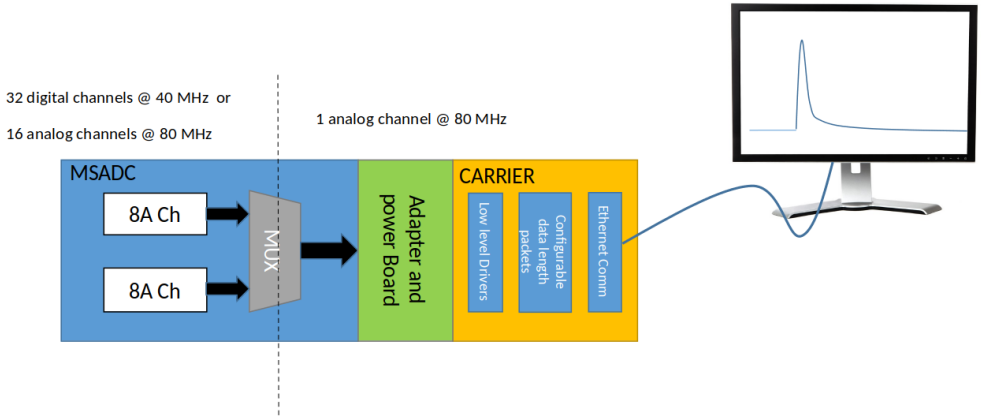
Characteristics

- Long traces retrieval required for data analysis
- Continuous data stream from the MSADC, on selected channel.
- Ethernet communication to transmit the data stream
- GUI for remote control and data visualization and storage.
- Built in test on MSADC to verify functionality.

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

MSADC Firmware Modifications and Carrier Board development



Carrier firmware and software characteristics

Carrier Design (Firmware/Hardware)

- Programmable frequency clock output
- System reset generator
- Multi-platform portable design
- Online programmable data length packets
- PC interface protocol for configuration and data transmission

PC Software Interface

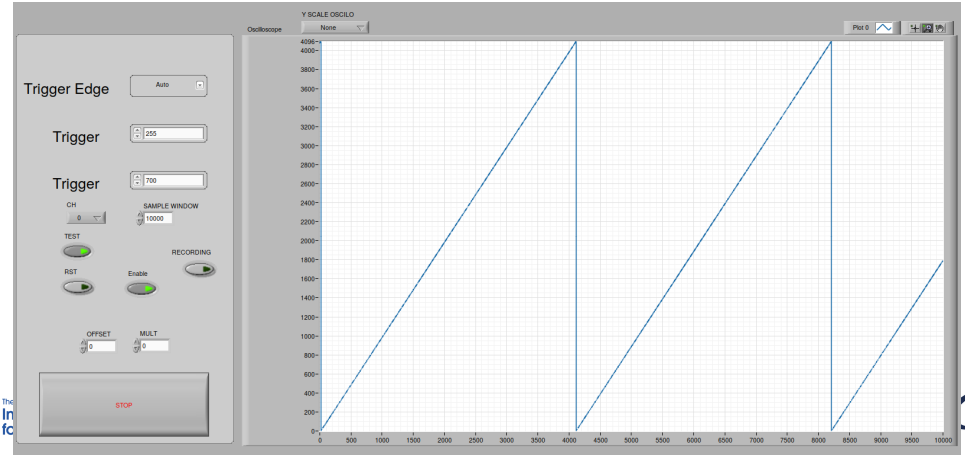
- Channel selection
- Test mode available and data visualization.
- Selectable trigger mode
- Configurable Ethernet communication parameters

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

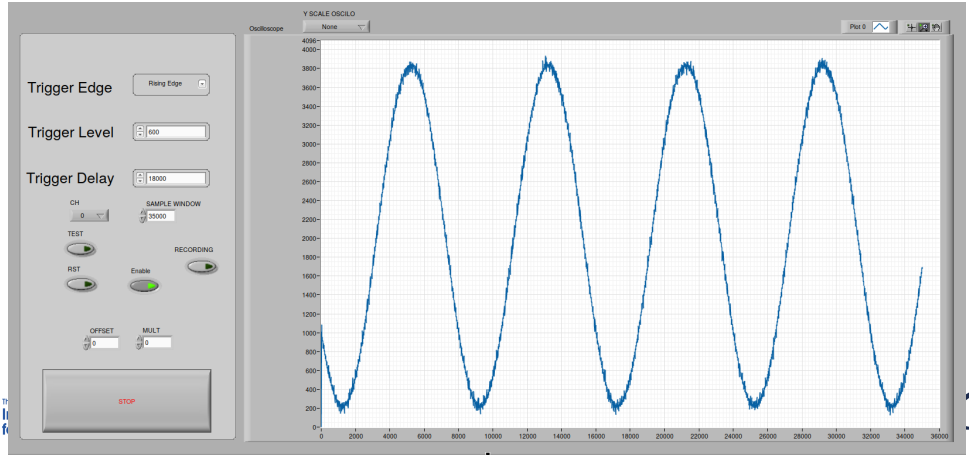
Test Results

Test signal generated from the MSADC readout and stored.

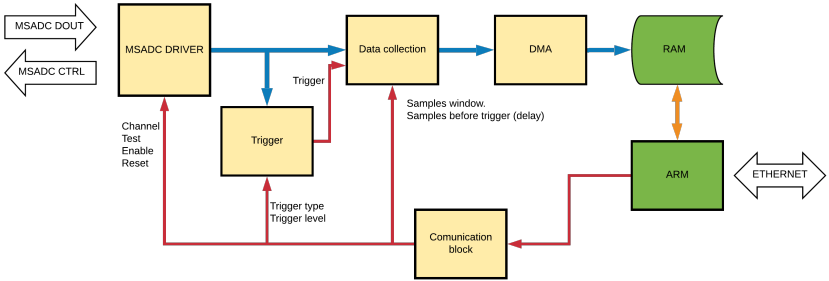


Test Results

MSADC Readout with external signal stimulation.



Carrier FPGA design block diagram



The Abdus Salam International Centre for Theoretical Physics

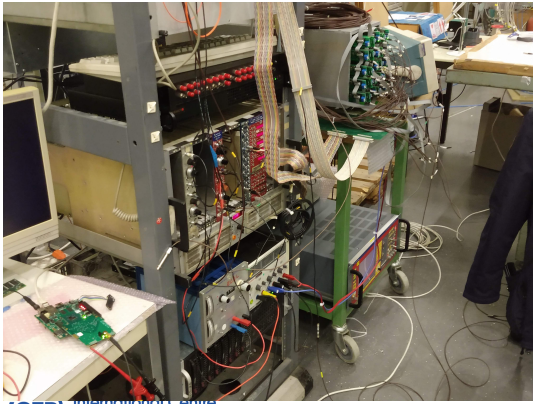
INFN TRIESTE

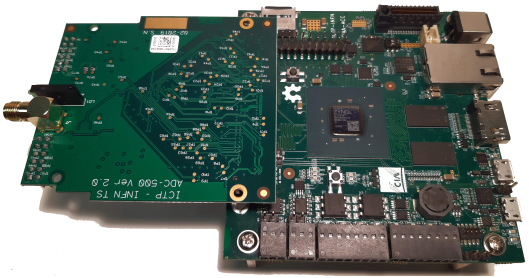
Long trace data acquisition for noise characterization on ECAL 2 for optimized feature extraction with ICPT-INFN ADC500

The Abdus Salam International Centre for Theoretical Physics

INFN TRIESTE

Long trace data acquisition for noise characterization on ECAL 2 for optimized feature extraction





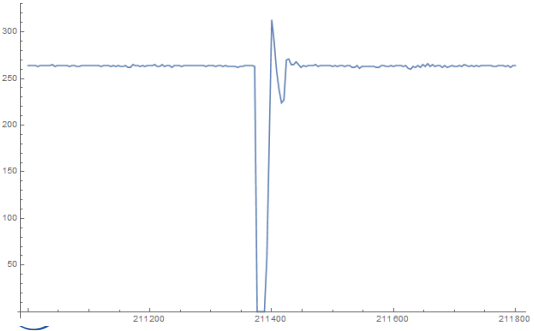
ICTP International Centre for Theoretical Physics

INFN TRIESTE

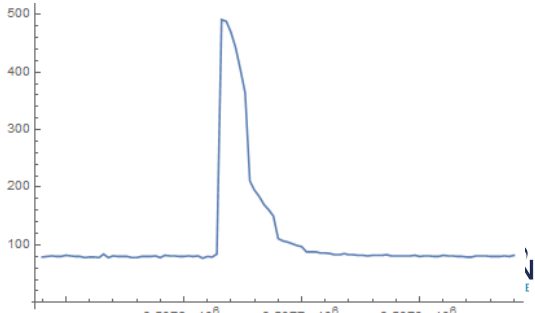
ECAL2 data acquisition test

- ADC 500 (8 bits @ 500 MHz)
- 32,000 decimated by two samples (8+1 bits @ 250 Mhz)
- 320 mV ($\pm$ 160 mv) dynamic range.

Before pulse shaper



After pulse shaper



Thanks for your time.