CHIPS: CERN-HEP IC design Platform & Services

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ASICs for HL-LHC Upgrades

- List of ASICs for the upgrade programmes

ALICE (and NA62)
SAMPA, ALPIDE, FEERIC, Non-LHC, TDCpix (NA62)
LHCb
VELO – VeloPix, Upstream Tracker – SALT, RICH – CLARO, SciFi – PACIFIC, CALO – ICECAL, MUON - nSYNC
ATLAS
ITK Pixel, ITK strips, Lar Calorimeter, HGTD, Muon NSW, Muon MDT, Muon TGC, Muon RPC, Trigger-DAQ
CMS
GEM VFAT3, OT CBC, OT CIC, OT MPA, OT SSA, EB CATIA, EB LITE-DTU, IT ROC, EC Si ROC (HGCROC, H2GCROC), EC TCON, ECON, DCON, EC LDO, BTL TOFHIR, BTL ALDO2, ETL ETROC, CMS CFO
CERN common ASICs
lpGBT, LDQ10, lpGBTIA, GBTX, GBT-SCA, GBLD, GBTIA, FEAST2, bPOL12V, bPOL2V5, linPOL12V, RD53

ASIC design Challenges

- 67 ASICs are being developed (21 in ATLAS)
  - Most of them comply with development schedules
  - Many were delayed or required multiple prototyping iterations
  - Few are problematic and might have serious repercussions on the physics programs of the experiments

- The CERN SPC[1] highlighted at its December 2018 meeting (among other things) the challenges associated with ASIC developments in the HEP community and *asked for a coherent plan for dealing with these problems*

- What primarily emerged, is that the complexity of the CMOS processes being used is high and will increase in the future and along with that the complexity of our designs

[1]SPC: Scientific Policy Committee
an advisory body to CERN council
https://council.web.cern.ch/en/content/welcome-scientific-policy-committee

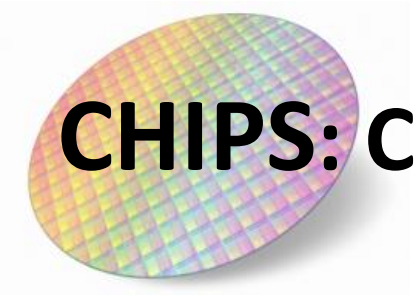
Facing the Challenges

- The ***Digital on Top design implementation*** and ***System Level Verification methodologies*** must be adopted systematically to avoid expensive and time-consuming errors even if this implies a significant increase in design time and resources

- The layout of analog blocks for ***radiation hardness*** (and Single Event Upset resilience) becomes increasingly challenging and deep expertise is required

- As the design ***community remains geographically scattered and smaller groups*** may struggle to cope with the new design flows CERN could strengthen training and support

New Support Service



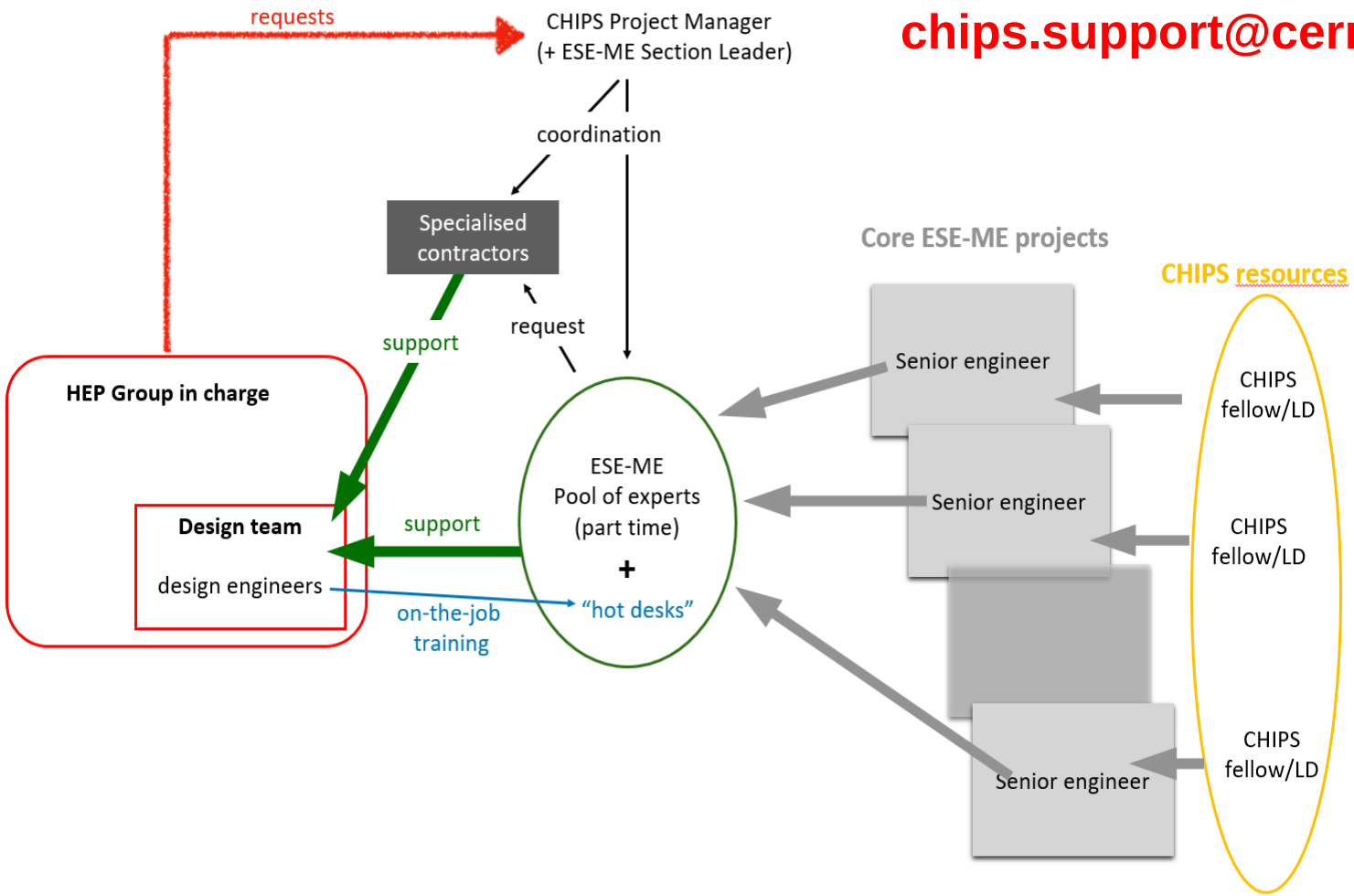
CHIPS: CERN-HEP IC design Platform & Services

- Strengthening Foundry Services and Technical Support in CERN EP-ESE-ME
- Meeting the challenges of present and future CMOS designs in the HEP community and at CERN
- Announced to the HEP community at the MUG meeting at TWEPP 2019
- Officially active since January 2020

CHIPS Action Plan

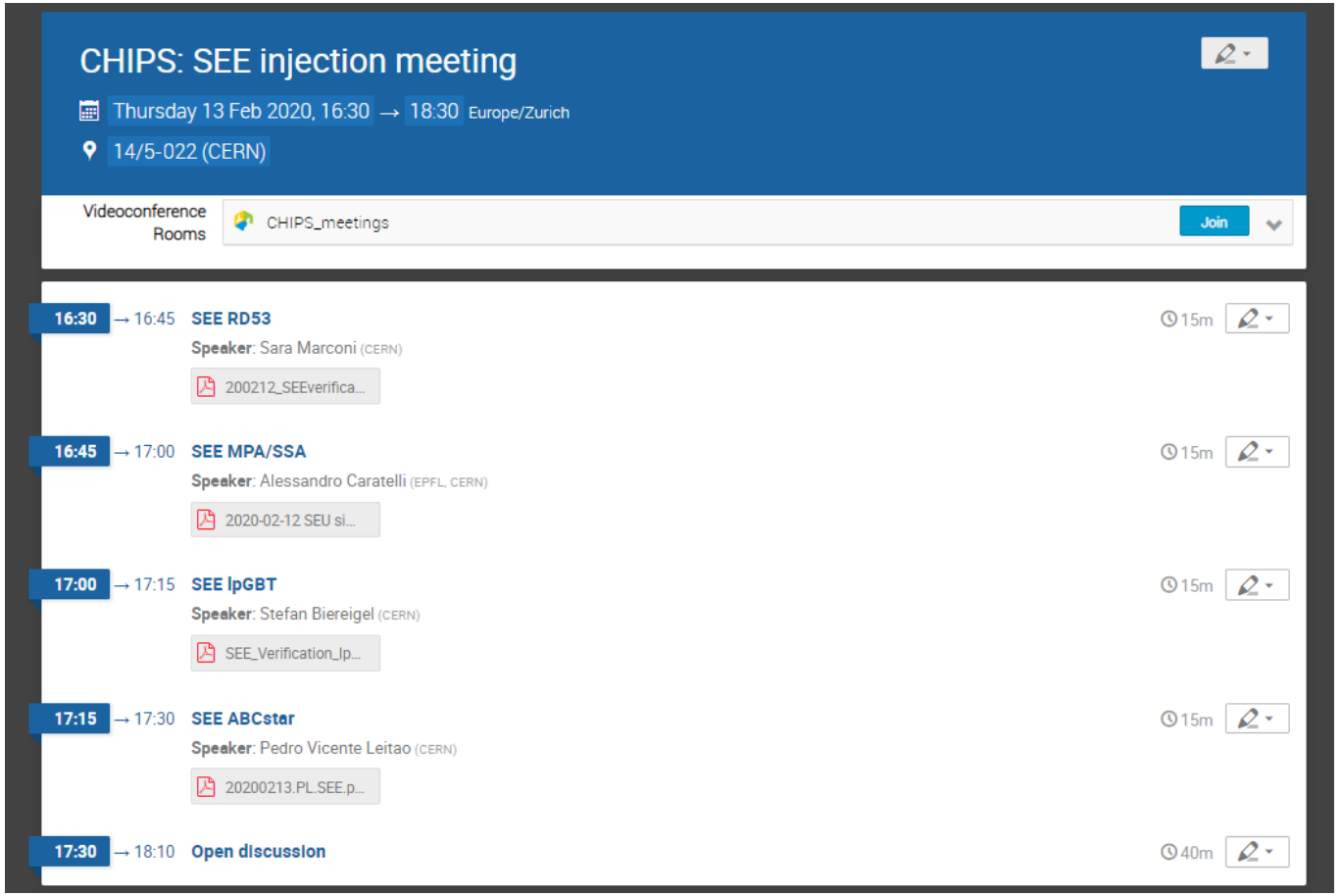
1) **Involve a broader spectrum of experienced practitioners in design support:**
   - At present a small core team in EP-ESE-ME provides support. It is proposed to redistribute the technical support tasks more uniformly across the experienced designers in EP-ESE-ME. For each step in the design flow one or two specialists will be identified and these will be tasked with supporting outside groups. Such support can only be provided by experienced practitioners
2) **Subcontract specialised tasks:**
   - Reinforce contracts with companies able to give punctual help with particular issues related to the tools and design flow. These facilities should be available both to CERN engineers and to members of the community. As with all such external contracts there should be one person responsible (of course with a back-up) to act as intermediary between the company and the designers
3) **Train and coach:**
   - Continue to organize formal training sessions to expose designers to the latest tools and, in particular, to educate them in the use of the common design platform.
   - Furthermore, host designers from the HEP community at CERN in each case for some months per year. Some ‘hot desks’ could be allocated for such activities

CHIPS Organization



chips.support@cern.ch

CHIPS service for CMS-HGCAL



https://indico.cern.ch/event/888280/

CHIPS: Example ATLAS-ITK

- Started a “rolling” review (design support) process:
  - Accelerate interaction with design
  - Optimize the time dedicated by expert designers

- What’s the plan:
  - Have 1h long meetings every 1 or 2 weeks
  - Focused in a specific technical topic
  - Selected CERN design experts based on discussed topic

- What has been done so far:
  - 2 meetings to present the AMAC and HCCSTAR projects
  - 1 meeting to discussed the AMAC analog block
    - A follow up meeting (23rd April) with R. Ballabriga (CERN)
  - Planned TMRG tool meeting with S. Kulis (CERN)

Summary

- CHIPS is a new service aimed to give ASIC design support to HEP ASIC designers:
  - Invole experienced practitioners (EP-ESE)
  - Subcontract specialized tasks
  - Train and coach

- Service is hosted in the EP-ESE-ME (chips.support@cern.ch):
  - Small core team (2 fellows + 5 FTE-months for 2020)
  - 1 new LD verification engineer to start on June → lpGBT
  - Support requests are shared amongst ~10 FTE (analog, digital and verification experts)

- Mid to long term plan is to ramp-up the service with FTE staff positions