FEAST and bPOL status and plans

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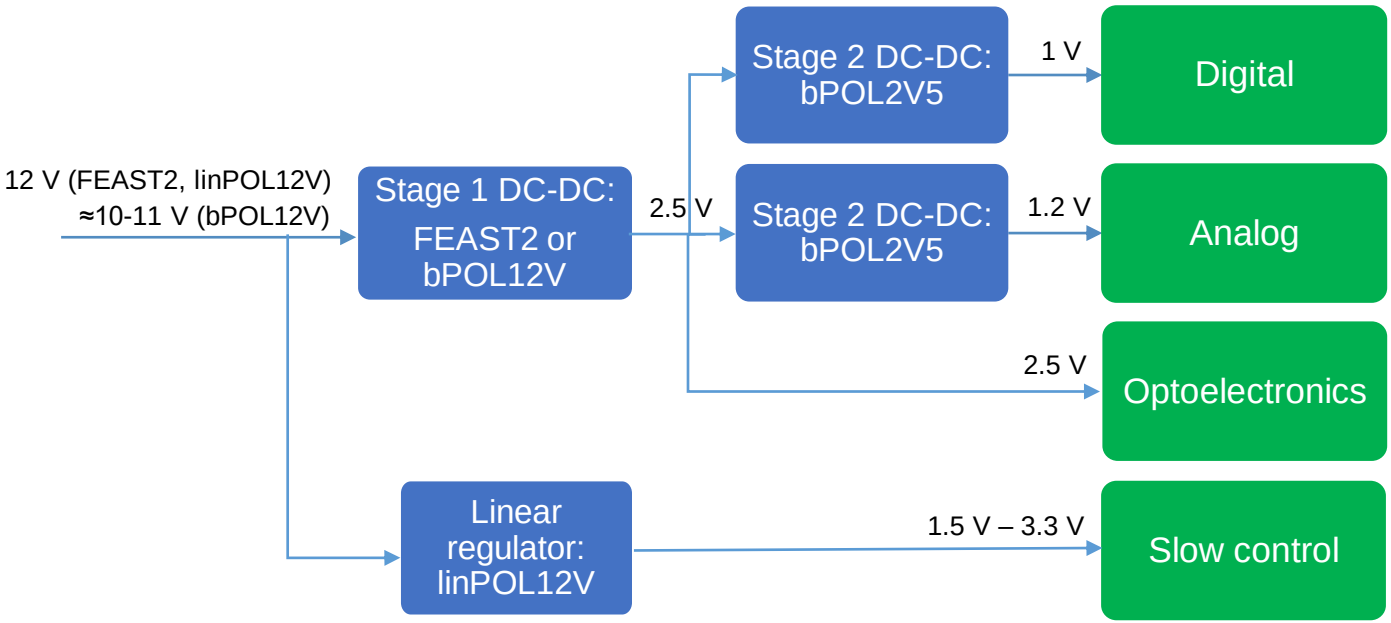
ACES, May 26, 2020

The DC-DC project in the EP-ESE group develops the elements for a modular radiation and magnetic field tolerant power distribution system



This table presents the components that are or will be available for on-detector power distribution

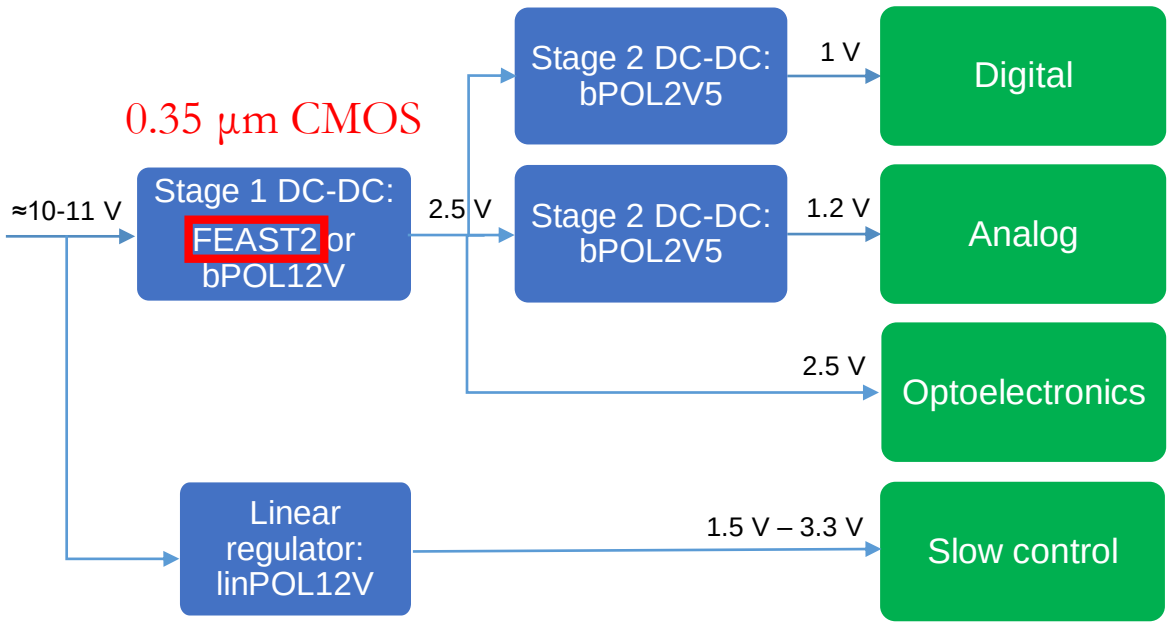
Nomenclature

xPOLyV_Vz.w

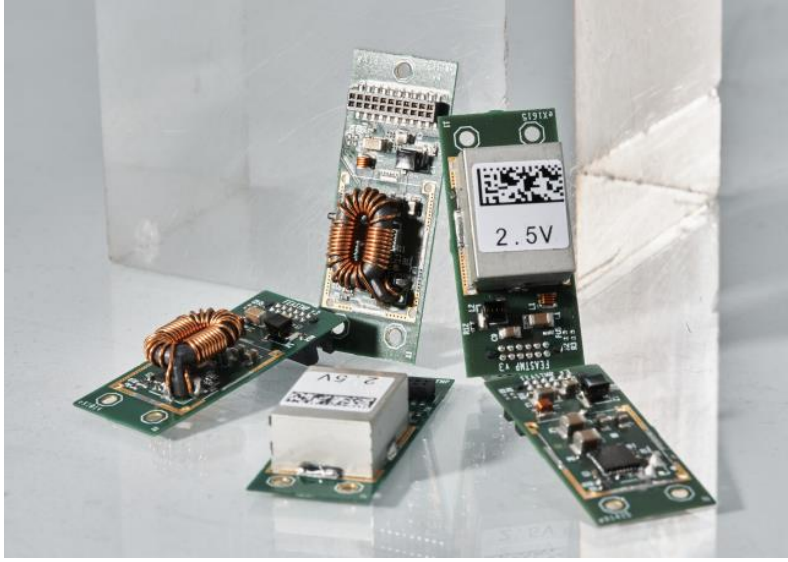
x = buck or linear
POL = Point Of Load
y = input voltage rating (12V, 2V5, etc.)
z = rating of the CMOS technology
w = version of the design

	Name	Type	Vin max	Iout max	Technology	Radiation specs	Package	Availability
Stage1	**FEAST2**	DCDC buck	12V	4 A	350nm CMOS with High Voltage extension at 80V	150Mrad 5e14 n/cm^2 SEE "immune"	QFN32	✓
Stage1	**bPOL12V**	DCDC buck	10-11V (TBD)	4 A	350nm CMOS with High Voltage extension at 25V	150Mrad **2e15 n/cm^2** SEE "immune"	QFN32	In development (see planning slide 21)
Stage2	**bPOL2V5**	DCDC buck	2.5V	3 A	130nm CMOS	150Mrad 7e15 n/cm^2 SEE "immune"	Naked chip with bumps for flip-chip	In development (see planning slide 21)
Linear	**linPOL12V**	Linear regulator	12V	80 mA	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm^2 SEE "immune"	DFN8	✓

Information and datasheets available at: http://project-dcdc.web.cern.ch/project-DCDC


0.35 μm CMOS
≈10-11 V
Stage 1 DC-DC:
FEAST2 or
bPOL12V
2.5 V
Stage 2 DC-DC:
bPOL2V5
1 V
Digital
Stage 2 DC-DC:
bPOL2V5
1.2 V
Analog
2.5 V
Optoelectronics
Linear
regulator:
linPOL12V
1.5 V – 3.3 V
Slow control

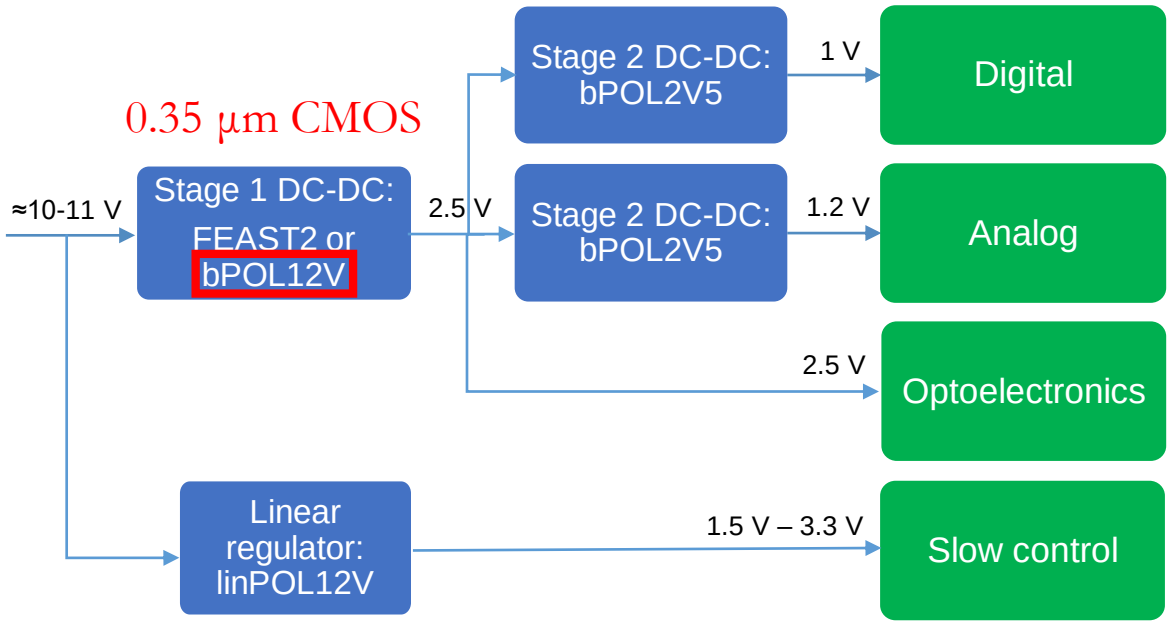
~40000 FEAST ASICs and
~47000 FEASTMP modules
have been/are being delivered to the experiments



No signs of discontinuation of the CMOS process

For big orders of ASICs, the turnaround time is at least 6 months

For modules, future orders will be grouped in production runs, and the cost and turnaround time cannot be guaranteed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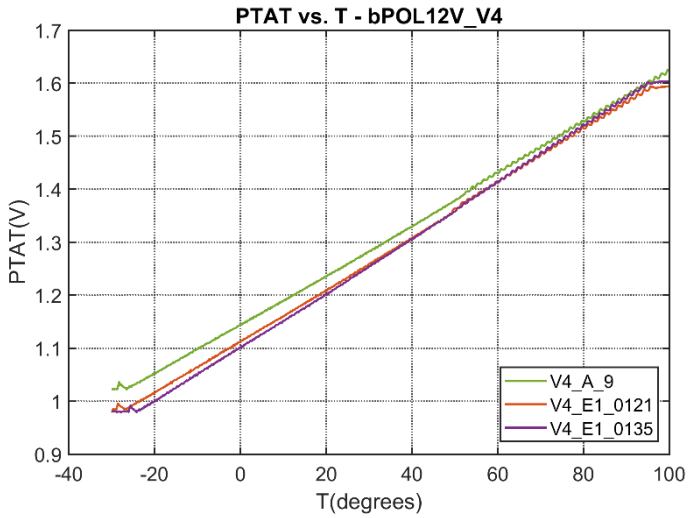
bPOL12V features:

An adjustable switching frequency f_{sw}. Caveat: for reliability concerns, the $f_{sw} \cdot L$ product must be as large as possible, where L is the inductor value (the minimum requirement is $f_{sw} \cdot L > 550\ MHz \cdot nH$)

An overcurrent protection which does not allow $I_{out} > 5.5\ A$ if the load requires a large current in faulty conditions (in all cases the systems must be designed so that $I_{out} \leq 4\ A$ in normal conditions)

A temperature sensor and an overtemperature protection (it turns off the converter when its temperature exceeds 120°C)

The PTAT output provides a voltage that is proportional to the on-chip temperature

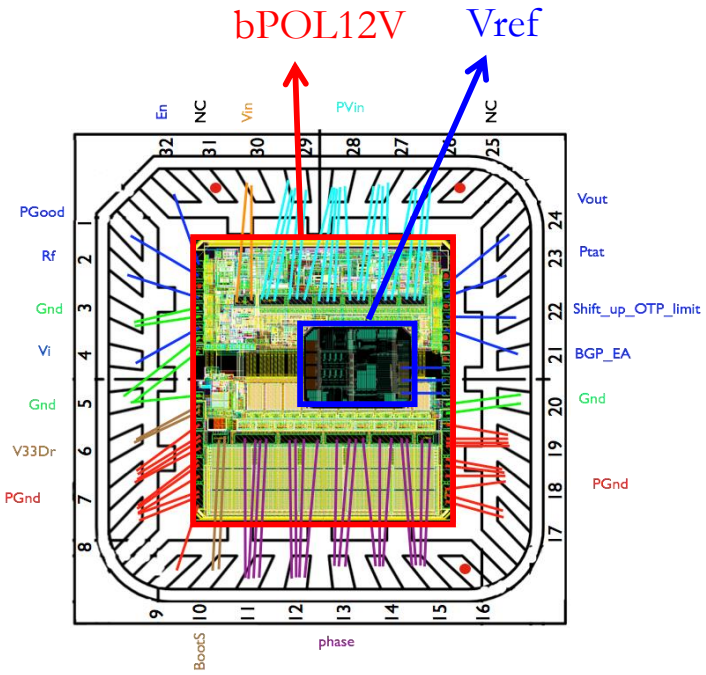


A bandgap voltage reference that will be trimmed at wafer level through e-fuses during production tests, guaranteeing a narrow distribution of the output voltage

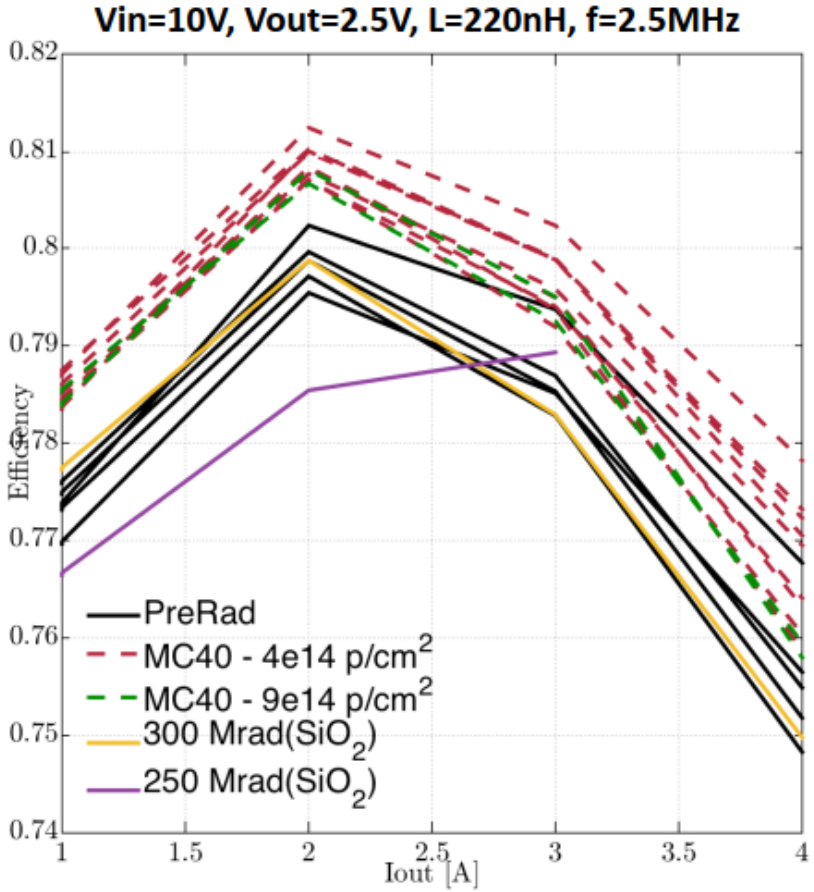
Voltage reference for bPOL12V: the Vref chip (130 nm CMOS)

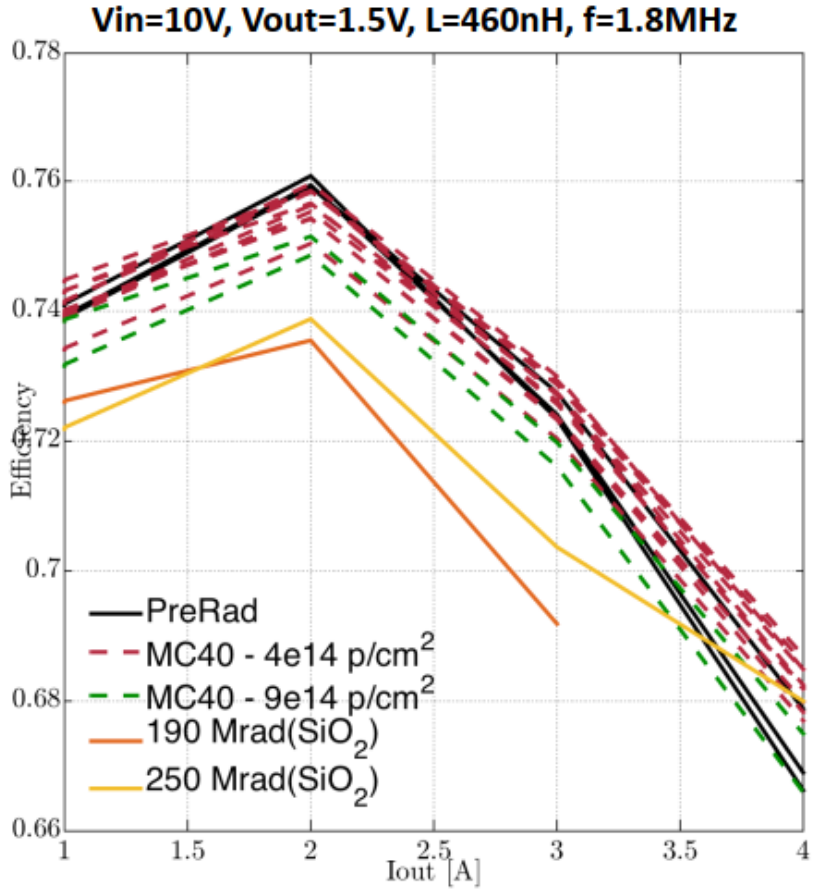
Vref can provide a radiation-hard voltage reference to bPOL12V, which will be also trimmed through e-fuses during production tests.
It is placed on top of bPOL12V and is embedded in the same QFN32 package.

The last prototype of Vref has shown tolerance to Single Event Effects
and to 200 Mrad of TID



Efficiency of bPOL12V_V25.4 (latest prototype of bPOL12V)





bPOL12V_V25.4 has been proved to be tolerant to:

- $300\ Mrad$ of Total Ionizing Dose (X-ray irradiation at CERN)
- $9e14\ p/cm^2$ (corresponding to $2e15\ n/cm^2$, $1\ MeV$ equivalent, irradiation at the MC40 cyclotron, Birmingham)

bPOL12V_V25.3 (the previous prototype, few differences with bPOL12V_V25.4) was proved to be tolerant to Single Event Effects (irradiation at the Heavy Ion facility in Louvain-la-Neuve, Belgium)

A preliminary datasheet of bPOL12V_V25.4 can be found at:
http://project-dcdc.web.cern.ch/project-DCDC/public/ASICDatasheet.html

bPOL12V: long-term reliability

What industry does	What we can do
The voltage rating of the used device is usually $\approx 2V_{in,max}$	Due to radiation-hardness constraints, we have to use $14\ V$-rated devices for bPOL12V. Little reliability information on the process is available. What is the maximum V_{in} to guarantee a reliable operation?
< 100 samples are stressed for ≈1000 h	We built three systems to keep up to 220 DC-DC modules in (or beyond) operational conditions for long runs.
Screening to decrease infant mortality	Screening procedure based on voltage stress of the power transistors

bPOL12V: results of the long-term stress tests

Failures have been found starting from $V_{in} = 12\ V$

Despite the new gate drivers designed to contain this problem, bPOL12V_V25.4 does not show an improved reliability

bPOL12V_V25.3

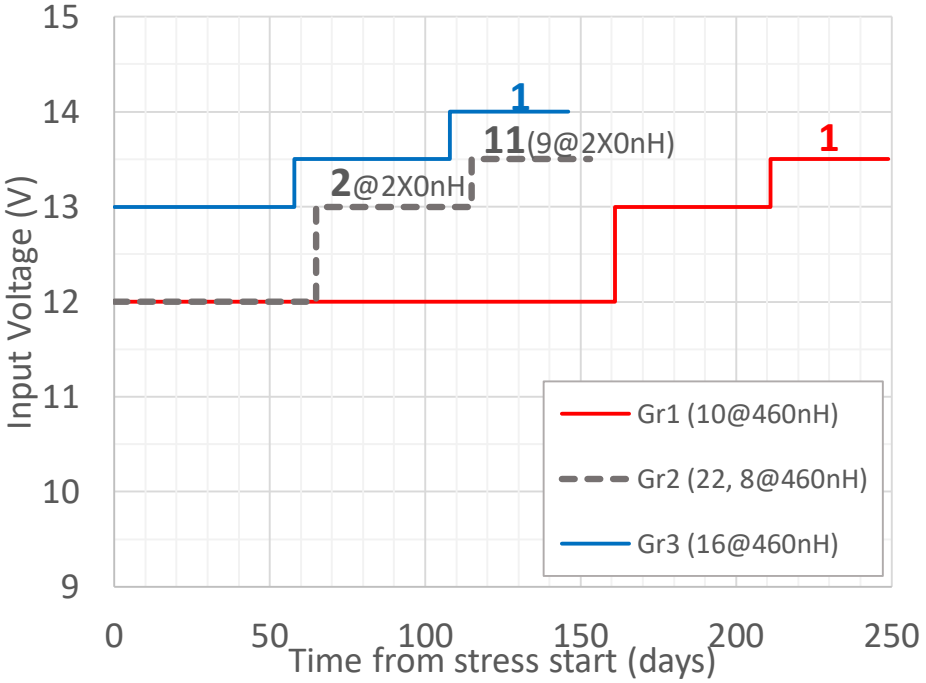
Stress conditions (48 samples, Dec 17 – Aug 18):

$I_{out} = 2.5 - 3\ A$ $V_{out} = 1.5\ or\ 2.5\ V$

$L = 220\ or\ 460\ nH$ $f_{sw} = 1.8, 2.5\ or\ 3\ MHz$

$T \approx 60℃$

Samples both in qfn32 package or Chip-On-Board



+ 48 samples kept at $V_{in} = 12\ V$ for 190 days with no failures

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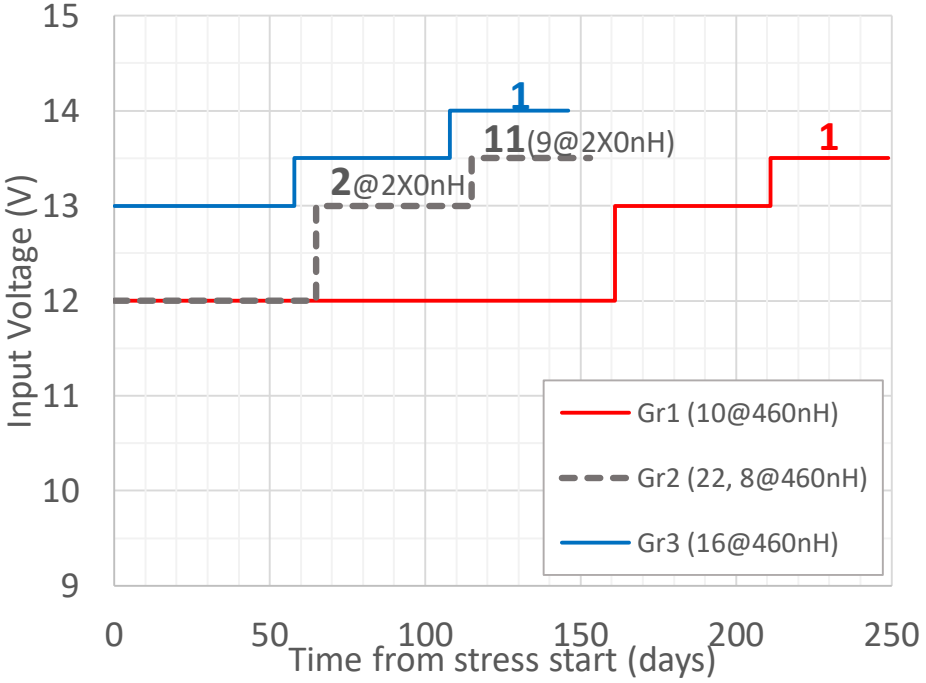


+ 48 samples kept at $V_{in} = 12\ V$ for 190 days with no failures

bPOL12V_V25.4 (latest prototype)

Stress conditions (70 samples, Oct 19 –):

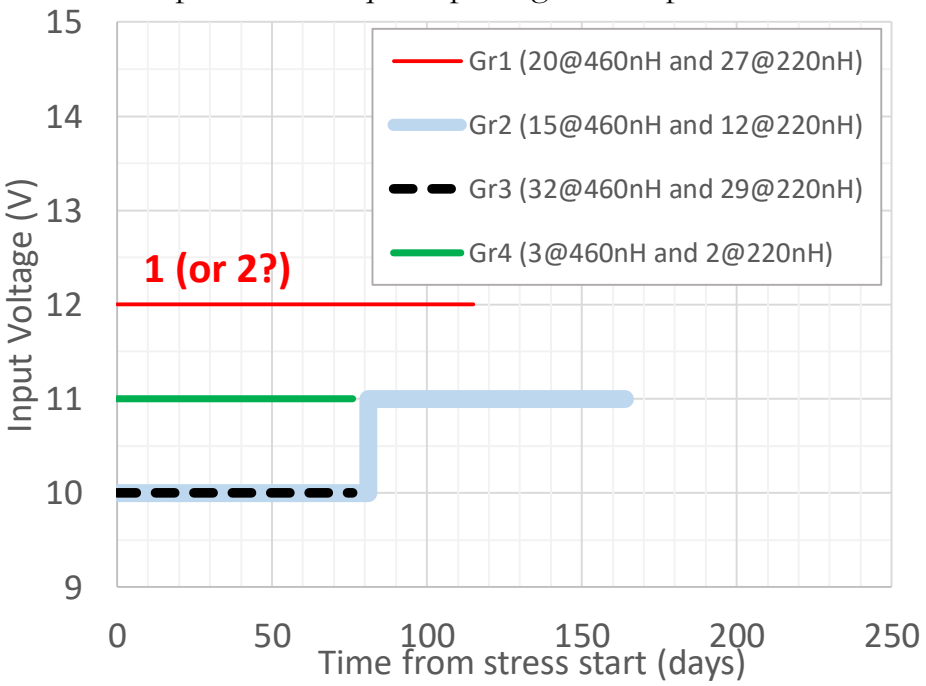
$I_{out} = 0 - 4\ A$ $V_{out} = 1.5\ or\ 2.5\ V$

$L = 220\ nH\ and\ f_{sw} = 2.5\ MHz\ or$

$L = 460\ nH\ and\ f_{sw} = 1.8\ MHz$

$T \approx 100℃$ for Chip-on-Board

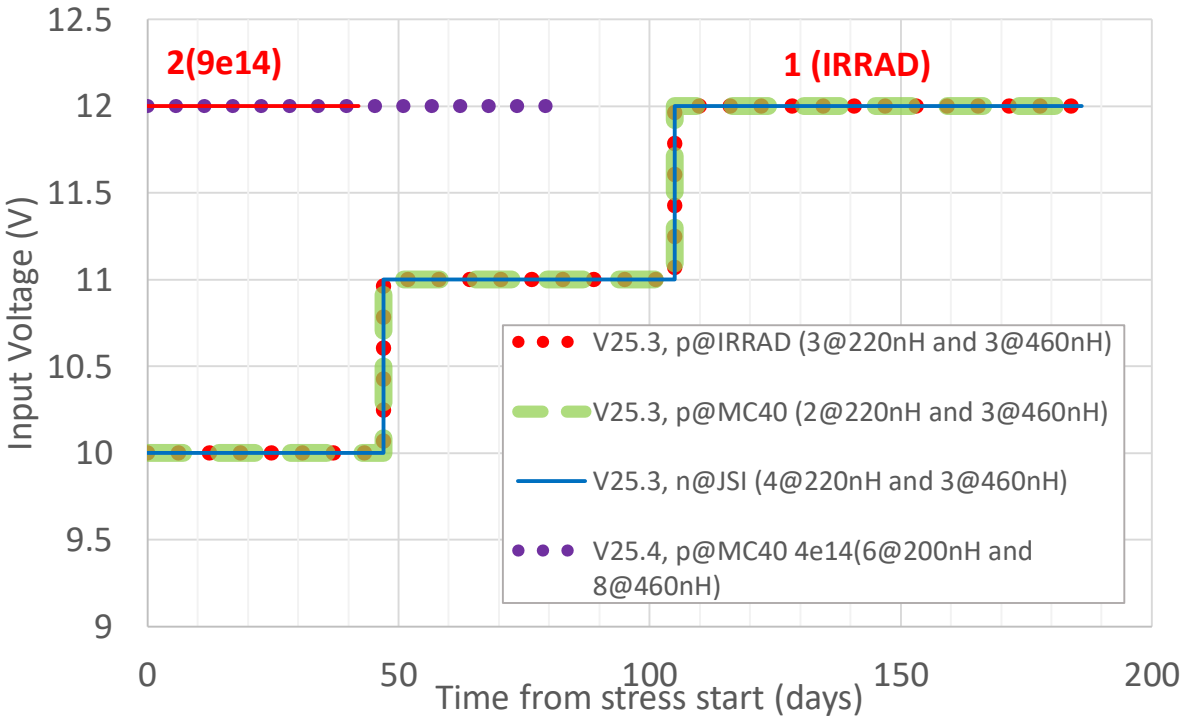
Samples both in qfn32 package or Chip-On-Board



bPOL12V: results of the long-term stress tests on irradiated samples (protons or neutrons)

Irradiated samples of both bPOL12V_V25.3 and bPOL12V_V25.4 have shown failures at $V_{in} = 12\ V$

Stress conditions (32 samples, Apr 19 – Oct 19):
$I_{out} = 0\ -3.7\ A \quad V_{out} = 1.5\ or\ 2.5\ V$
$(L = 220\ nH\ and\ f_{sw} = 2.5\ MHz)\ or\ (L = 460\ nH\ and\ f_{sw} = 1.8\ MHz)$
Samples only in Chip-On-Board



bPOL12V cannot operate reliably for $V_{in} \geq 12\ V$

No failures have been found with $V_{in} = 11\ V$ yet, both on pre-rad and on irradiated samples

We are trying to devise a strategy to determine the maximum acceptable V_{in} from accelerated stress tests (delayed by the present sanitary crisis)

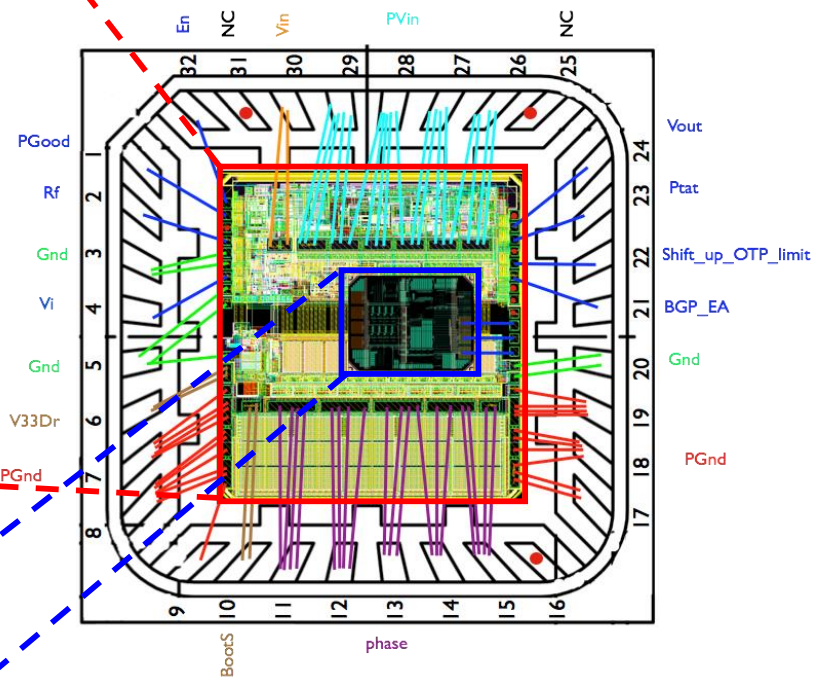
bPOL12V: status

bPOL12V_V25.5

Released for fabrication in January, 2020

Main changes compared to V25.4:

- Gate drivers have been replaced with those of V25.3
- The current flowing through the external resistor that defines f_{sw} has been increased (to avoid a frequency shift found with Displacement Damage). For the same f_{sw}, a lower value of resistance will be needed in V25.5.

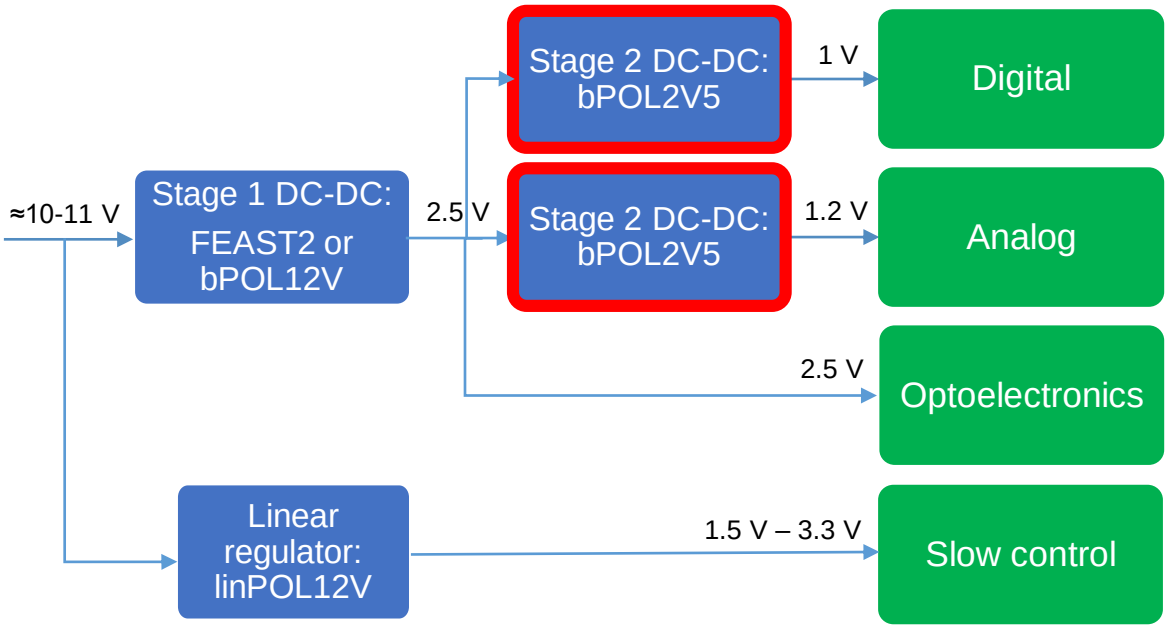


Vref

Released for production in April, 2020

Stress tests on bPOL12V_V25.5 will start as soon as possible after the reception of the ASICs (June 2020)

130 nm CMOS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1.5 V – 3.3 V
Slow control

bPOL2V5 features:

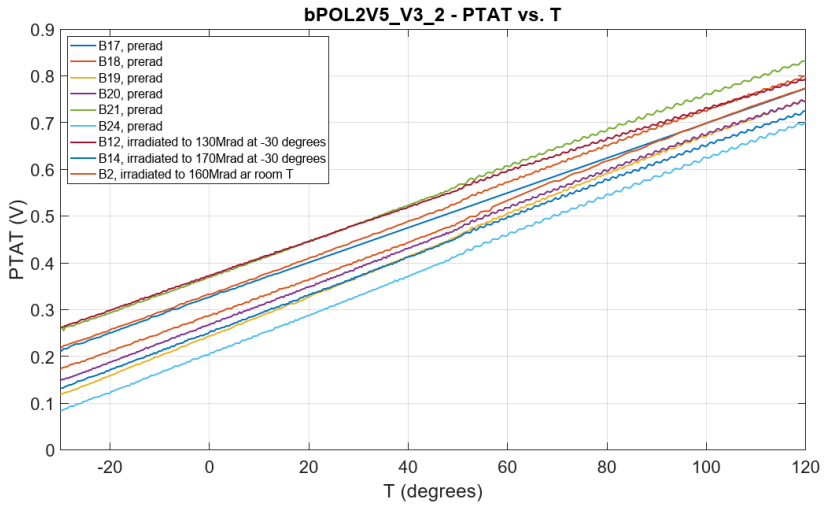
A bandgap voltage reference that will be trimmed through e-fuses during production tests, guaranteeing a narrow distribution of the output voltage

An overcurrent protection which does not allow $I_{out} > 3.8\ A$ if the load requires a large current in faulty conditions (in all cases the systems must be designed so that $I_{out} \leq 3\ A$ in normal conditions)

A negative current protection, that prevents the converter from being damaged by a large negative inductor current

A temperature sensor and an overtemperature protection (it turns off the converter when its temperature exceeds 100°C)

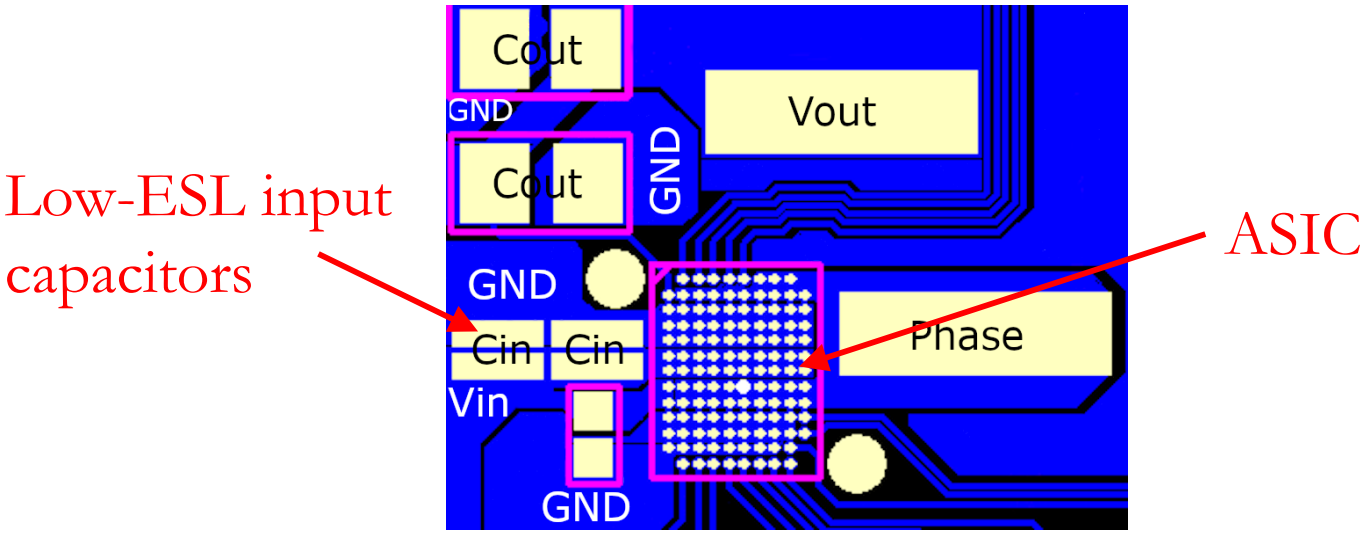
The PTAT output provides a voltage that is proportional to the on-chip temperature



bPOL2V5: guidelines for reliability

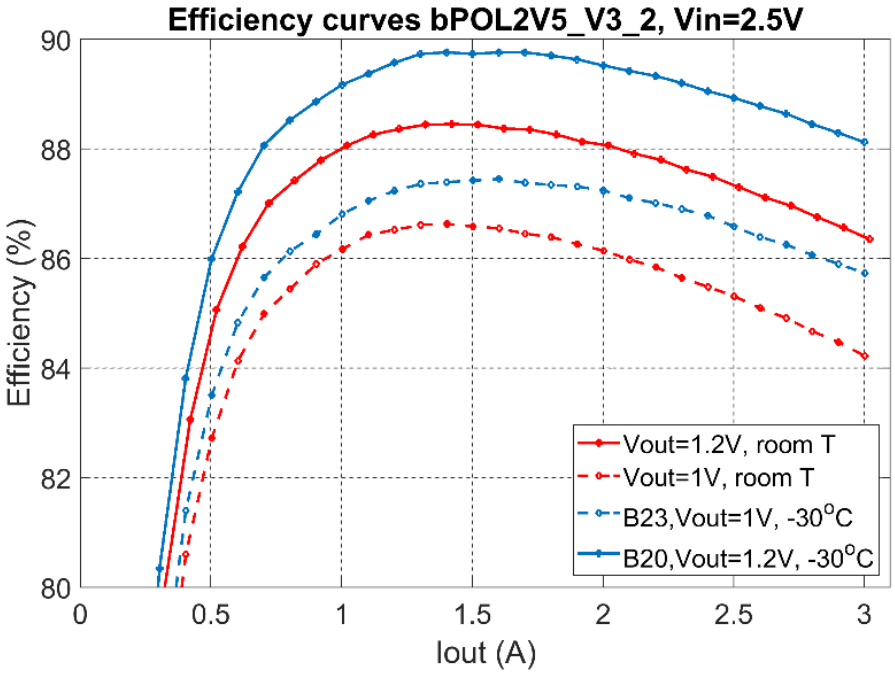
The voltage rating of the used devices is $3.3\ V$, while $V_{in,max} = 2.5\ V$.
The input parasitic inductance (due to the bonding, the PCB and the ESL of the input capacitance) must be minimized to limit the voltage spikes generated by the switching operation:

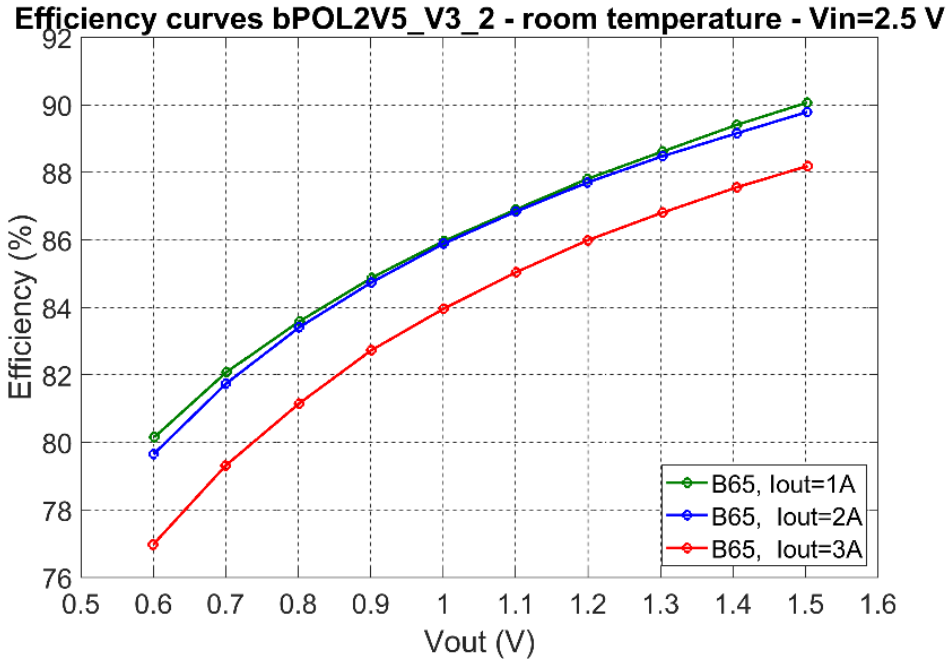
- a flip-chip assembly is mandatory
- the choice and the placement of the input capacitors must be identical or very similar to our test module (we can provide the PCB layout)
- any PCB design using bPOL2V5 must be validated by extracting the parasitic input inductance and comparing it to our test module (our collaborators at the University of Udine can help for this)



Operation with $L = 100\ nH$ and $f_{sw} \approx 4\ MHz$ is highly recommended for high reliability and efficiency

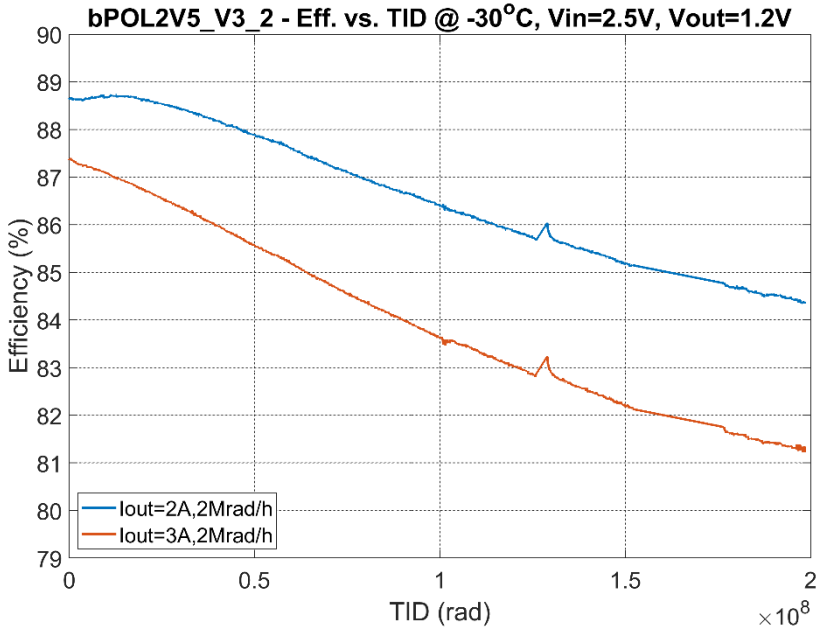
Experimental results on the last prototype of bPOL2V5 (bPOL2V5_V3.2)





bPOL2V5: radiation tests (1/2)

- **Total Ionizing Dose**



The lower is the dose rate, the lower is the efficiency degradation:
the drop in the efficiency is expected to be significantly lower in the LHC experiments.

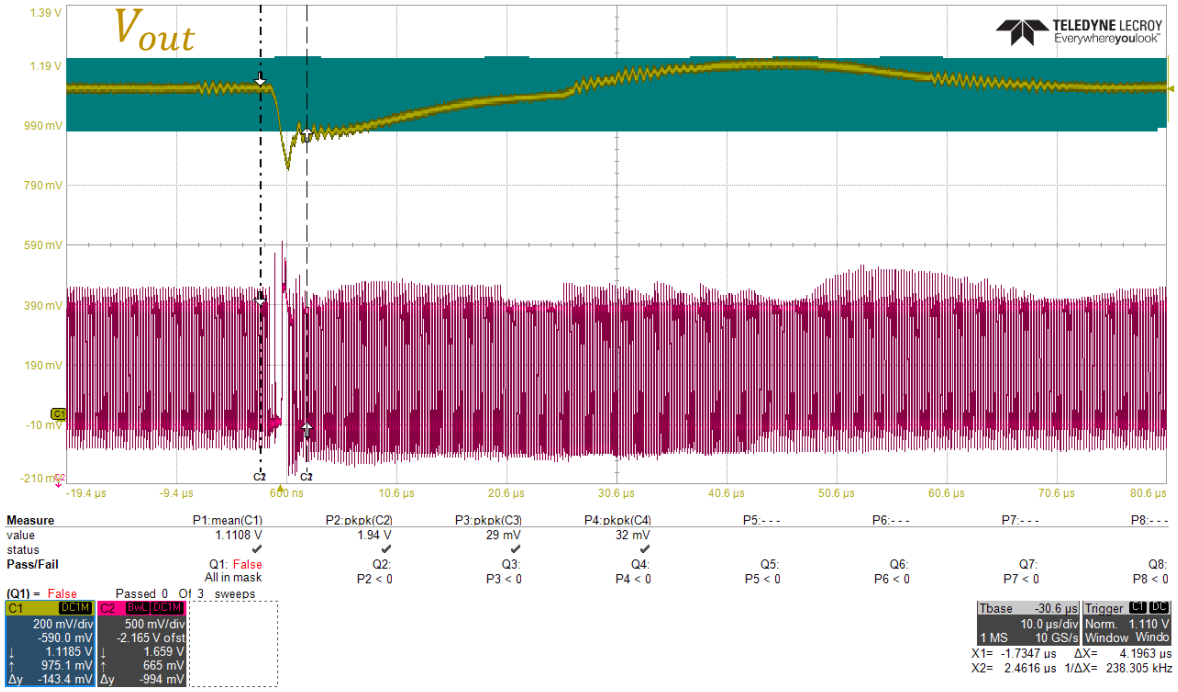
- **Displacement Damage**

No significant performance degradation have been found on samples of bPOL2V5_V3.1 irradiated with protons (at the IRRAD facility at CERN, up to $6.6e15\ p/cm^2$) and neutrons (at the TRIGA reactor in Ljubljana, up to $1e16\ n/cm^2$)

bPOL2V5: radiation tests (2/2)

- **Single Event Effects**

Irradiation of bPOL2V5_V3.2 at the Heavy Ion facility in Louvain-la-Neuve, Belgium highlighted that transients exceeding 10% for few µs on V_{out} occur for LET≈$14\,\frac{MeV\,cm^2}{mg}$



Irradiation with a focused ion beam at GSI, Darmstadt, Germany, allowed the localization of the sensitive spots (n-wells not connected to the power supply acting as the bulk of p-type differential pairs).

Strategies to filter out these events have been devised.

bPOL2V5: long-term stress tests

Stress tests with $V_{in} = 3\ V$ on 32 samples of bPOL2V5_V3.2 for 1000 h have highlighted no failures ($L = 100\ nH$, $f_{sw} = 4\ MHz$, $I_{out} = 1.2 - 3\ A$)

No failures were found also for a previous prototype using devices rated $2.5\ V$, using V_{in} up to $2.9\ V$ ($L = 100\ nH$, $f_{sw} = 4\ MHz$, $I_{out} = 2.2\ A$, 21 samples stressed for more than a year, 24 samples stressed for 6 months)

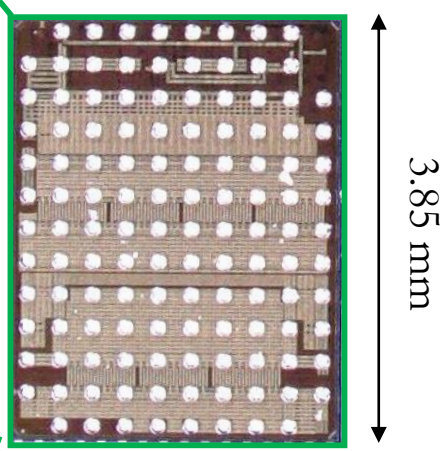
bPOL2V5: status

bPOL2V5_V3.3

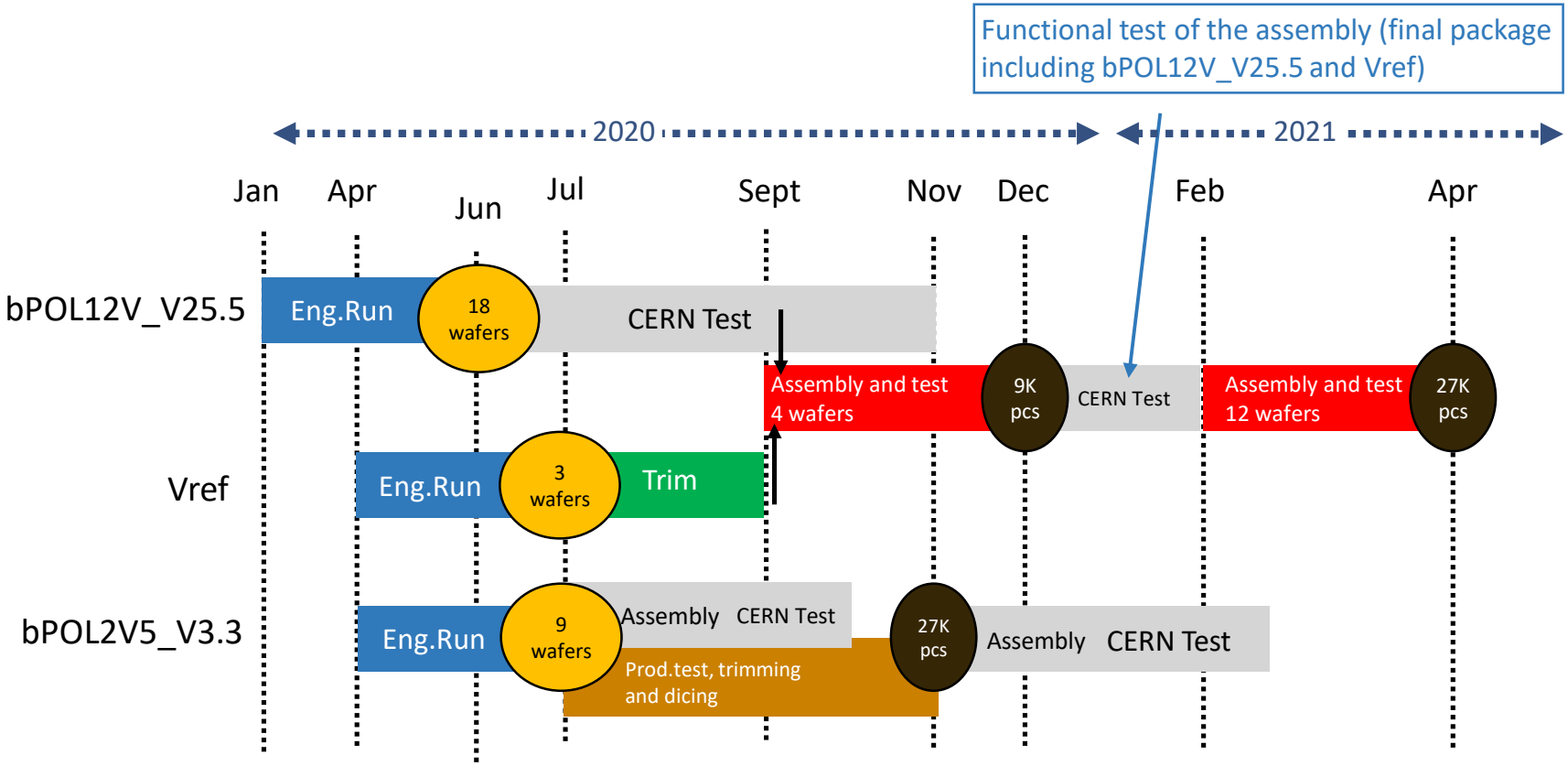
Released for production in April, 2020

Main changes compared to V3.2:

- Test features added to allow wafer-level testing (the pinout is slightly changed compared to V3.2 due to this).
- On-chip filters added to filter out the single events.
- Improved circuitry to minimize the TID-induced degradation.



Planning



The production testing and assembly rely on companies, whose schedule may be affected by the current sanitary crisis.

The amount of ASICs that are being produced correspond to the needs of the ATLAS ITk strip and of the CMS outer tracker.

If more are needed, this should be notified as soon as possible, and the expected delay between the request and the delivery of the ASICs is 8 months.

Summary

FEAST ($12\ V$- $4\ A$)

ASICs and modules are in production

No signs of discontinuation of the CMOS process

bPOL12V ($10/11\ V$- $4\ A$, increased radiation tolerance compared to FEAST)

The last prototype complies with the radiation tolerance specifications

Some failures have been found during long term stress tests for $V_{in} \geq 12\ V$: a de-rating of the input voltage is needed

The fully-tested and packaged final ASICs should be available in April 2021

bPOL2V5 ($2.5\ V$- $3\ A$)

The available prototypes comply with the Total Ionizing Dose and Displacement Damage specs

Improvements to avoid significant transients on V_{out} due to Single Event Effects have been included in the final version

The fully-tested final ASICs should be available in Q1 2021