lpGBT Project Status and Plans

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Outline

- lpGBT Chipset
- GBTIA
- LDQ10
- lpGBT v0
  - Availability
- lpGBT v1 what's new!
  - Motivation
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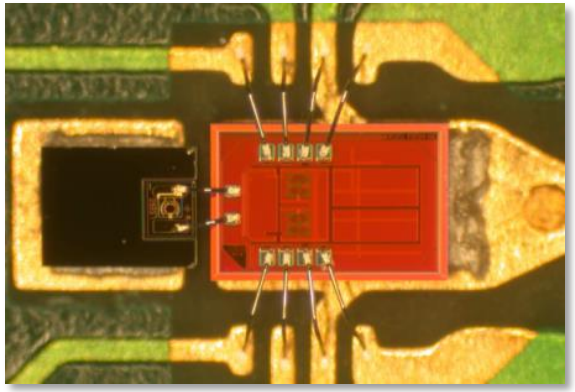
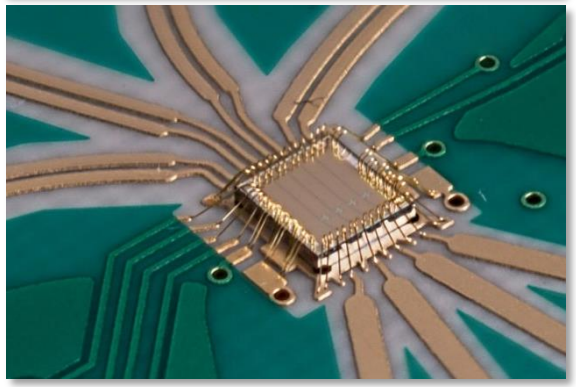
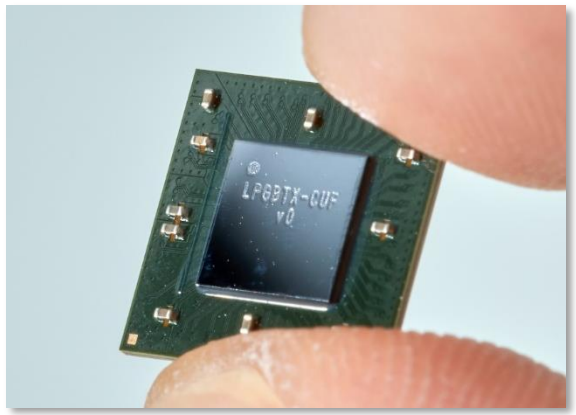
- PiGBT

lpGBT Chipset

- GBTIA
  - 4.8 Gb/s Transimpedance Amplifier
  - Amplifies the weak photo-current detected by the PIN diode
- LDQ10
  - 10.24 Gb/s Quad VCSEL Driver
  - Modulates the VCSELs current to achieve electro-optical conversion
- lpGBT
  - 5.12 / 10.24 Gb/s Transceiver
  - Establishes the communications between the counting room and the frontend modules





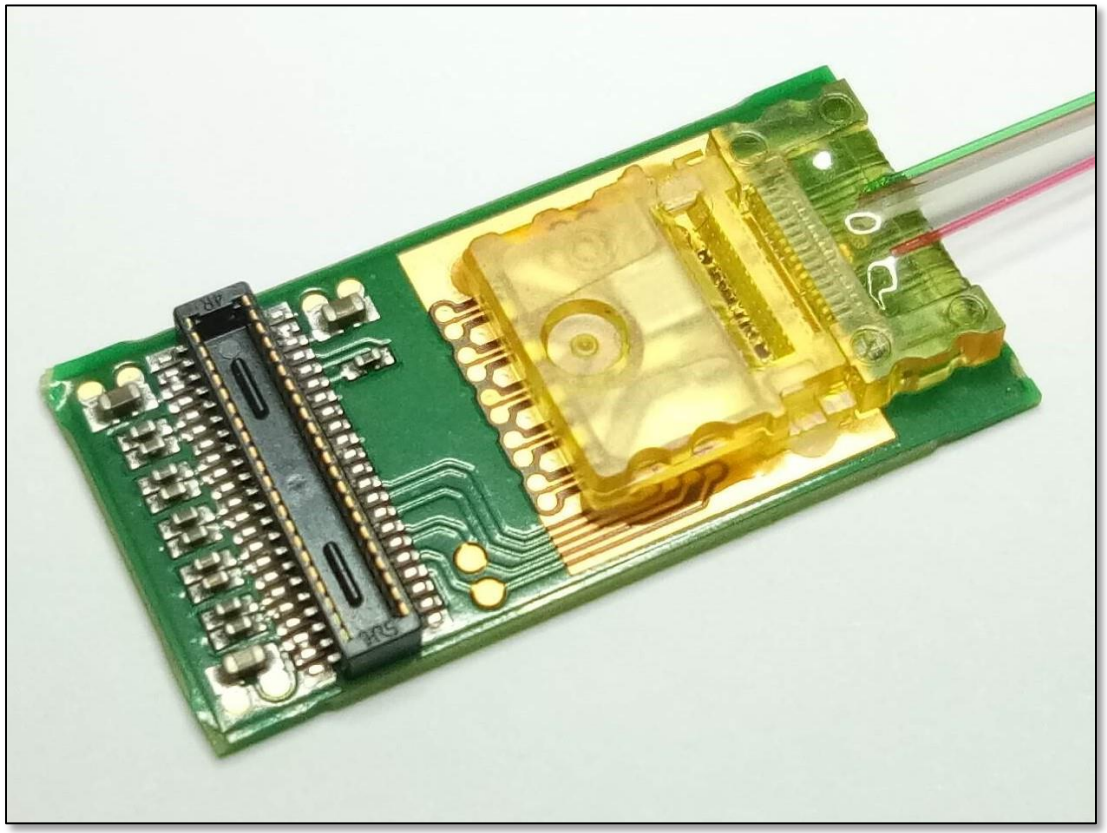


GBTIA

4.8 Gbps PIN-receiver

- Legacy from the GBT project
  - Originally: 130 nm IBM
  - Now: 130 nm GF (basically the same process)
- It will be used at 2.56 Gbps
- Has proven
  - Excellent performance
  - Low power (~120 mW)
  - TID (~200 Mrad) & SEU robust
- Production wafers available
  - 5 “IBM” wafers (2015)
  - 24 “GF” wafers (2018)
  - 24 “GF” wafers (2020)
  - ~2.1k chips/wafer
- Approx. 70k will be used to assemble VTRX+ modules
  - Module assembly yield: ~90%

VTRX+



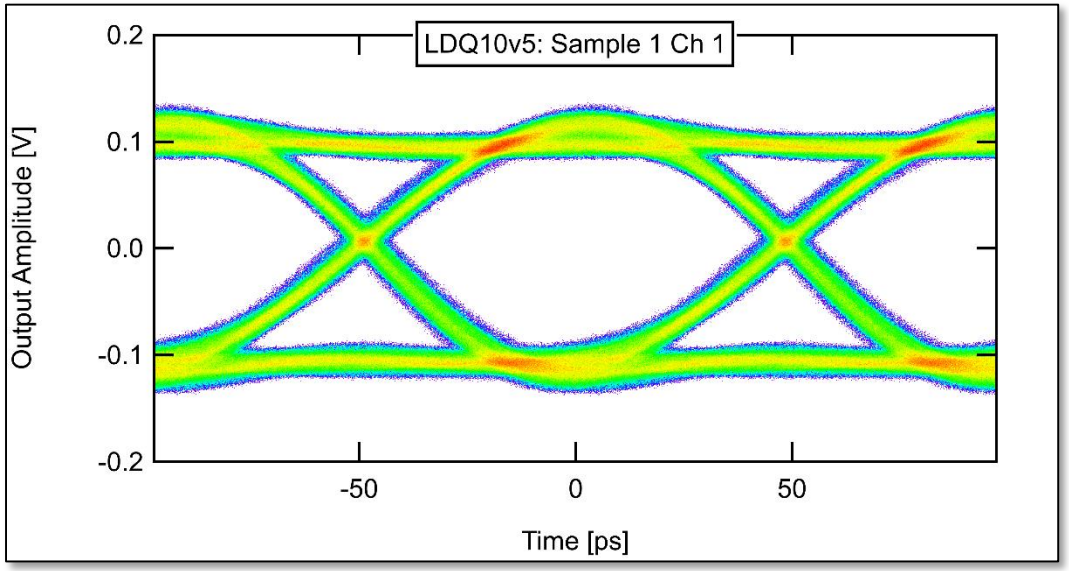
(See: Francois Vasey, “VL+ status and plans”)

LDQ10

10.24 Gb/s Quad VCSEL Driver

- Engineering run: Nov. 2019
  - Shared run: LDQ10 / picoTDC
- 24 wafers ordered
  - 11 “LDQ10 Wafers”
  - 9590 LDQ10 chips / wafer
- 6 wafers delivered: February 2020
  - 3 reserved for the picoTDC project
  - Further 18 on “hold”
- LDQ10 v5:
  - Corrects v4 SEU/SET sensitivity
  - Covid-19 just prevented SEU testing!
  - But confidence is very high:
    - Extensive SEU / SET verification
    - 10k events injected per node during write/read/idle states
    - Simulation done for back annotated design (min/typ/max corners)

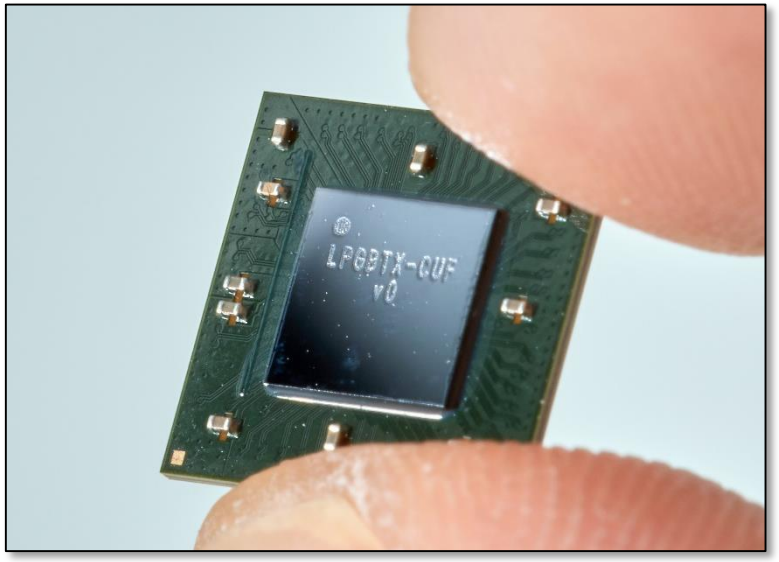
- Approx. 70k will be used to assemble VTRX+ modules
- First test results:
  - 5 devices tested
  - Chips fully functional
  - [Almost] no chip-to-chip variation and very good channel uniformity



(See: Francois Vasey, “VL+ status and plans”)

lpGBTv0 Availability

- Chips distributed so far: 373
  - “Good”: 204
  - “I2C0”: 169
- Available:
  - Tested: 123
  - To be tested: 400 (yield forecast: 94%)



Exp.	Detector	Good	I2C0	
ATLAS	ITK	60	0	60
ATLAS	Lar	10	14	24
ATLAS	Muon	11	0	11
ATLAS	BCM	2	0	2
CMS	DCT	0	6	6
CMS	IT	0	10	10
CMS	ME0	0	20	20
CMS	?	0	17	17
ESE	VLDB+	27	0	27
ESE	ESE	0	6	6
ATLAS	HGCAL	0	10	10
CMS	Pixel	45	0	45
CMS	ETL	0	3	3
CMS	OT	45	30	75
CMS	DT	0	6	6
CMS	EB	0	47	47
BE/BI	BLM	4	0	4
		204	**169**	**373**

Motivation

- The lpGBT v0 was extensively tested during 2019
- Tests included:
  - Functionality (digital and analogue)
  - Total Dose Tests
  - SEU Tests
- Tests proved the ASIC to be close to “100% functional”
  - Samples distributed to the users for system prototyping (373 so far)
  - Minor functional bugs discovered!
  - Up-to-date list of know issues can be found in the manual:
    - https://lpgbt.web.cern.ch/lpgbt/v0/known_issues.html
- TID & SEU tests revelled some “fragilities”, with the most “notorious” being:
  - Performance degradation with TID of the Phase-Shifter, eFuses and the ePorts at 1.28 Gbps
  - Configuration registers sensitive to SEEs
  - Relatively high deterministic jitter (for high precision timing applications) on the eClocks (except the 40 MHz clock)
- These motivated the redesign of some of the circuits and functionality

lpGBT v1 new features (1/…)

- Pin ***RSTN***
  - Has now an internal **pull-up** (instead of pull-down in v0)
- I2C slave pins ***SLSDA*** & ***SLSCL***
  - Have now internal **pull-ups** (instead of pull-downs v0)
- I2C Masters ***M2SDA***, ***M1SDA***, ***M0SDA***, ***M0SCL***, ***M1SCL*** & ***M2SCL***
  - Have now internal **pull-ups** (instead of pull-downs v0)
- Pins ***TSTCLKINP*** & ***TSTCLKINN***
  - "Removed": not used (for the time being…) but still present in the package
    - Warning*: they might become static configuration pins if needed!

Corrected

- Pin ***VCObypass***
  - Renamed to ***BOOTCNF0**** (to reflect the new functionality). Configuration pin!
- Pin ***SC_I2C***
  - Renamed to ***BOOTCNF1**** (to reflect the new functionality). Configuration pin!
- Pin ***STATEOVRD***
  - Renamed to ***ECDINTERM**** (to reflect the new functionality). Configuration pin!

* These are configuration pins. Please remember to leave "place holders" for pull-up / pull-down resistors in case you have not yet decided on a specific configuration setting (or not enough information is yet available, as is the case for the "removed" pins TSTCLKINP & TSTCLKINN)!

What's new in the lpGBT v1 (2/…)

- Configuration memory:
  - Changes for SEE robustness:
    - eFuses synchronously read and copied into the memory
  - Changes for TID robustness:
    - CRC word added to the eFuses
    - Configuration CRC verified at start-up (loading from Fuses) and during operation
    - Useful for weak to moderate radiation hard environments (< 100 Mrad)
    - (No attempt to directly solve the eFuses TID sensitivity)
- Chip start-up now includes an option to initialize from a built-in ROM:
  - Allows the basic functions to be initialized letting the chip ready for detailed configuration via the IC-channel or the EC-port
  - Useful for radiation hard environments (> 100 Mrad)
- The EC-port now supports multi-drop buses:
  - Allows a master lpGBT (transceiver) to communicate with several secondary lpGBTs (transmitters or receivers) or Frontend devices through the EC-port
- Power-up sequence controlled by pins ***BOOTCNF1*** and ***BOOTCNF0*** introduced in the previous page
- Pre-emphasis will be removed from the high-speed transmitter for the benefit the [basic] performance at 10.24 Gbps!

lpGBT Manual[s]

- Two versions of the manual are now available at:
  - https://cern.ch/lpgbt
- The “v0” manual correspond to the first version of the chip:
  - These are the chips currently in circulation;
  - The v0 manual is stable with possible minor revisions to address either typos or for added clarification;
  - The v0 manual will be discontinued once the v1 version of the ASIC will be available!
- The “v1” manual corresponds to the final version of the chip:
  - The v1 chips are not yet available!
  - The v1 manual is available to give a preview of the final chip functionality!
  - Since design work is still ongoing it is possible that the v1 manual will undergo significant updates!
  - Nonetheless, the changes outlined in the previous pages are baseline!

lpGBT Schedule

- To keep updated with the project schedule please refer to:
  - https://ep-ese.web.cern.ch/content/lpgbt-vl-dcdc-schedule
- Schedule:
  - lpGBT v1 tapeout: Q4 [November] 2020
  - Prototypes @CERN: Q1 2021
  - Functional / TID / SEU testing complete: Q2 2021
    - Samples available
  - lpGBT v1 engineering tapeout: Q2 2021
  - Chips available (forecast):
    - 3k ASICs: [early] Q4 2021
    - +21k ASICs: Q4 2021

    } 8 engineering wafers

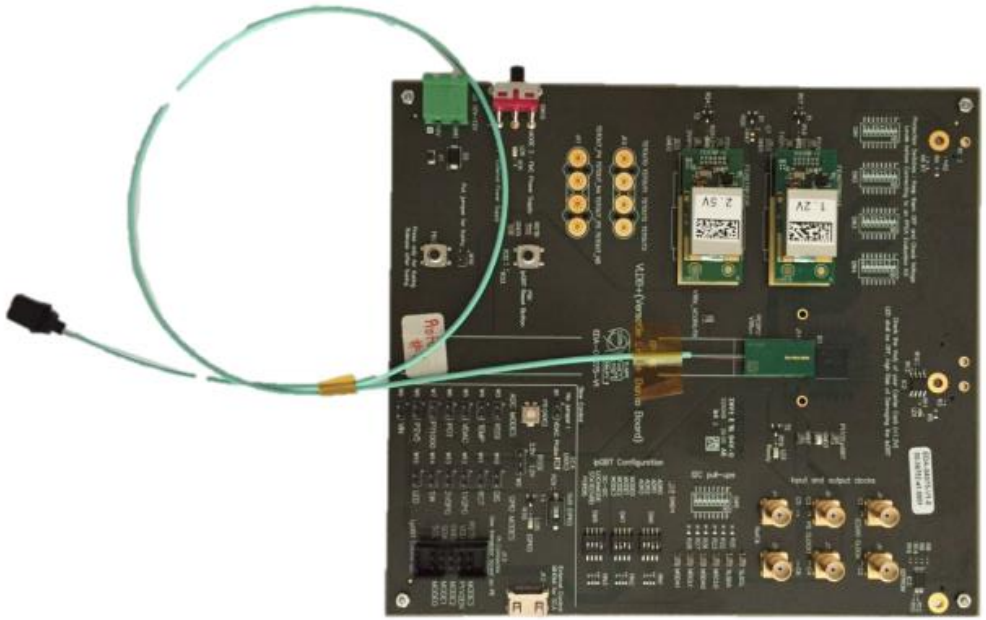
    - +75k ASICs: Q2 2022
    - +75k ASICs: Q3 2022

    } 50 production wafers

VLDB+

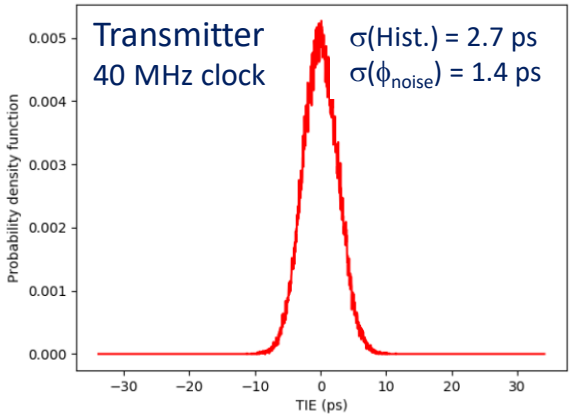
VLDB+ Prototype (v1)

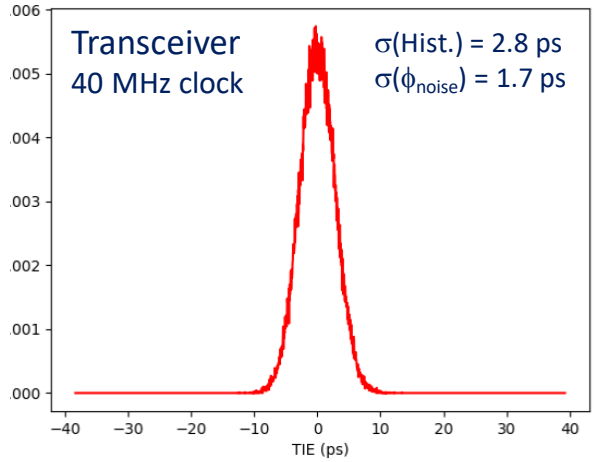
- Functionality: ✓
- Performance: ✓
- Manual:
  - https://vldbplus.web.cern.ch/manual/overview.html
  - Revision foreseen June
- Quantity:
  - 18 (reserved, only 2 tested so far)



VLDB+ (v2)

- Improving routing for high frequency performance (clocks and HS links)
- 1st production lot:
  - 30 pieces
  - Available: September
  - Cost: 1.8 kCHF – 2.0 kCHF (with DCDC but no VTRx+)





PiGBT

- Interfaces with the lpGBT to:
  - Control the chip
  - Program the eFuses
- Uses the lpGBT I2C and the mode control signals
- Implements a “web server”
  - Ethernet or Wi-Fi.
- Control is done through a web interface:
  - On your computer
  - On your mobile phone
- Knows how the registers relate to each other and to the modes of operation (prevents you from doing basic mistakes)
- Facilitates system development
- Documentation available soon at:
  - https://vldbplus.web.cern.ch/pigbtmanual/
- You can start [virtually] playing at:
  - https://pigbt.web.cern.ch/#/
- Prototype availability:
  - 20 available (reserved)
  - Additional 30 (to be assembled)
  - Price: 250 CHF