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The ATLAS ITk Strip Tracker

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on behalf of the ATLAS ITk Strip Community

ACES, CERN, 27th May 2020

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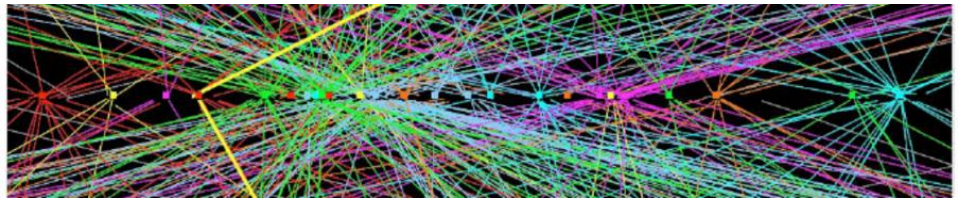
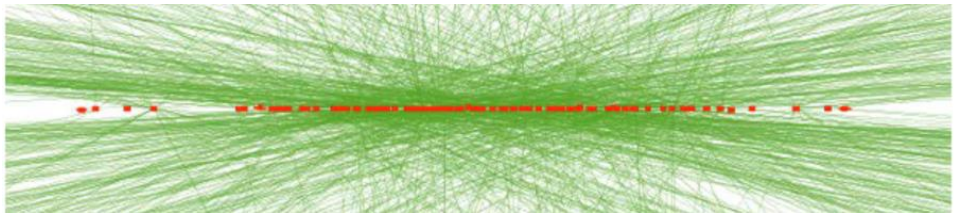
Detector Concept

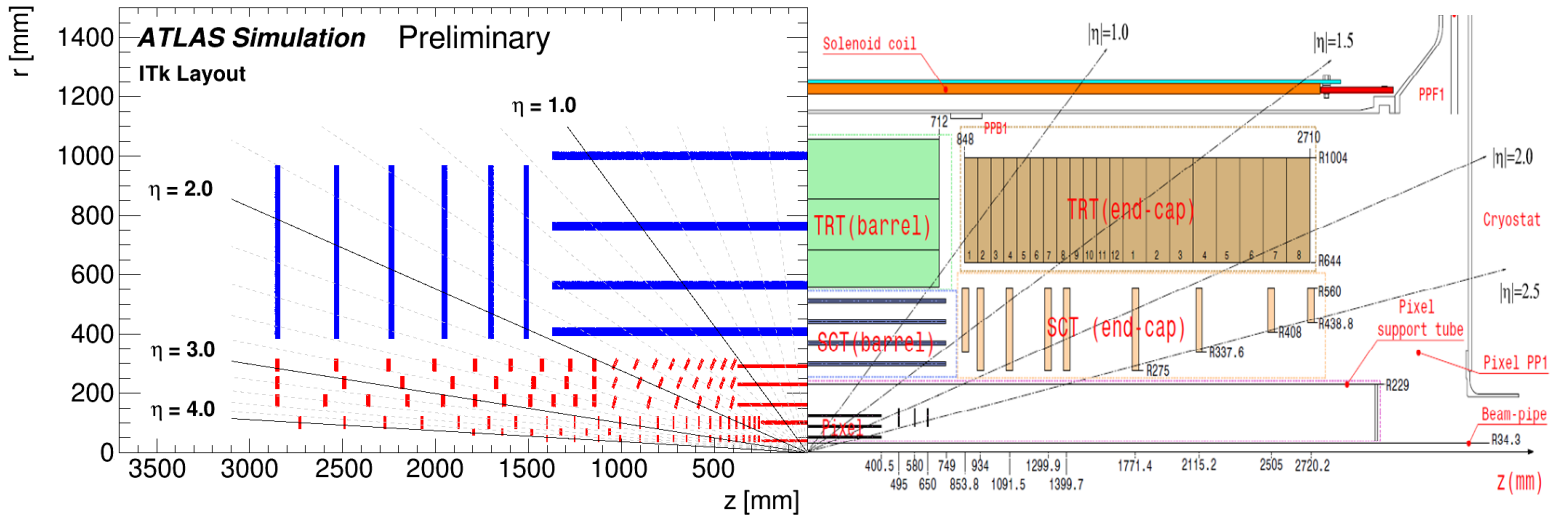
- An all new silicon tracker will be installed in ATLAS during LS3
- Strip barrel made of 4 double sided barrel layers
  - Two outer layers of “long” strips of 48 mm, 75.5 µm strip pitch
  - Two inner layers of “short” strips of 24 mm , 75.5 µm strip pitch
  - Stereo angle of ±26 mrad by module placement on local support
- Strip end-caps each comprising 6 double sided disks
  - Strip length varies with radius from 18-60 mm and pitch from 69.9-80.7 µm
  - Stereo angle of ±20 mrad in endcap implemented in sensor design
- Total Strip area (barrel + end-cap) 165 m^2, 60 million channels
- Along with 5 layer pixel system provides tracking coverage up to $|\eta| < 4.0$

LHC (25 vertices)



HL-LHC (200 vertices)





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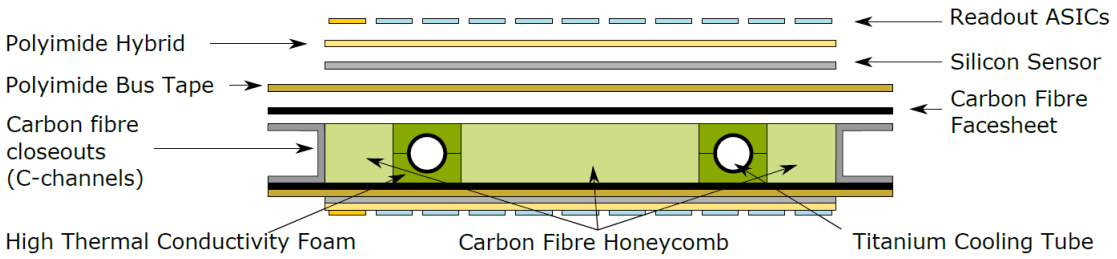
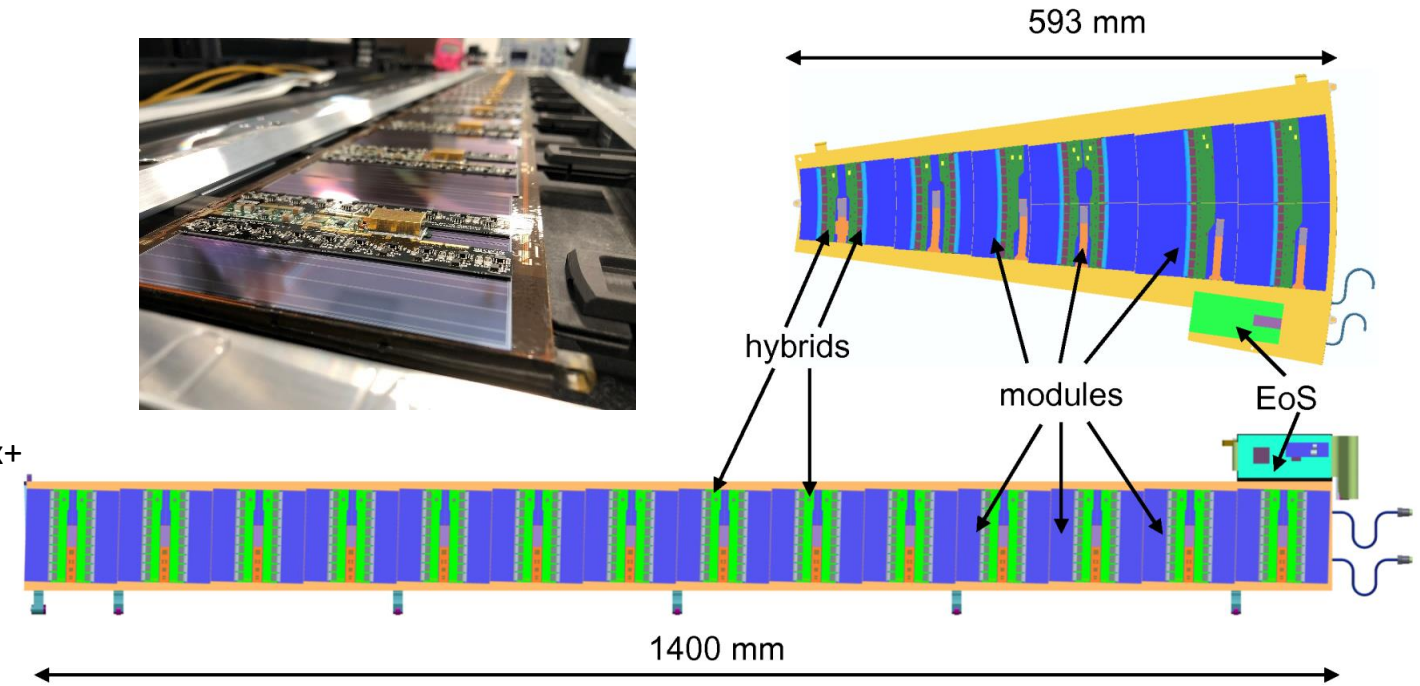
The Local Support Concept

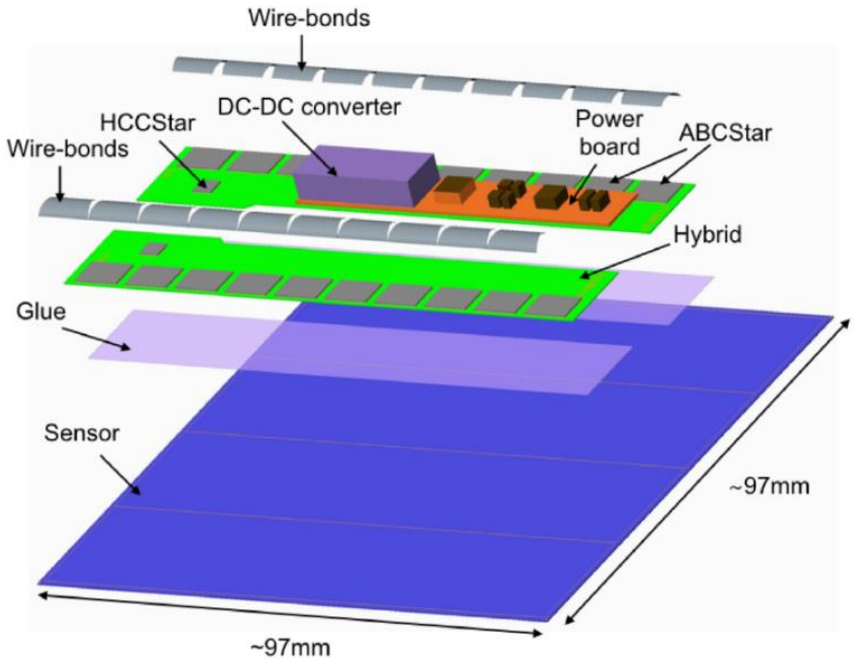
- Detector assembled from “medium” size local support objects
  - Barrel Staves and End-cap Petals
- Each Stave/Petal is a standalone system-level object providing:
  - Mechanical support and location control
  - Cooling
  - Power (LV & HV)
    - 1 LV bus per side
    - 4 HV buses per side
  - Trigger, control, clock signals
    - CERN Low Power Signalling (CLPS)
  - T, V, I monitoring
  - Data readout
    - Electrical-to-optical conversion at End-of-Substructure (EoS) card with lpGBT and VTRx+
- *Additional EoS material presented yesterday by Peter Gottlicher*

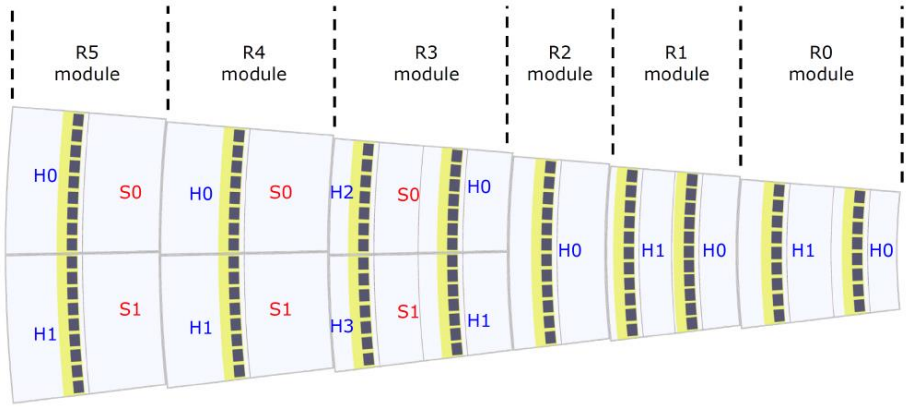




Modules

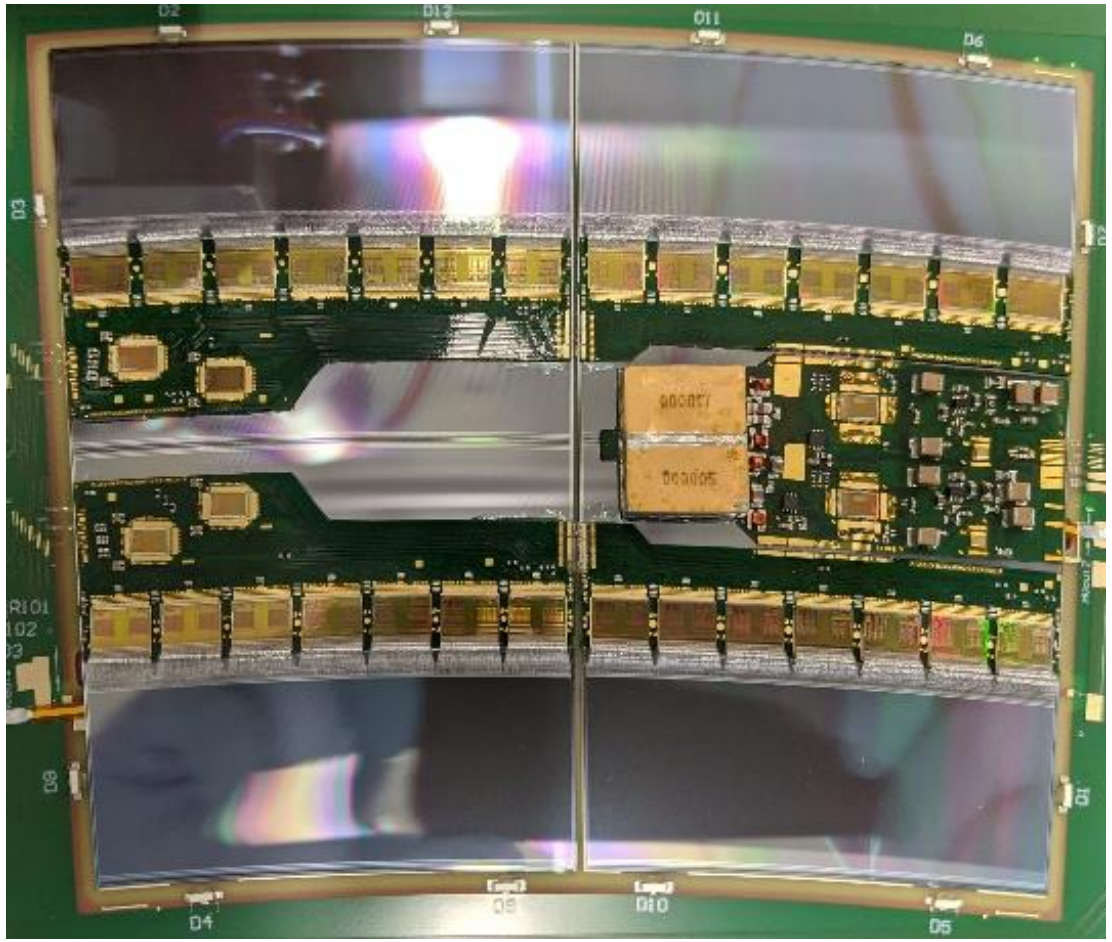
- All modules have same electrical architecture but with different geometries
  - 2 module variants in the barrel
    - Long strips and short strips
  - 6 module variants in the end-cap
    - R0 through R5
- Hybrids and powerboard are glued directly to sensor surface
  - Integrated module with good thermal management
- ITk Strip ASICs made in GF 130 nm CMOS technology
  - ABCStar Front End ASIC
    - 256 channels per chip
    - Point-to-point data connection to HCCStar at 160 Mbps
  - HCCStar Hybrid Controller Chip
    - Forwards data to lpGBT on EoS at 640 Mbps
- All interconnections made by aluminium wire-bonds
- Sensor HV bias via polyimide-insulated aluminium “tab” (not shown)



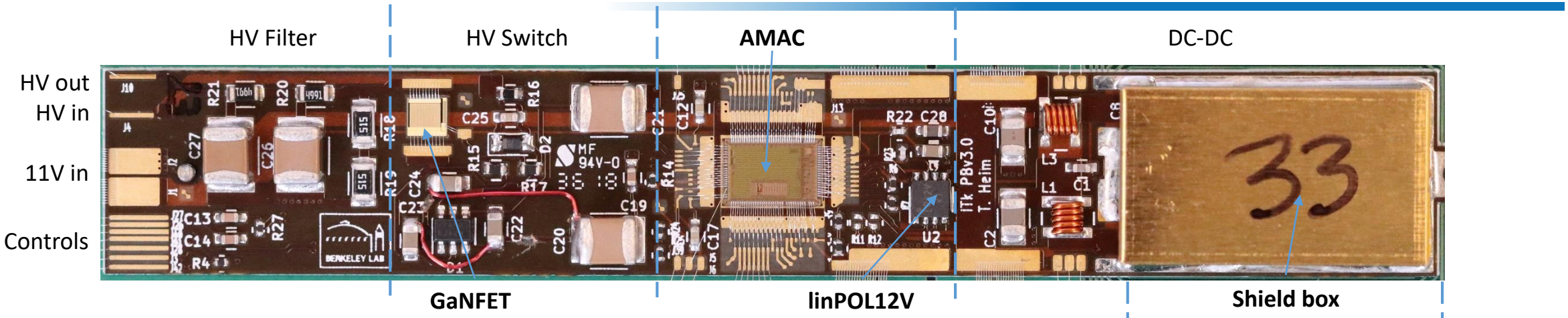


Split Modules

- Sensors for outer rings (R3, R4, R5) cannot be made from a single (6 inch) silicon wafer
- Modules made from two sensors utilising split hybrids
- Retains basic architecture with data on LHS and power from RHS
- Split halves of modules are built separately
- Connections between split hybrids made by wire-bonding

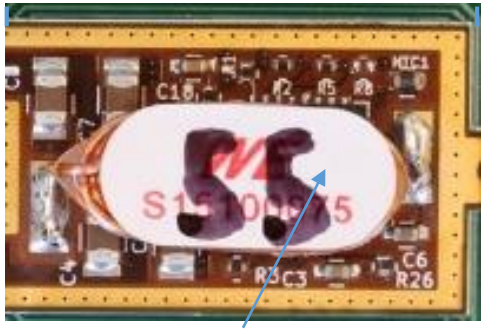


Powerboard



Barrel Powerboard PB 3.0

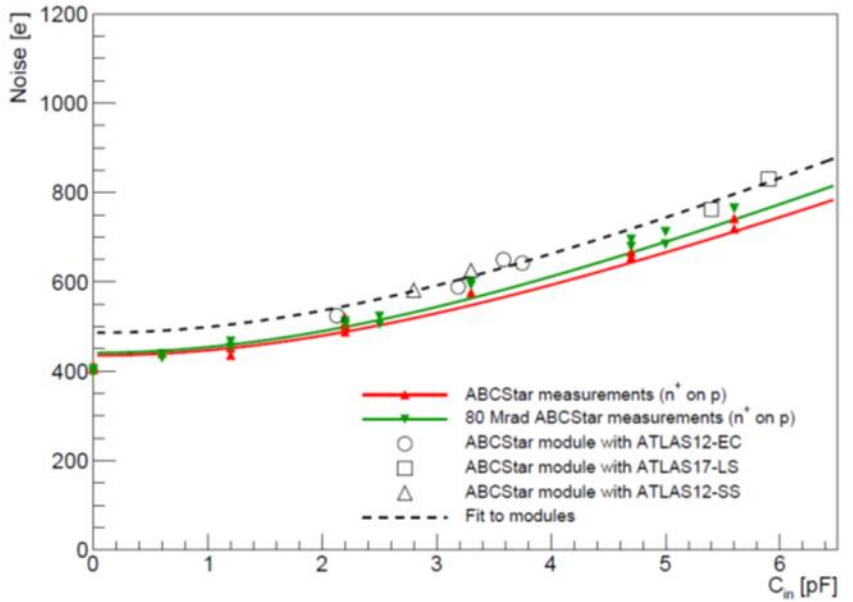
- The Powerboard (PB) is a separate circuit providing power, control, monitoring and autonomous interlocking
  - Autonomous Monitoring And Control (AMAC) ASIC
    - 16 channel, 10-bit Wilkinson ADC with additional signal multiplexers
    - Autonomous interlocking based upon local temperature and current readings
    - Powered by linPOL12V linear regulator (11 V in, 1.5 V out, always on)
  - bPOL12V DC-DC converter (11 V in, 1.5 V out to power hybrids, enabled by AMAC)
    - Low profile (5mm), 100 µm thick Al shieldbox, Au plated for soldering (upper figure)
    - Custom solenoidal coil due to clearance requirements (lower figure)
  - HV switch using commercial GaNFET under AMAC control
- One barrel PB layout (shown) and four endcap PB layouts (not shown)
  - Functionally similar but geometrically different



bPOL12V (under coil)

Module Results and End of Life Predictions

- Figure to right shows Short Strip, Long Strip, R0 and single chip noise results
  - Very little change in noise with radiation
    - *See presentation by Peter Everaerts yesterday*
  - **All within expectation**
- Module load capacitance taken from sensor probing measurements
  - Includes nearest neighbour, not next-nearest neighbour effects (~10%)
- Together with a knowledge of sensor behaviour the resulting fit may be used to estimate the end-of-life performance
  - The requirement of >99% efficiency and $<10^{-3}$ noise occupancy maps to a signal to noise ratio of 10:1
- **Prediction: better than 12:1 everywhere**



Layer/Ring	Barrel	Disk 0	Disk 1	Disk 2	Disk 3	Disk 4	Disk 5
0	15.8 [a]	15.1	14.8	14.4	13.9	13.3	12.2
1	-	17.3	17.0	16.5	16.0	15.2	14.1
2	16.2 [b]	17.9	17.5	17.0	16.4	15.7	14.8
3	-	19.1	18.7	18.2	17.5	16.7	15.7
4	-	15.1	14.8	14.4	13.9	13.4	12.7
5	-	14.8	14.5	14.1	13.6	13.1	12.5

a - worst case SS module
b - worst case LS module

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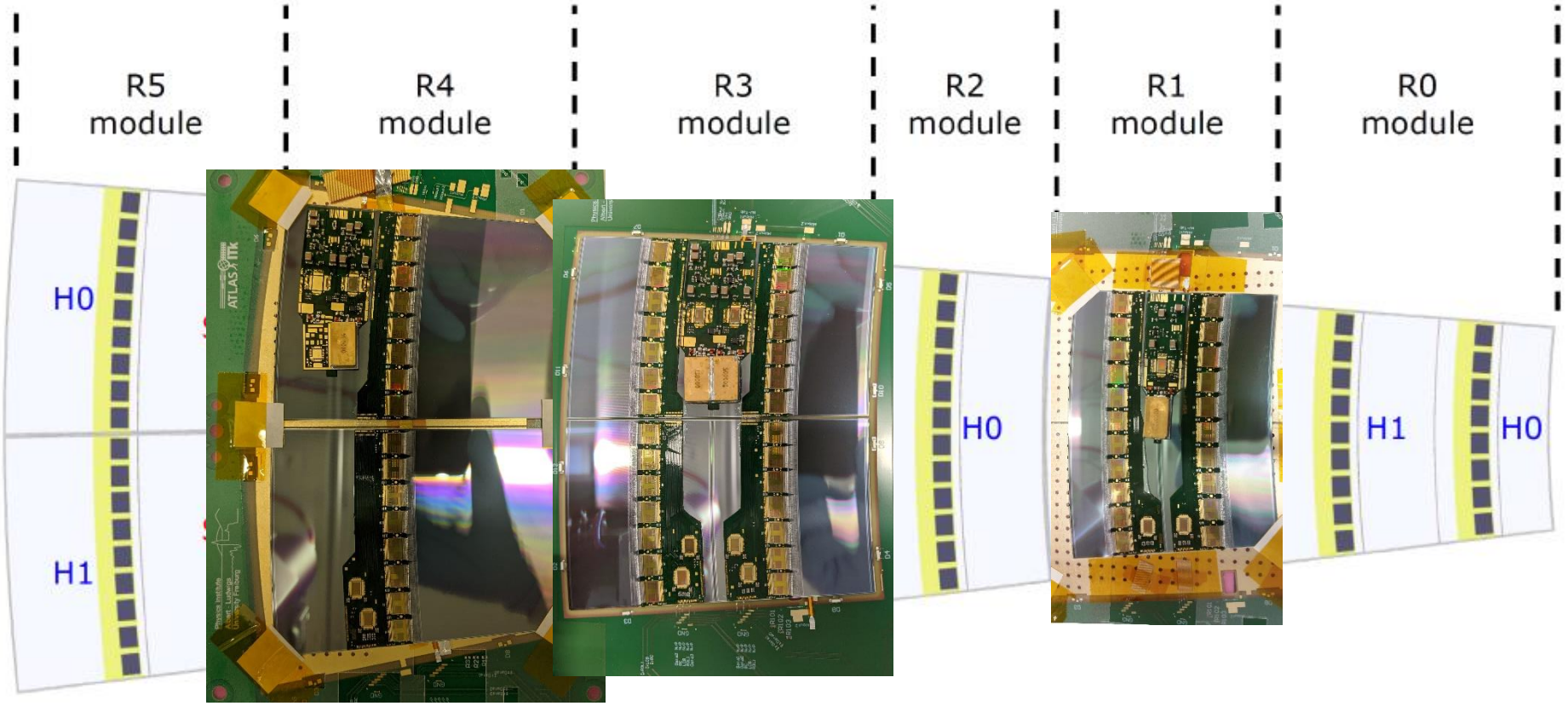
Petal Hybrids with ABCStar

A complete set of petal hybrids and powerboards was temporarily mounted on a bus tape and successfully read out using a direct electrical connection. Many parts have since been removed to build the first complete set of petal modules.

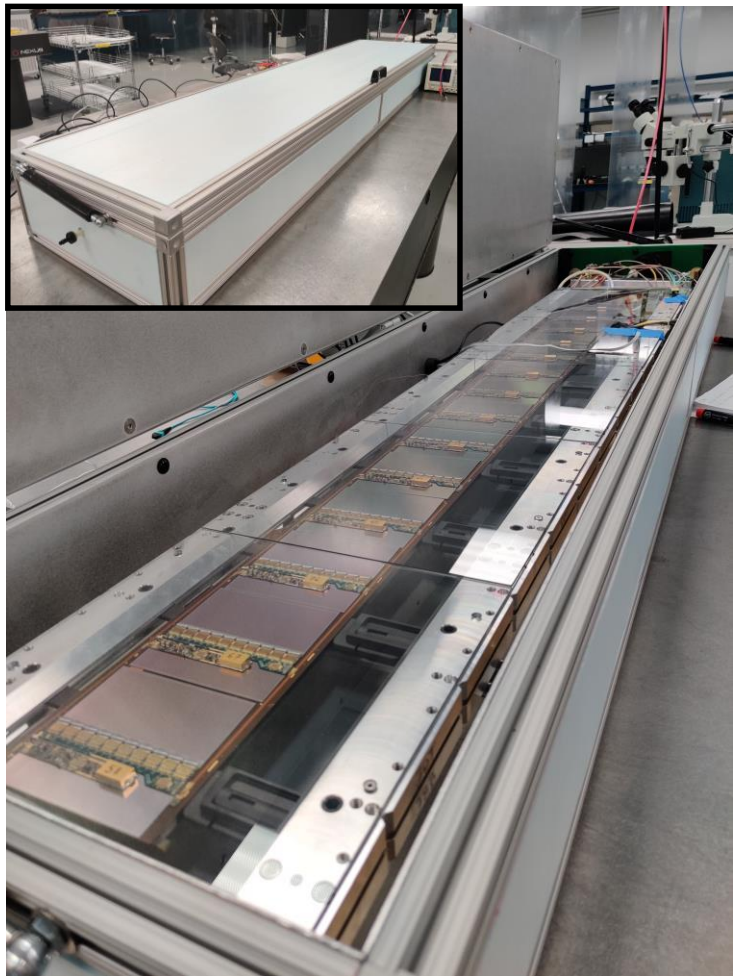
Petal Modules with ABCStar



Despite lockdown, the first R1, R3 and R4 modules have recently been completed and are undergoing testing. Next up will be R5, then R0, then finally R2. A complete petal side with EoS equipped with lpGBT should be ready for test a few weeks from now, followed by a double sided petal soon thereafter.

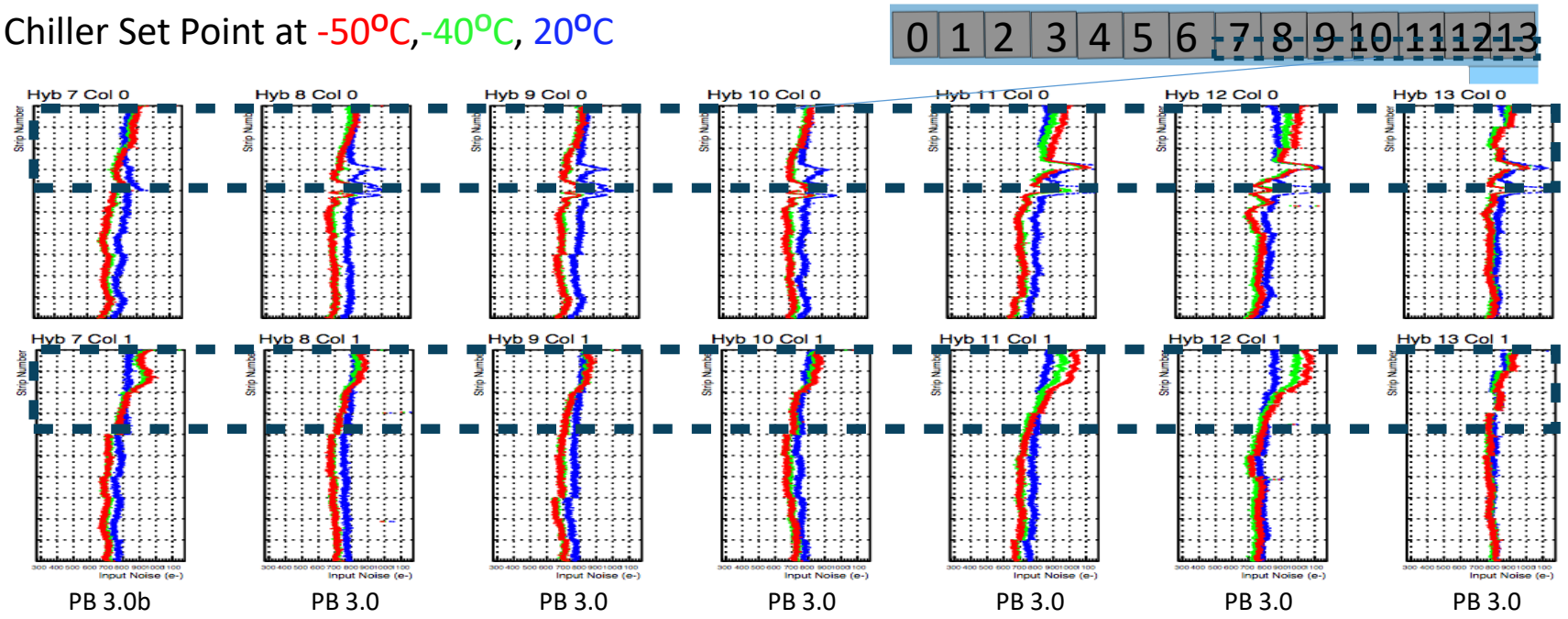
Fully loaded, Double Sided Long Strip Stave

- A stave cold box was built at BNL to facilitate thermal cycling and electrical tests at expected operating temperature
  - System uses “NOVEC” engineered coolant
  - 15^{O}C differential between chiller output and stave input
- The LS stave was completed at Brookhaven National Laboratory in February 2020
  - Most modules use powerboard version PB 3.0 with 0.5 oz copper planes
  - Two modules (6 and 7) use PB 3.0b with 1.0 oz copper planes
- Room temperature performance was satisfactory
  - Known noise peaks correlated with PB 3.0 much reduced on modules with PB 3.0b (next slide)
- Strip modules of several generations (ABCN25, ABC130, ABCStar) had been tested cold before
  - Performance has always been satisfactory
  - We had no reason to suspect a complete stave would behave differently
  - But it did...



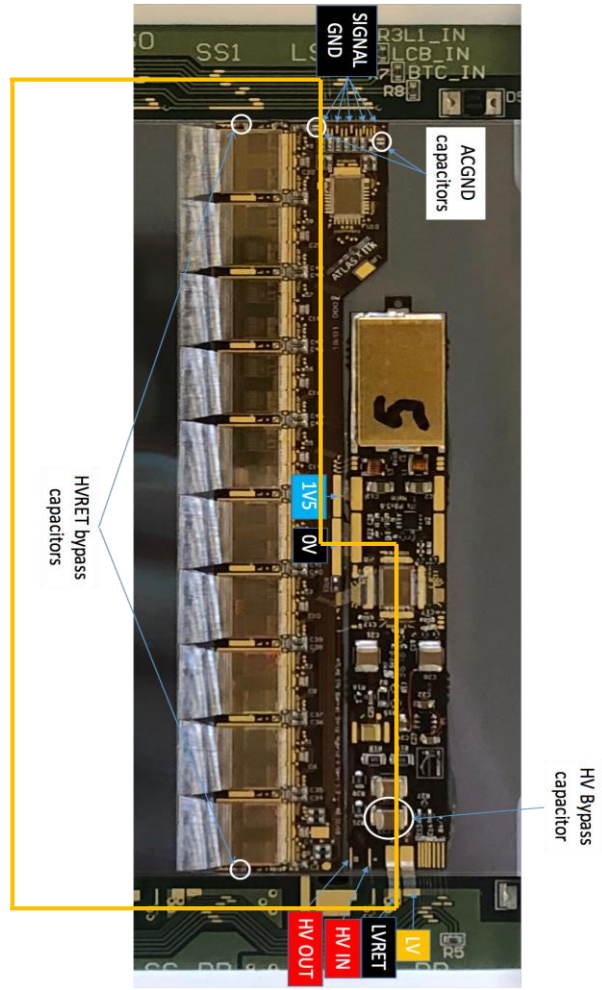
Long Strip Stave: Cold Test Results

Chiller Set Point at -50°C,-40°C, 20°C



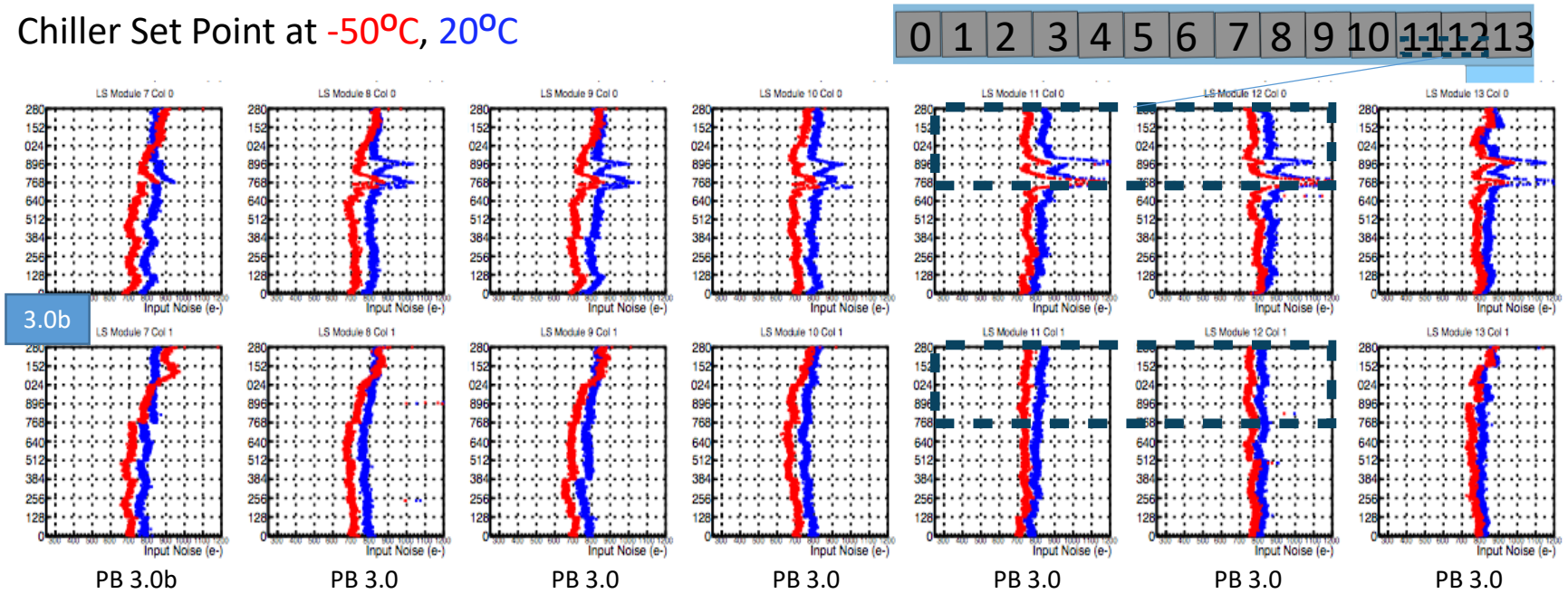
PB 3.0b PB 3.0 PB 3.0 PB 3.0 PB 3.0 PB 3.0 PB 3.0

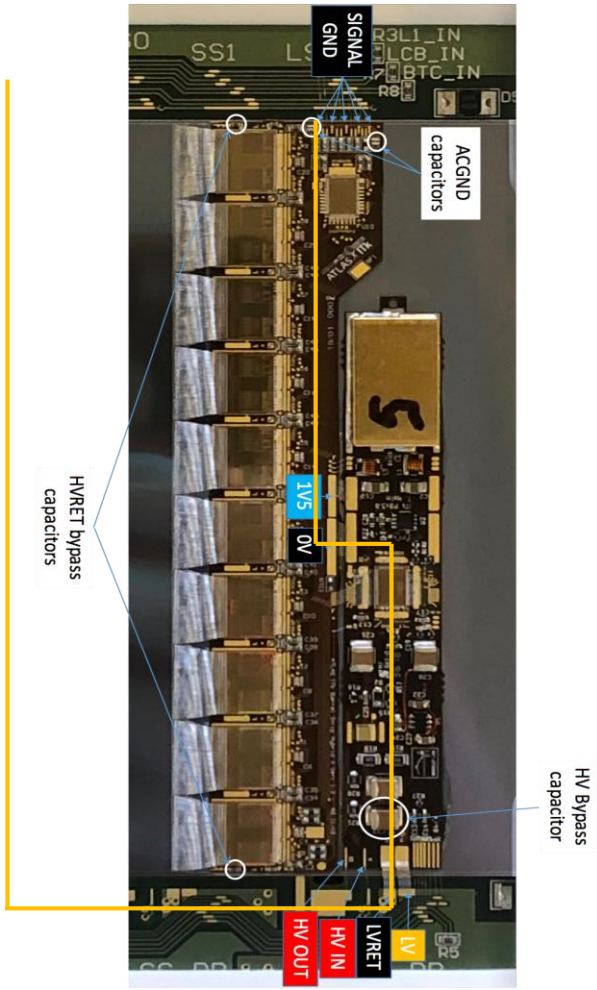
- Noise increases as T decreases in the upper half of each hybrid and towards EoS
- What is the aggressor here?
  - Temperature dependent noise decreases as DC-DC input voltage is reduced (see backup)
- How does this couple into the upper half of each hybrid?
  - Presence of an AC coupled Signal Ground connection adjacent to HCCStar, intended to control common mode voltages on the fast signalling, provides a route for noise currents to flow through the upper half of the hybrid (yellow line). This violates the intended "Star" ground of the module.



Long Strip Stave: Effect of removing Signal GND bonds

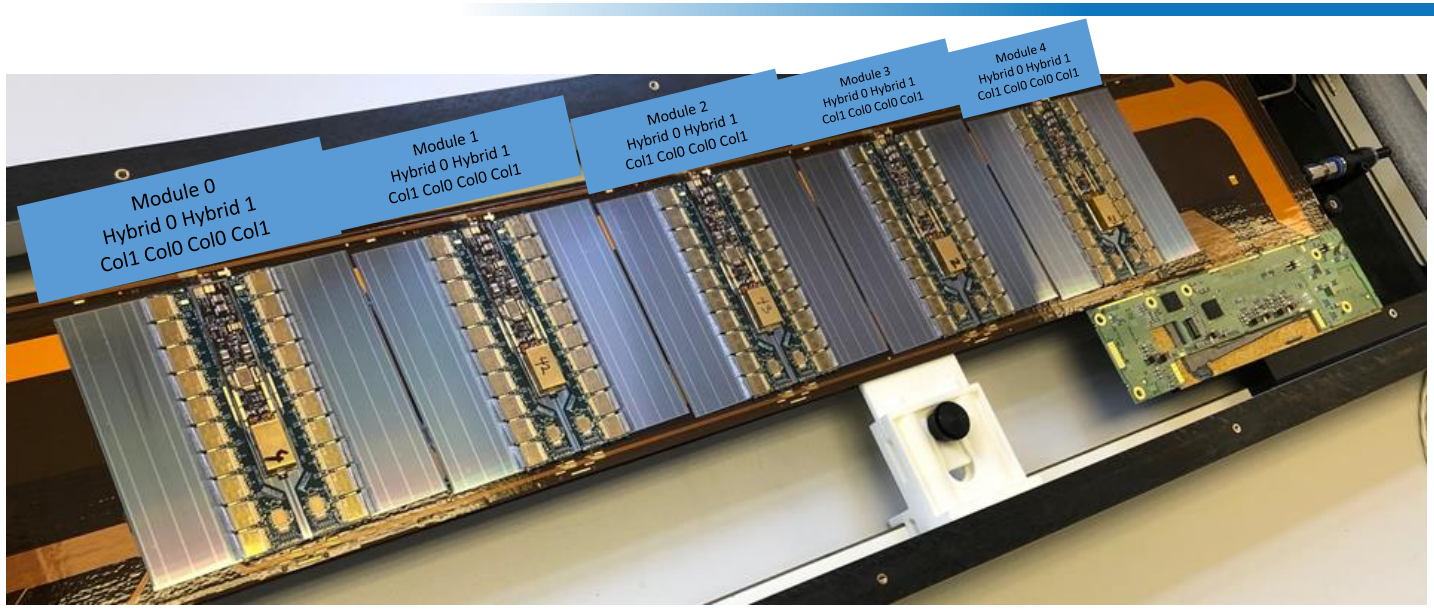
Chiller Set Point at -50°C, 20°C





- Signal GND bonds removed from modules 11 and 12
  - Increased noise is gone!
- Follow-up tests post COVID-19 to include
  - Removal of all Signal GND bonds (both sides of stave)
  - Magnetic trigger Noise Occupancy Tests
- **We are optimistic that satisfactory performance of the LS stave at low temperatures will be obtained after removal of all Signal GND bonds**

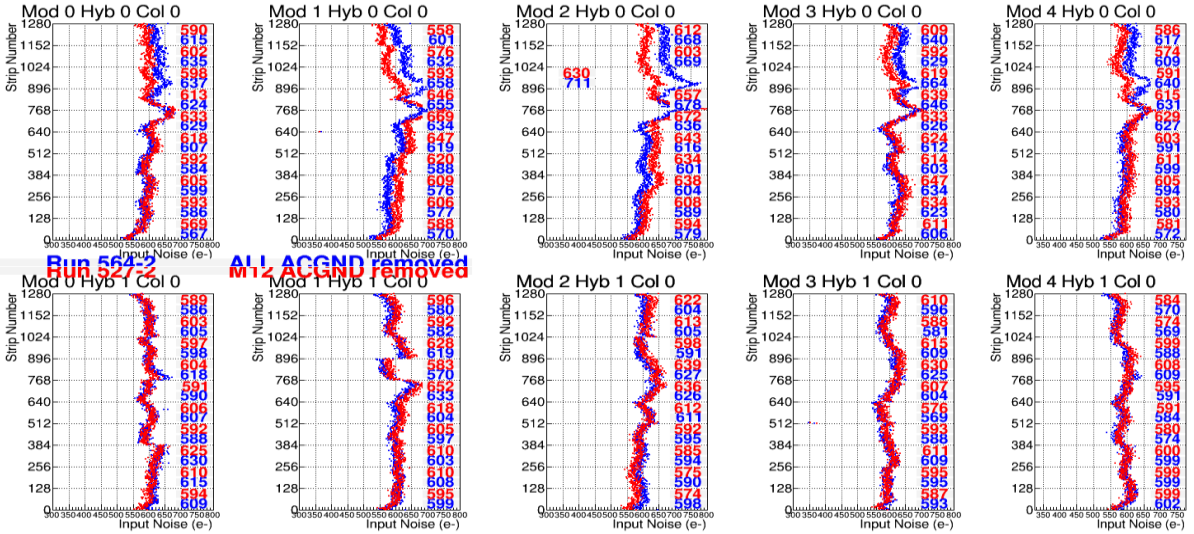
5SS Short Strip Stave



- Built at RAL primarily to test digital communications on the stave
  - CLPS control buses split into segments of 4 / 4 / 5 / 1 modules: 5SS represents the most heavily loaded case
  - No issues with digital communications
- Modules all built with powerboard PB 3.0 with ½ oz copper planes
  - Aside from known spikes from inadequate PB shielding, analogue results at room temperature were good
- 5SS was built with the signal ground bonds in place
  - Whilst we cannot yet run staves cold at RAL, we could at least pull the signal ground connections to study their effect at room temperature.

5SS: Effect of removing Signal GND bonds

RED: ACGND ON BLUE: ACGND OFF



Input Noise (e-) for inner column of each hybrid

- Effect of removal of Signal GND
  - Hybrid 1s get slightly less noisy
    - Same hybrid as LS stave
    - Same result ☺
  - Hybrid 0s get much more noisy
    - "Mirrored" hybrid wrt LS stave
    - Different result ☹

- Not fully understood where this asymmetry comes from
  - However the DC-DC "hot loop" in which switching currents at 11V flow routes primarily over the strips served by Hybrid 0
- Signal ground was not bonded on the three short strip staves built with the ABC130 chipset, and they did not show this effect
  - With powerboard version PB 2.0
- We will "fast track" construction of an additional SS module built with PB 3.0b (1.0 oz copper) and add it to 5SS
  - Will this reduce the effect?
- Pre-production powerboard PB 3.1 will have additional improvements
  - Reduce impedance of "hot loop"
  - Restoration of current free bottom layer (electrostatic shield)
- Design work continues at RAL to be able to run 5SS cold as soon as possible

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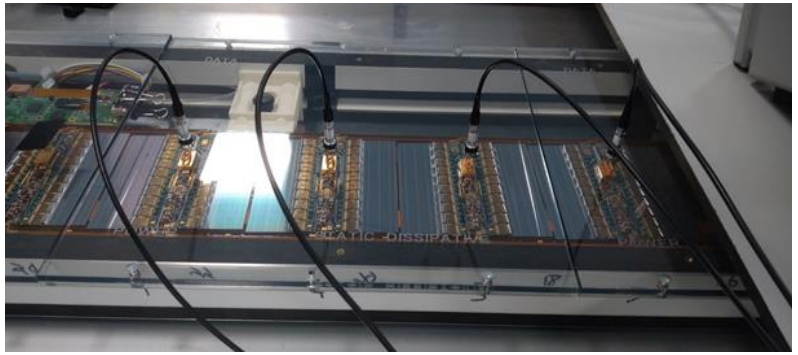
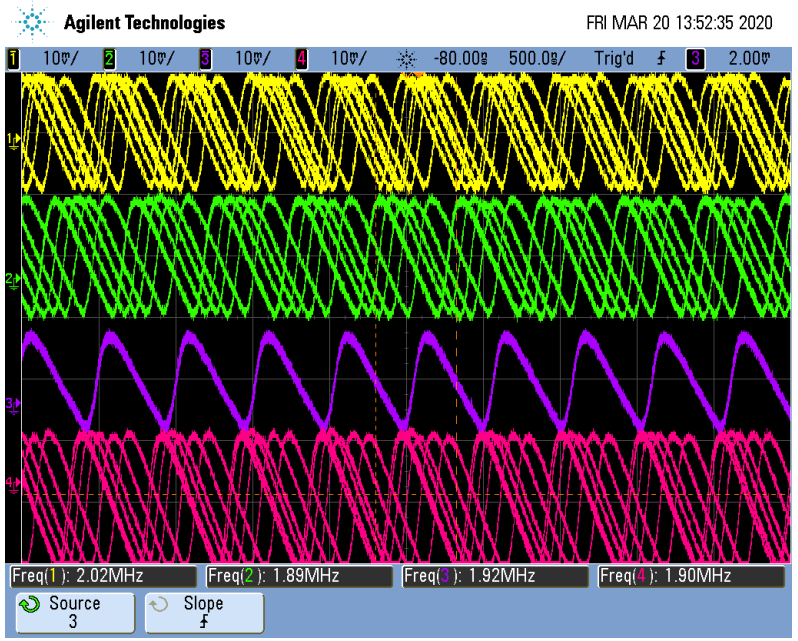
5SS: Magnetic Trigger Setup

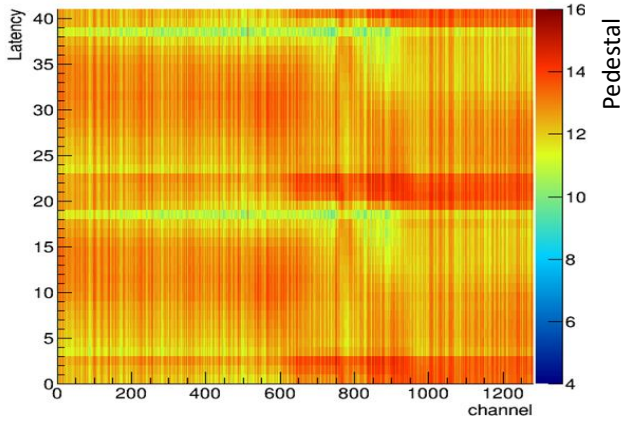
- A trigger coil is mounted above each of four powerboards to pick up the DC-DC switching frequency
  - spare PB solenoids are used
- The scope is used to form a trigger off the selected channel
  - This is fed into the DAQ system and subjected to a programmable delay in order to trigger at specific points in the switching cycle
- At each phase (latency) we record a threshold scan without injecting any calibration charge
- The system can run automatically across four modules in a few hours (ideally overnight)
  - Tests were first made with the ACGND bonds on, then with ACGND bonds off
- The data is processed offline to determine how the effective pedestal (amplifier offset) varies at different points in the DC-DC cycle

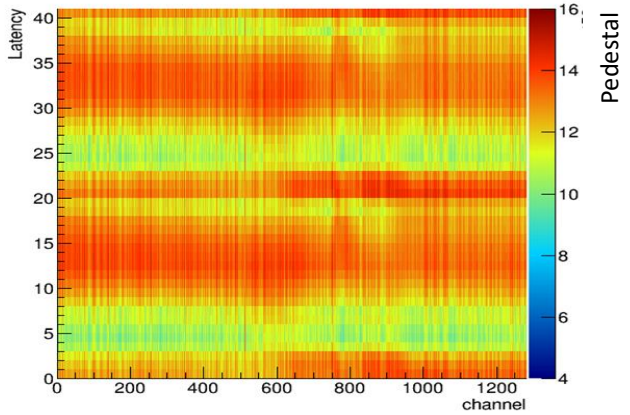




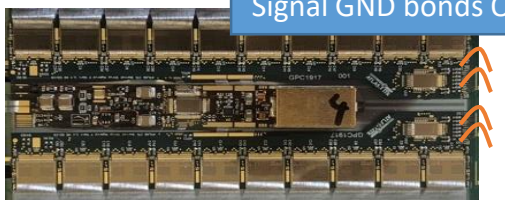
5SS: Magnetic Trigger Result for Module 3

Hybrid 1
Inner Column

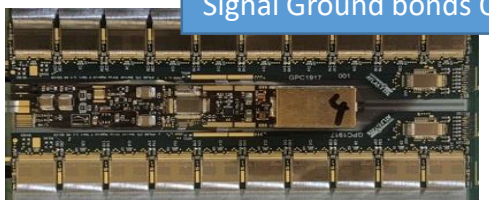




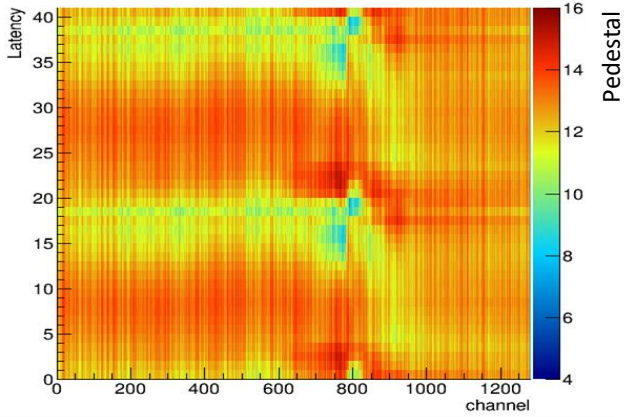
Signal GND bonds ON

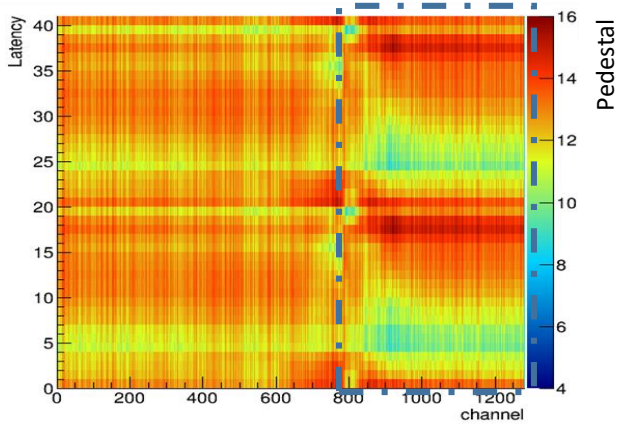


Signal Ground bonds OFF



Hybrid 0
Inner Column





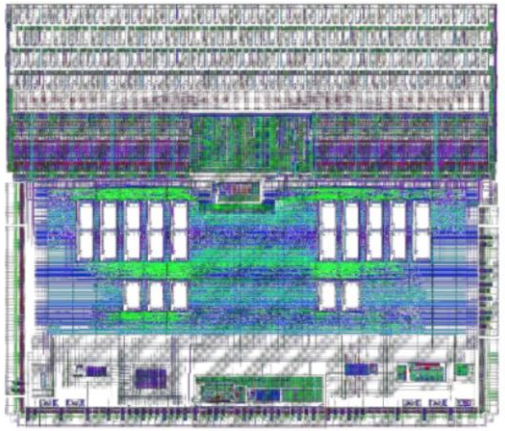
Pedestal shift consistent with ENC results.
Removing the Signal GND connection:

- Hybrid 1s get slightly less noisy
- Hybrid 0s noisier (last four chips)
  - more dark red and cyan is visible, indicating increased movement of the effective pedestal

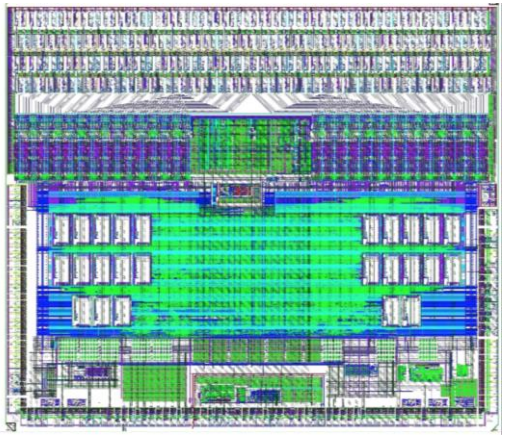
- Another effect of the removal of the signal ground connection is that the other modules of the stave are affected less by the operation of M3's DC-DC (backup slides)
  - but unlike the effect on M3, the effect upon the other modules was already negligible...

Coming Soon: Pre-production ASICs

- ASIC designs being revised for pre-production
  - Main motivation: improved SEE and SET protection
  - *See presentation by Peter Everaerts yesterday*
- ABCStar
  - Full triplication of clocks and resets using the Triple Module Redundancy Generator (TMRG) tool
  - To compensate for the power taken by the additional logic a number of power saving measures were adopted. For example:
    - Clock gating
    - Compression of the register map
    - Minimisation of data output circuitry clocked at 160 MHz
- AMAC -> AMACStar (Simplified, Triplicated And Respun)
  - Total area is fixed: design simplified to make room for the full triplication of clocks and resets
    - Number of ADC channels which feed into autonomous interlock decisions cut from 16 to 12
    - Thresholds changed from windowed (high **and** low) to single-sided (high **or** low as appropriate)
  - Internal clock frequency reduced from 40 MHz to 20 MHz to save power
- HCCStar
  - Total area is fixed: not possible to implement full triplication
  - Goal is to prevent persistent errors
    - Allow low rate of short periods or incorrect data which self-correct
- Timescales
  - ABCStar submitted in February 2020 and left the foundry this month
  - Common submission of HCCStar and AMAC expected mid-summer (at earliest)



Prototype ABCStar



Pre-production ABCStar

Pre-production, Production and Beyond

- Prototyping phase of the project is very much wrapping up
  - All Preliminary Design Reviews (PDRs) have been passed
  - Many Final Design Reviews (FDRs) have been passed or are imminent
- Module parts are starting to become available
  - Pre-production sensors starting to arrive
  - One pre-production ASIC is back from the foundry, others will be submitted soon
- Staggered arrival of pre-production ASICs leads us to split our pre-production programme into two parts
  - Pre-production “A” with pre-production ABCStar, prototype HCCStar and AMAC
  - Pre-production “B” with pre-production ABCStar, HCCStar and AMACStar
  - 5% of the total number of modules (and staves/petals) will be built in 1 year
- Provides full validation of the production chain with parts fed into system test setups
  - Systems FDR to confirm system performance before production starts
  - System test hardware subsequently forms long term setups for future DAQ and DCS developments
- Following preproduction we have one more review, the Production Readiness Review (PRR)
- Production starts (Q3 2021)
  - We will build 18,000 modules in 3.5 years!

Summary and Outlook

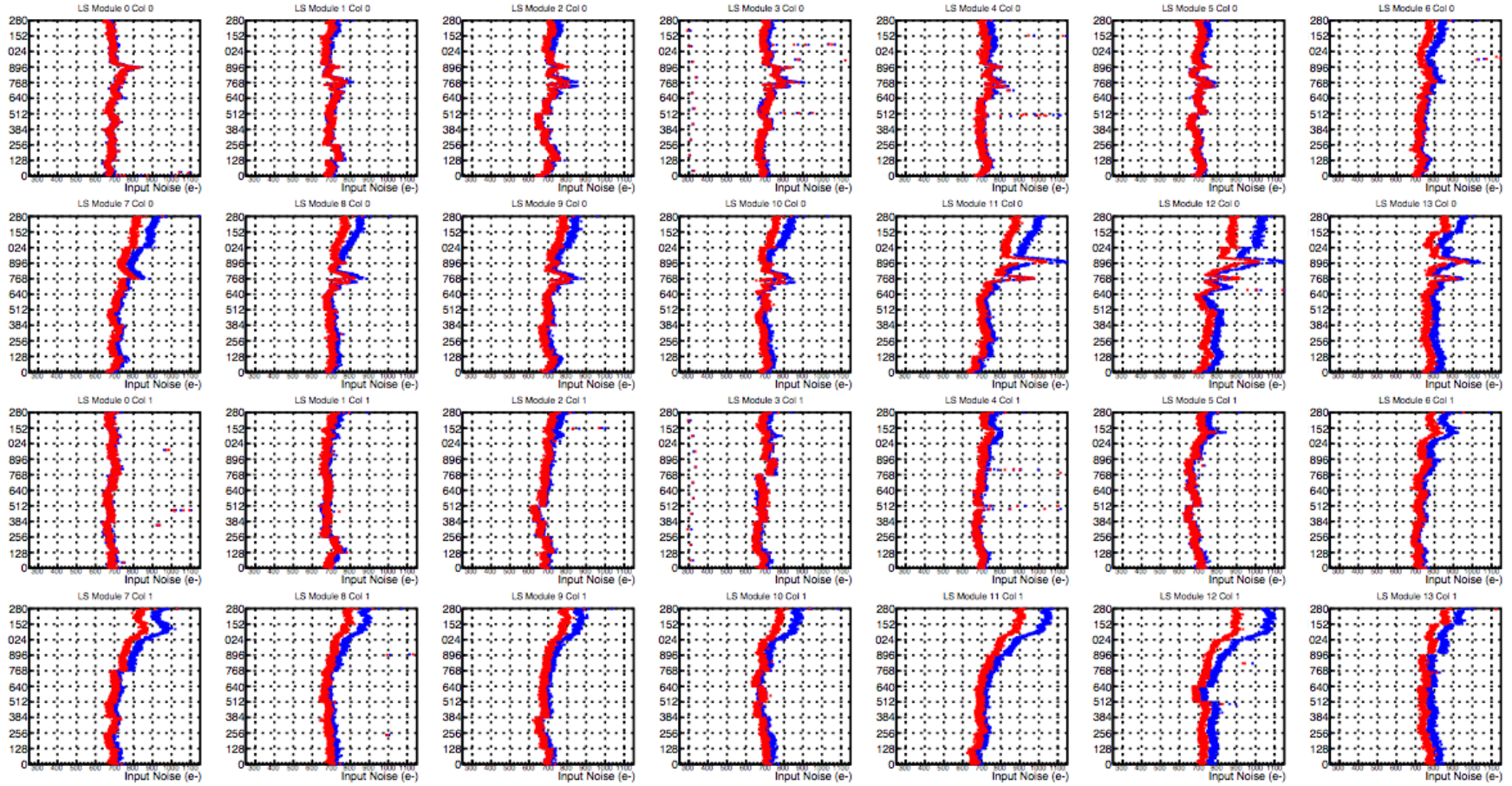
- Prototype chipset performance is excellent in all regards except SEE
  - Pre-production designs will address this
- Construction of modules for first petal with ABCStar chipset underway
  - Expect first results soon
- Unexpected “cold noise” effect found during Long Strip Stave testing
  - Evidence to date suggests this will be resolved by removal of the Signal Ground connection
- Removal of Signal Ground connection from a Short Strip Module introduces asymmetry to noise results
  - Subject to cold test data we could probably live with this, but would like to do better
  - Optimistic powerboard PB 3.0b (and 3.1) with 1 oz copper will reduce this effect
- Looking forward to Pre-production!

BACKUP

Long Strip Stave: Cold noise vs DC-DC input V

DC-DC input voltage: 11V vs 10V

Chiller Set Point at -50C

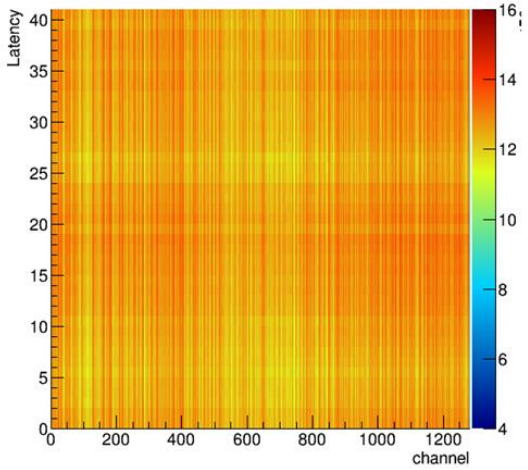


- Reducing input voltage to DC-DC reduces noise increase

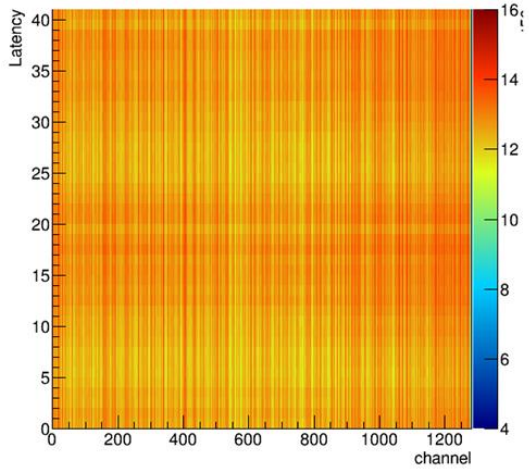
Master

Triggering M3 Hyb 0 Stream 0, Signal GND ON

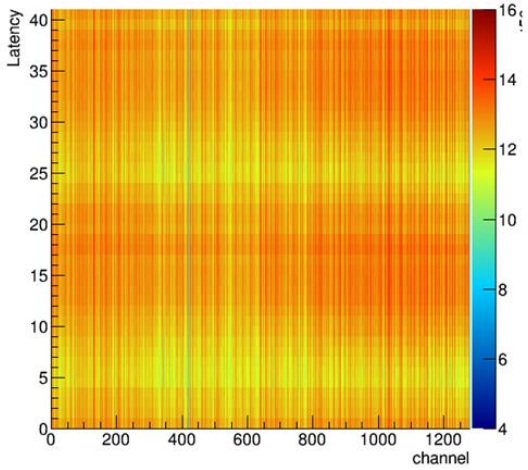
M0



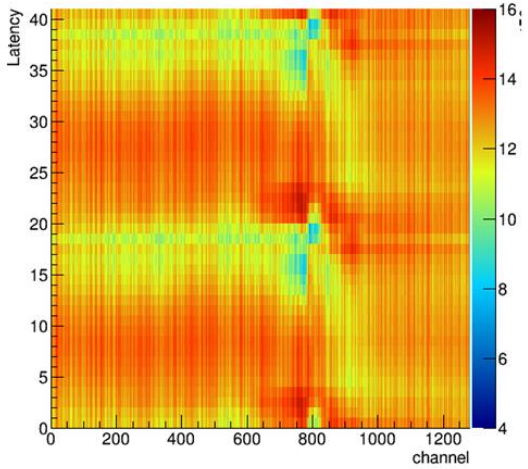
M1



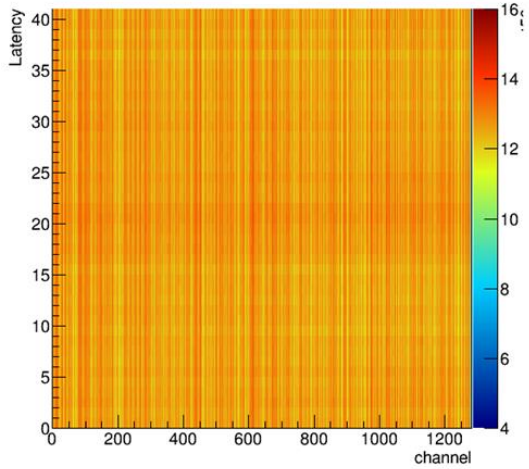
M2



M3



M4

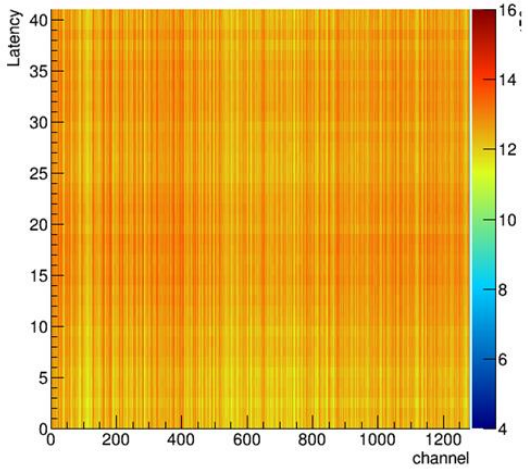


Strips **under** PB

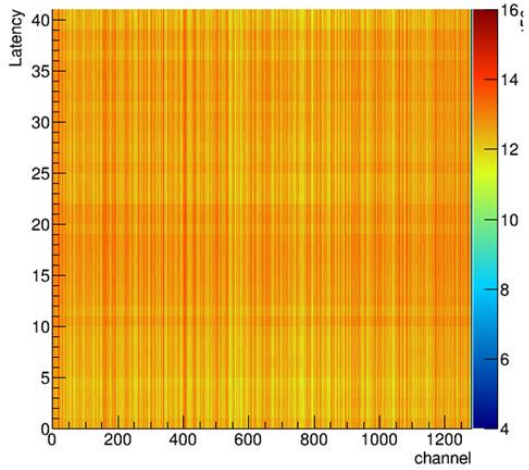
Signal GND **present** on all hybrids

Triggering M3 Hyb 0 Stream 0, Signal GND OFF

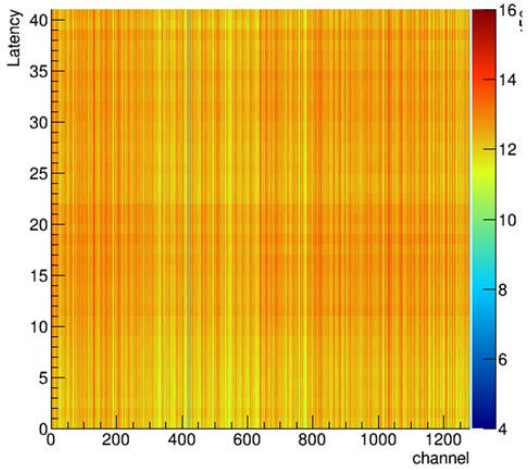
M0



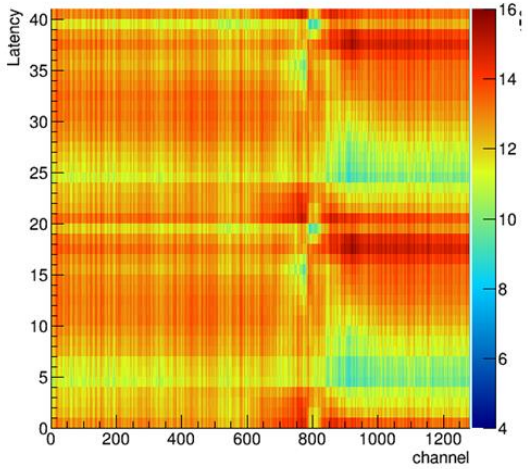
M1



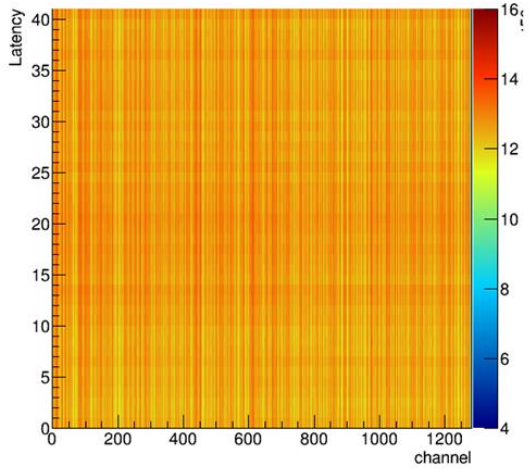
M2



M3



M4

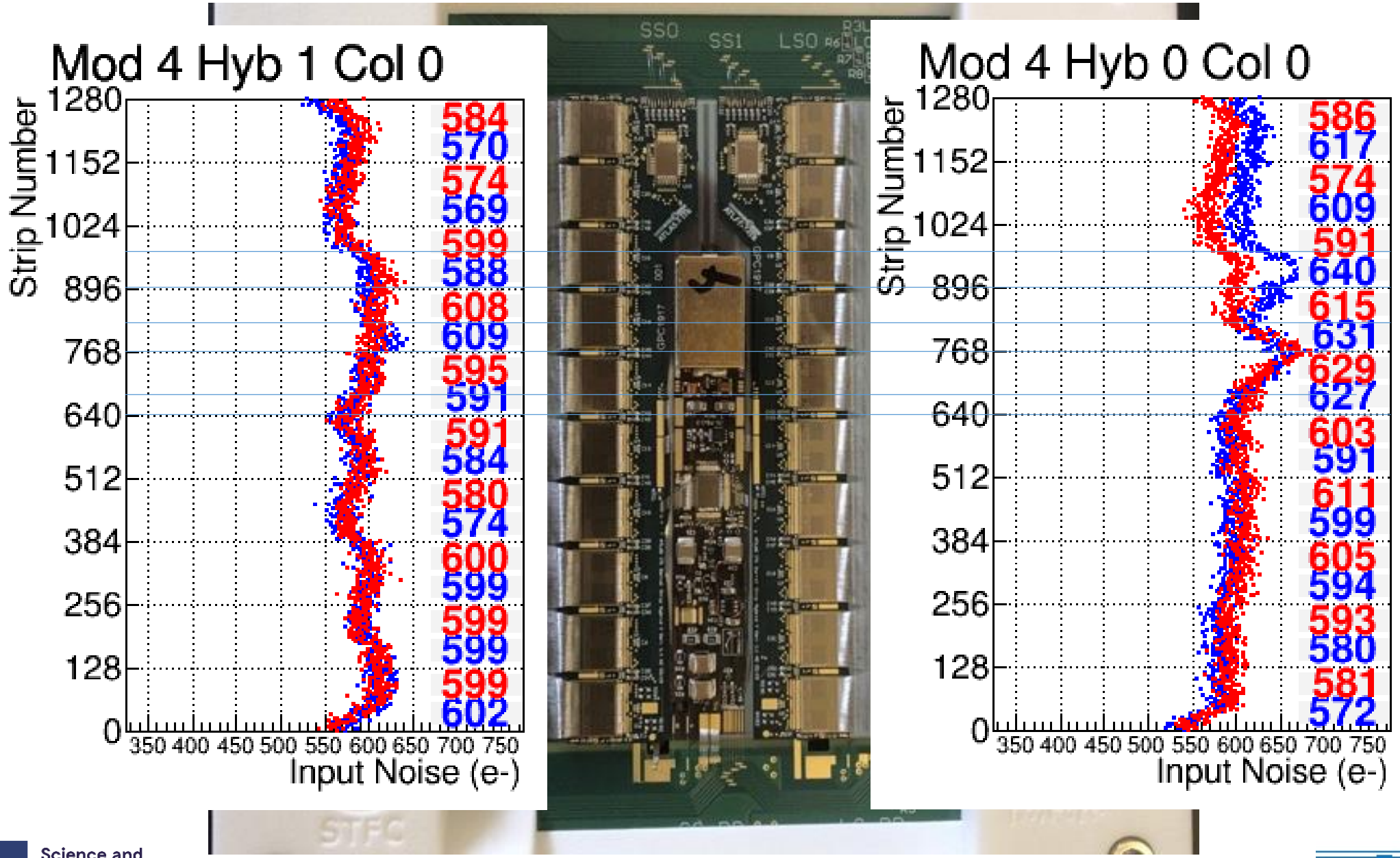


Striping reduced in modules 0,1,2 and 4

Strips **under** PB

Signal Ground **removed** from all hybrids

RED: ACGND ON BLUE: ACGND OFF



Barrel Powerboard Versions & Stackup

Version	Top	In1	In2	Bottom	Usage	Noise Bumps?
1.0	1.0	1.0	1.0	1.0	Early ABC130 prototypes	No
2.0	0.5	0.5	0.5	0.5	ABC130 prototypes	Yes
3.0	0.5	0.5	0.5	0.5	ABCStar prototypes	Yes
3.0b	1.0	1.0	1.0	1.0	2 modules on Long Strip Stave	Barely Visible
3.0c	0.5	1.0	1.0	1.0		???
3.1	0.5	1.0	1.0	1.0	Pre-production	???
	oz	oz	oz	oz		

Approximate copper thicknesses are: 0.5 oz = 17.5 microns, 1.0 oz = 35 microns.
At room temperature the skin depth of the second switching harmonic 3.6 MHz is 34.4 microns.
The use of 0.5 oz copper for power and shield layers was an unfortunate mistake.
(For the top layer, with fine tracking for wire-bonded ASICs, 0.5 oz is necessary for high yield.)