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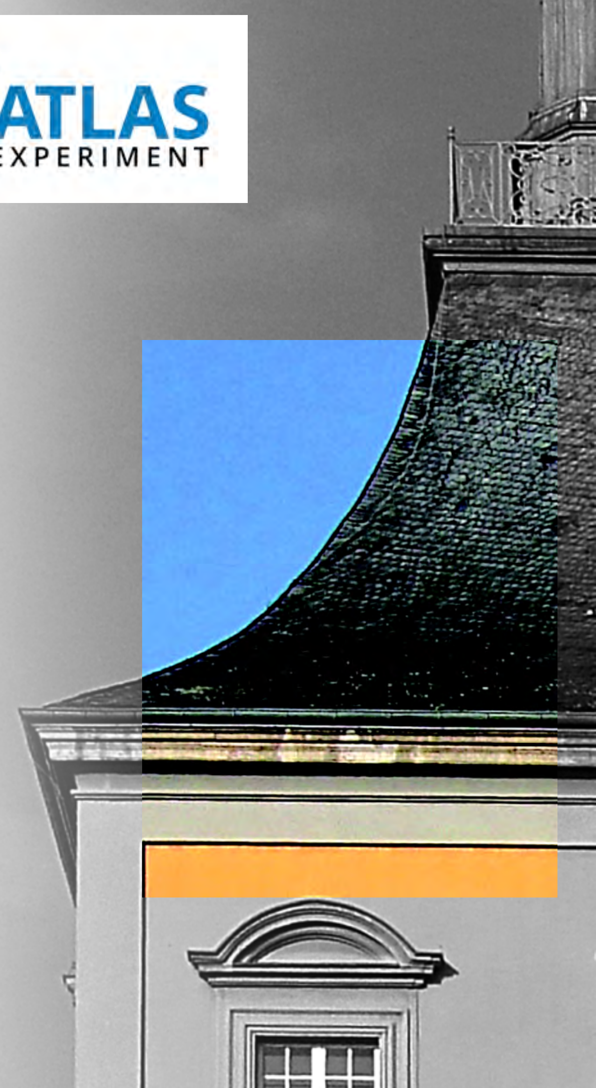
ATLAS ITk

ATLAS EXPERIMENT

ATLAS ITK PIXEL DETECTOR FOR HL-LHC

ACES 2020, CERN, MAY 26 - 28, 2020

FABIAN HÜGGING, UNIVERSITY OF BONN
ON BEHALF OF THE ATLAS ITK COLLABORATION



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OUTLINE

- Introduction
  - HL-LHC challenges
  - Layout of the ATLAS ITk Pixel Detector
- The ATLAS ITk Pixel Detector for HL-LHC
  - System Design
    - Powering scheme
    - Data transmission
    - Readout and trigger concepts
  - Pixel readout chip: RD53A & ITkPixV1 (RD53B)
  - Pixel sensors
    - 3D sensors
    - Planar sensors
  - Pixel Modules
- Conclusions

HL-LHC SCHEDULE

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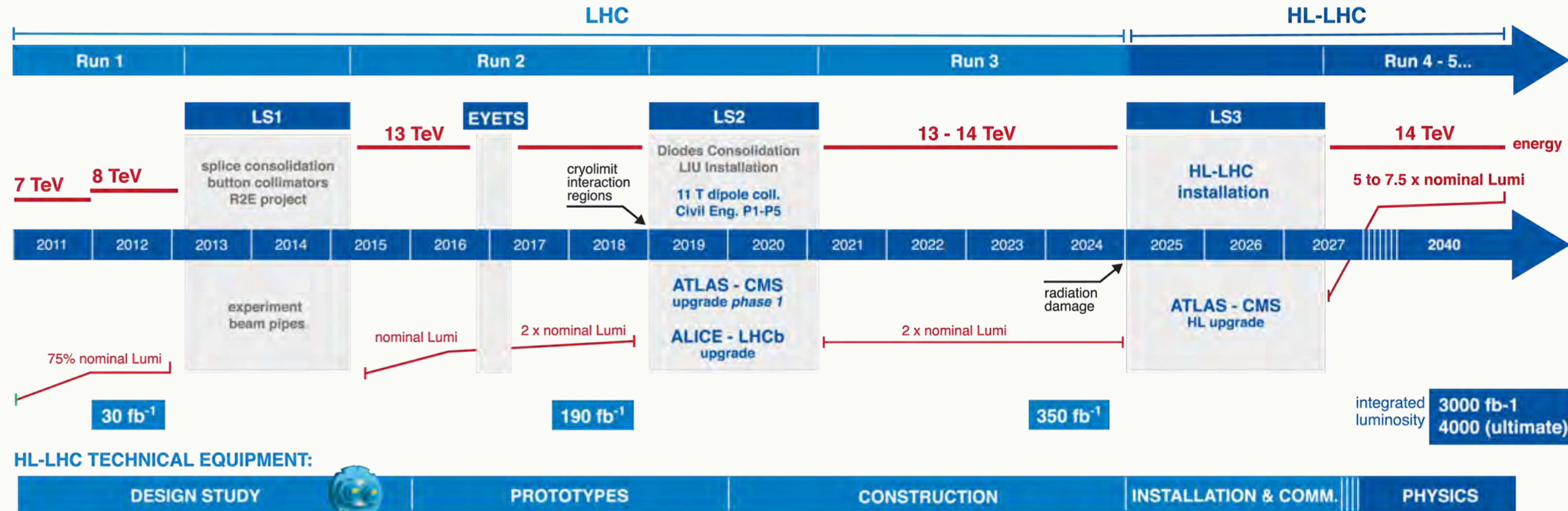
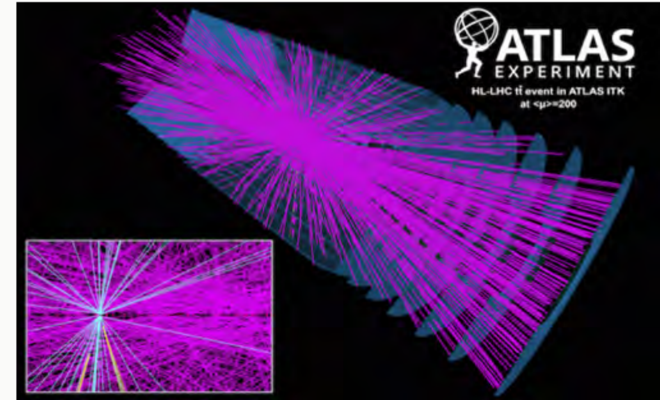


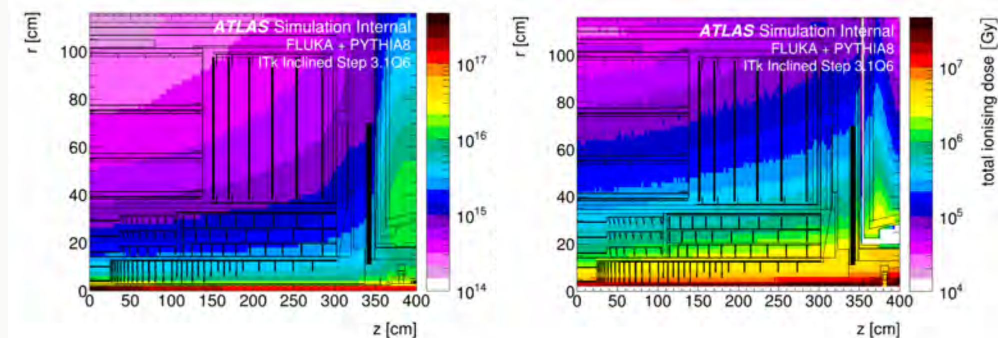
The LHC will be upgraded to the High Luminosity-LHC (HL-LHC) to produce up to 4000 fb^{-1} of integrated luminosity until 2035 and beyond

- benefits precision measurements in many physics channels
- allows studies of rare processes

INCREASING LHC LUMINOSITY: WHAT ARE THE CHALLENGES?

- HL-LHC luminosity ~$7x10^{34}cm^{-2}$
  - About x3.5 times Run-2 peak luminosity
- Increased luminosity → Increased pile-up:
  - Up to 200 pile-up events expected at the HL-LHC compared to ~34 in Run-II data
  - Increased pile-up compromises pattern recognition
  - Increased readout rates → increased trigger rates and latency requires multi-gigabit data transmission and large on-chip buffering
- Increased luminosity → Increased radiation damage:
  - Damage scales approximately linearly with luminosity ~x10 increase





ATLAS INNER TRACKER (ITK)

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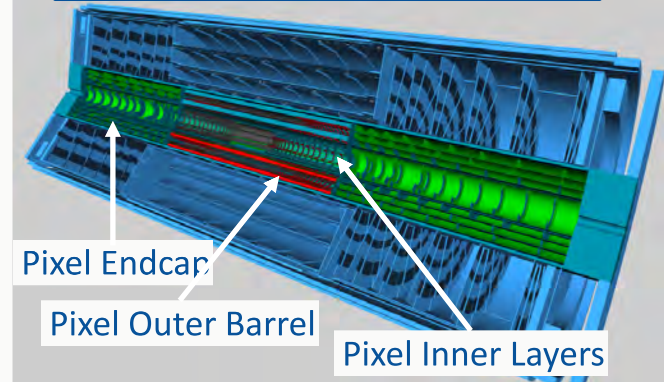
The current inner detector system will be replaced with a new all-silicon tracking system → ITk

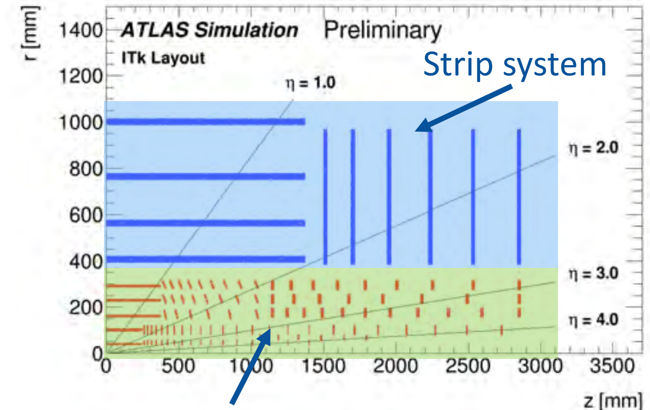
- Coverage up to |η| < 4 with ≥ 13 hits / track (barrel) & ≥ 9 hits / track (forward)

Requirements for ITk pixel detector:

- Same or better performance than current Inner Detector:
  - Track reconstruction efficiency > 99% for muons & > 85% for electrons and pions
  - Increased granularity to maintain fake rate < 10^{-5}, occupancy < 1% and robustness against loss of 15% of channels
- Low mass mechanics, cooling and serial power to minimize material:
  - Material budget ~ 1.5-2.0% X/X_0 per layer
- Fast readout with trigger rate 1-4 MHz and output bandwidth up to 5.12 Gb/s per front-end chip
- Increased radiation hardness up to $2 \times 10^{16}\ n_{eq}cm^{-2}$ & 10 MGy (TID)

ATLAS ITk





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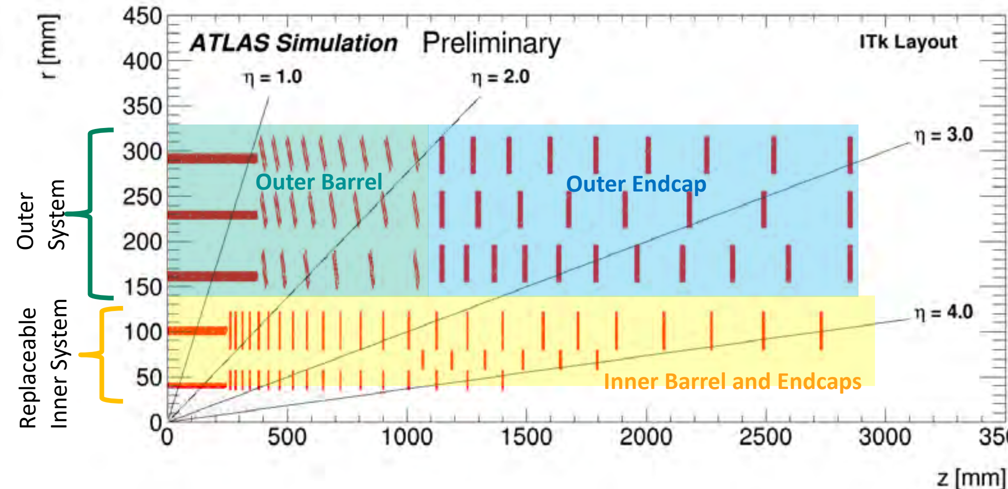
ITK PIXEL DETECTOR LAYOUT

Outer Barrel:
3 layers of flat staves and inclined rings
n-in-p planar quad modules
4472 quad modules, 7.2m^2
2.3x10^{15}n$_{eq}$cm^{-2} & 1.7MGy @4000fb^{-1}

Forward pixels:
3 layers of rings
n-in-p planar quad modules
2344 quad modules, 3.75m^2
3.1x10^{15}n$_{eq}$cm^{-2} & 3.5MGy @4000fb^{-1}

Current pixel system:
~92M pixels
~2000 modules
~1.9m^2 active area

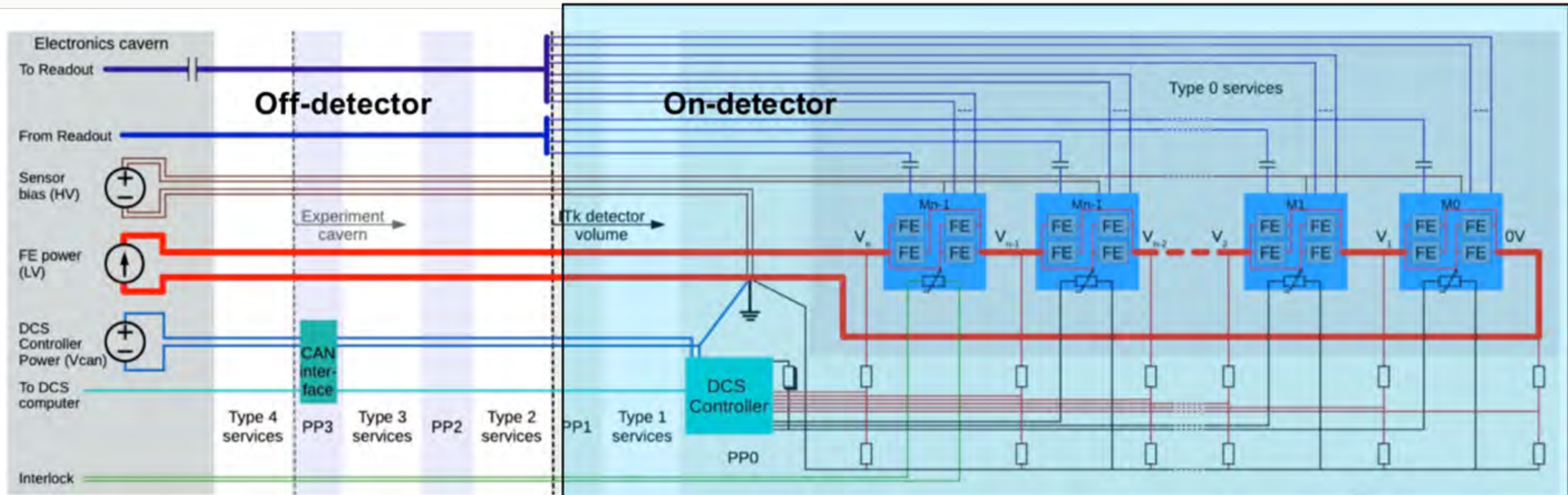
ITk Pixel System:
~1.4G pixels
~9400 modules
~13m^2 active area



Layout and performance described in ATL-PHYS-PUB-2019-014

Inner System ***Replaceable:***
2 layers of flat staves and rings
L0: 3D single modules, 1188 modules in 396 triplets, 0.5m^2
L1: n-in-p planar quad modules, 1160 modules, 2.0m^2
1.2x10^{16}n$_{eq}$cm^{-2} & 9.5MGy @2000fb^{-1} (layer-0 r=33/34mm)

SYSTEM DESIGN: POWERING SCHEME



- Serial powering of pixel modules with up 12 (16) modules per chain
- DCS functionality integrated in concept
  - DCS chip: monitor and control of module (bypassing)
  - Independent power and communication lines for the DCS

See M. Hamer‘s talk tomorrow for more details

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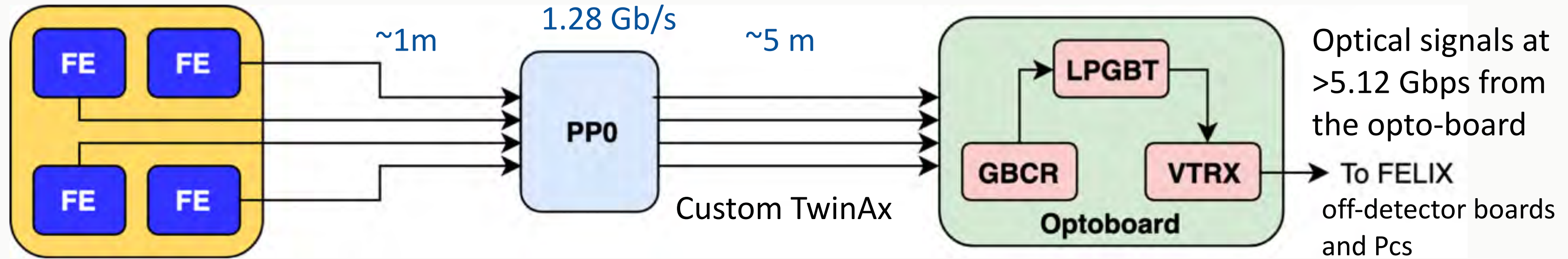
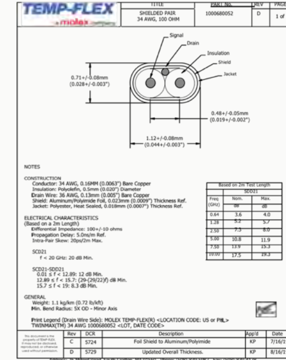
SYSTEM DESIGN: DATA TRANSMISSION



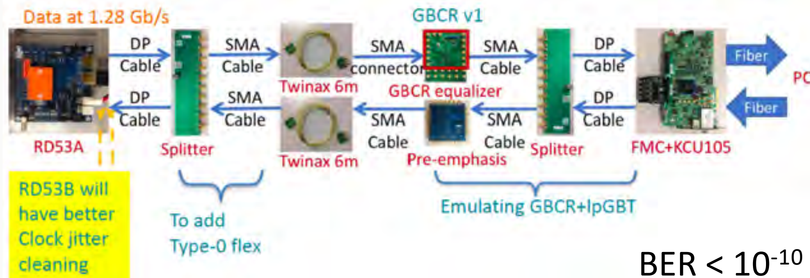
kapton/copper flexes → PP0 → TwinAx cables → Gigabit receiver chip (GBCR) → lpGBT (low-power Gigabit transceiver and VTRx+) for aggregation and electro-optical conversion

- Readout from FE-chip at 1.28 Gbps with up to 4 links per chip depending on position in pixel system
- Uplink sharing on module used on all layers to reduce material
- Sharing of downlinks under discussion: forwarding of CMD between modules
- Custom low-mass 34 AWG twinax cable for transmission from detector to optoboxes, up to 6m
- Losses to be kept below 20 dB from FE-chip to GBCR including connectors, flexes and cable
- Signal recovered at optobox by GBCR
- Aggregation of electrical signals and electro-to-optical conversion by lpGBTx and VTRx
- Optical fibres to readout PCs with FELIX boards

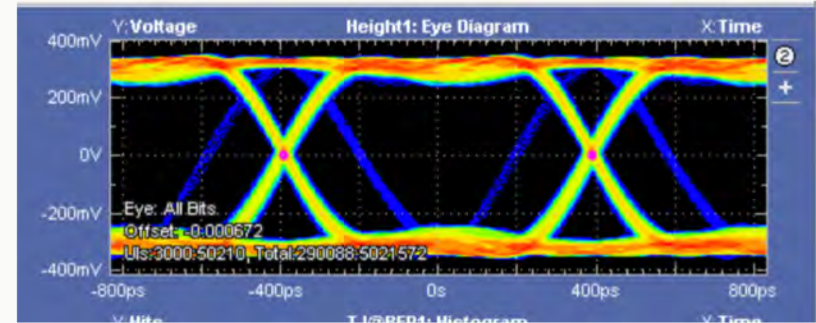
DATA TRANSMISSION



- **Candidate twinax cable identified**
  - Termination being developed
- **GBCR v2 submitted end of 11/2019, optimised for 1.28Gbps**
  - Include CMD pre-emphasis
- **Improved jitter in RD53B/ITkPixV1**
  - Data transmission tests with RD53 CDR test chip
- **Developing System tests with all elements**



BER < 10^{-10}

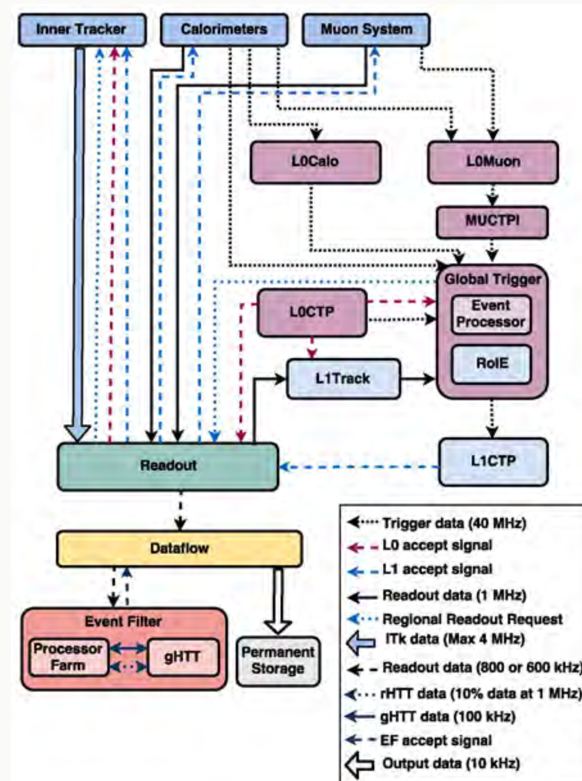


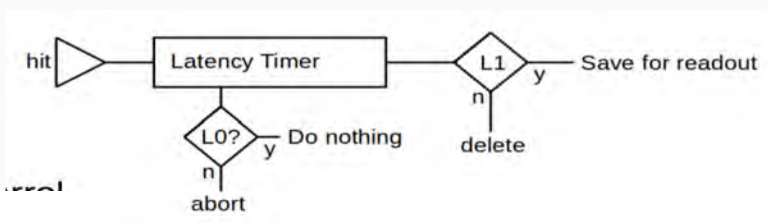
- Eye diagram over full chain:
  - RD53 CDR + Flex + TwinAx + GBCR with pre-emphasis
  - Jitter: ~50 ps, Eye opening: 250 mV

SYSTEM DESIGN: READOUT & TRIGGER CONCEPT

- Complete ITk readout on L0 with 1 MHz rate and 10 µs latency <u>or</u>
- Partial ITk readout on L0 with 4 MHz/10 µs and full readout at L1 with 600 or 800 kHz/35 µs
  - outer pixel layers can provide full data on L0
  - inner layers can't due to bandwidth limitation of 5 Gb/s

    → fast clear on L0, wait for L1

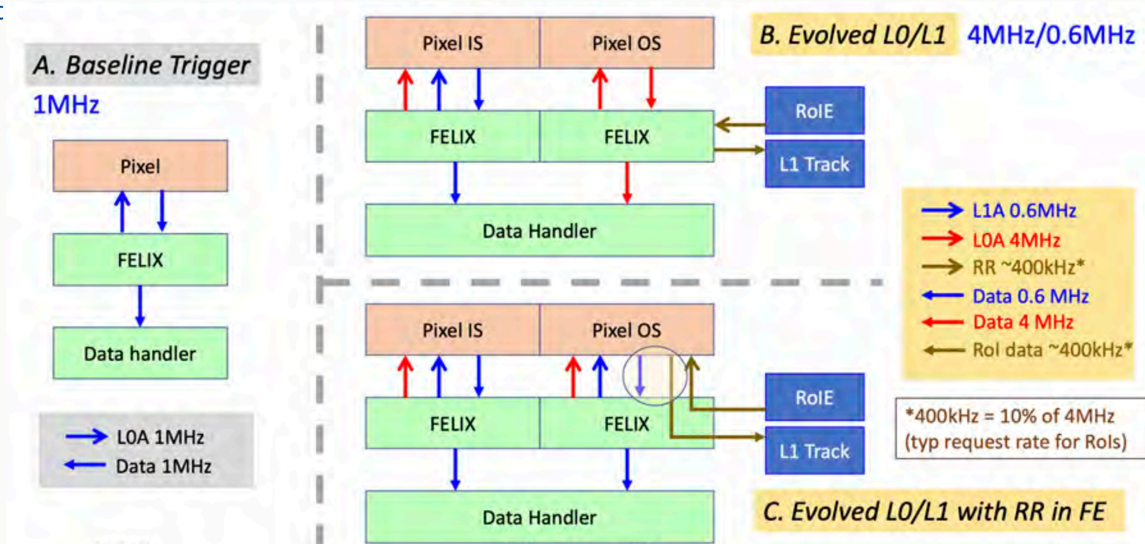




READOUT SCENARIOS: EVOLVED L0/L1 WITH OR W/O REGIONAL READOUT IN PIXEL

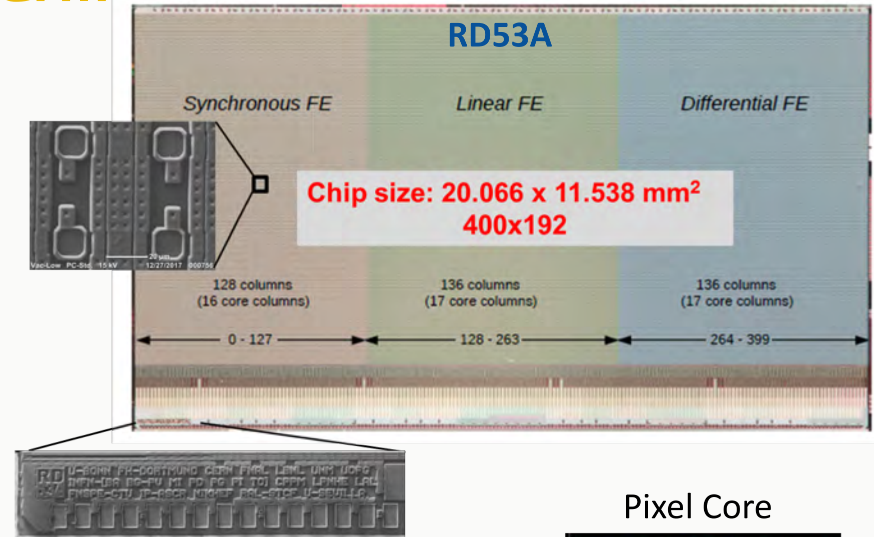
- Electrical readout until optoboards requires many services inside the detector volume and drives the material budget
  - new material budget and introduction of safety factor significantly increased data rates
  - estimates for link occupancy limits significantly decreased for hardware track trigger (HTT) requested regions
- **It seems impossible to fit more services into the available services gaps**
  - risk for baseline trigger scenario seems acceptable
  - standard evolved trigger scenario seems ruled out

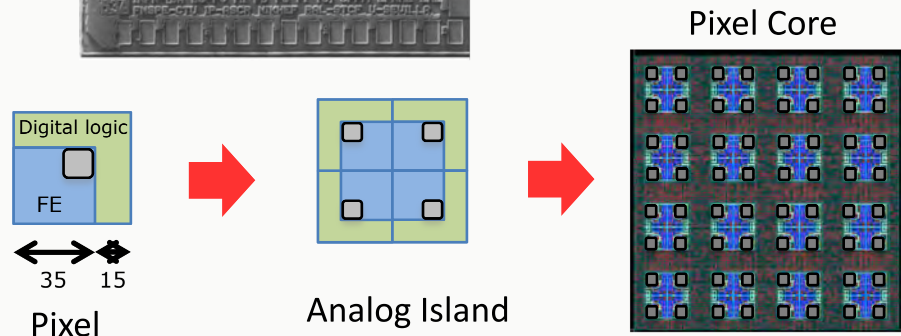
  → **Explore evolved trigger scenario with regional readout in Pixel FE**
- Some handles to recover rate capabilities
  - higher thresholds
  - ToT suppression
  - latency budget (fine-tuning on TDAQ side)



PIXEL READOUT CHIP

- Format & power similar to FE-I4
- CMOS node and vendor: 65 nm TSMC
- Joint development ATLAS & CMS
  - RD53 – share resources
  - Several prototypes fabricated and tested
- Radiation tolerance challenge → talk M. Menouni yesterday
  - Damage mechanism empirically characterized
  - Produce design spec for 500 MRad (1 GRad) target
- Pixel layout
  - 50x50 μm^2 with 4-pixel analogue section in 3 flavours for RD53A
  - Surrounded by synthesized digital sea, organised in 8x8 Pixel Cores
  - 50 μm minimum pitch to allow "standard" flip-chip
- Timescale
  - Aug. 31, 2017: RD53A Submission
  - Dec. 6, 2017: First chip test
  - Apr. 13, 2018: First bump-bonded chip test
  - Mar. 17, 2020: ITkPixV1 Submission





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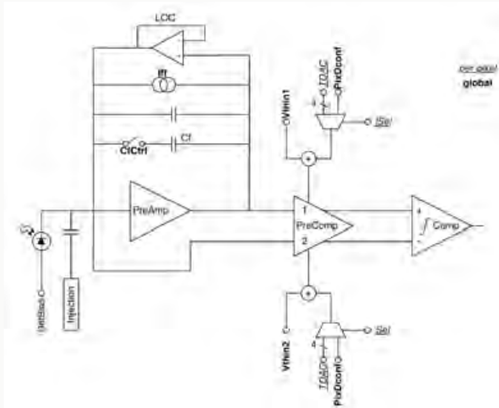
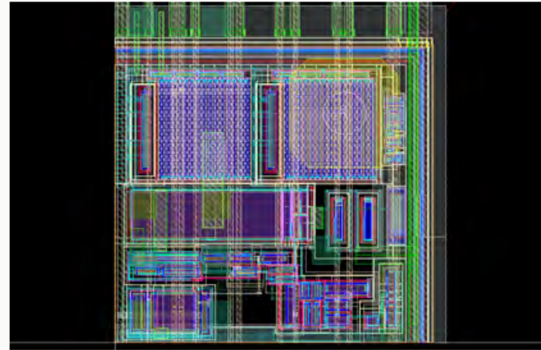
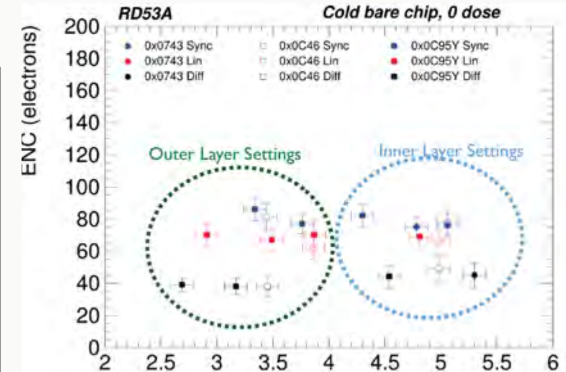
PIXEL READOUT CHIP SPECIFICATIONS

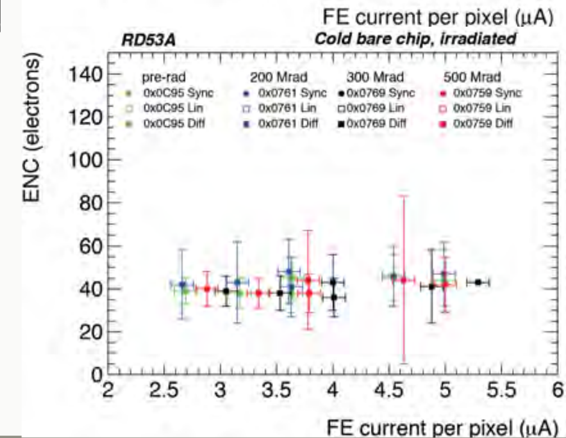
Technology	65nm CMOS
Pixel size	**50x50 um^2**
Pixels	394x400 = 157600
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	**<1200e-**
Noise hits	< 10^{-6}
Hit rate	**< 3GHz/cm^2** (75 kHz avg. pixel hit rate)
Trigger rate	**1 or 4 MHz**
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	**1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s**
Radiation tolerance	**500Mrad at -15°C**
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	**0.7 W/cm^2 including SLDO losses**
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

PIXEL READOUT CHIP: DIFFERENTIAL ANALOG FE









- ATLAS choose the differential FE for ITkPixV1
  - Continuous reset integrator first stage with DC-coupled pre-comparator stage
  - Two-stage open loop, fully differential input comparator
  - Leakage current compensation a la FEI4
  - Threshold adjusting with global 8bit DAC and two per pixel 4bit DACs
- Combines **excellent noise occupancy performance** and **low power**

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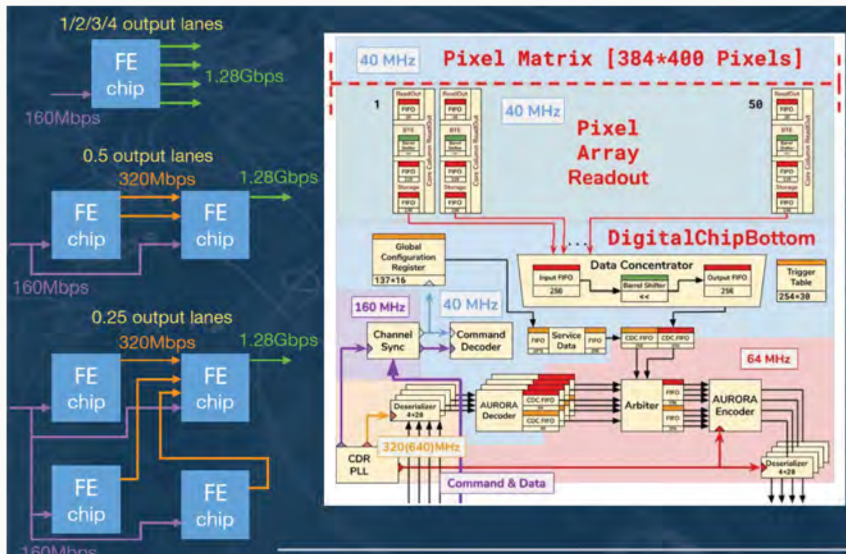
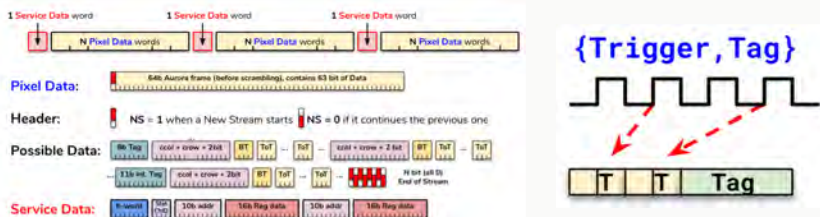
ATLAS ITk

PIXEL READOUT CHIP: DIGITAL ARCHITECTURE & I/O





{Trigger,Tag}

T T Tag

CMD Protocol:

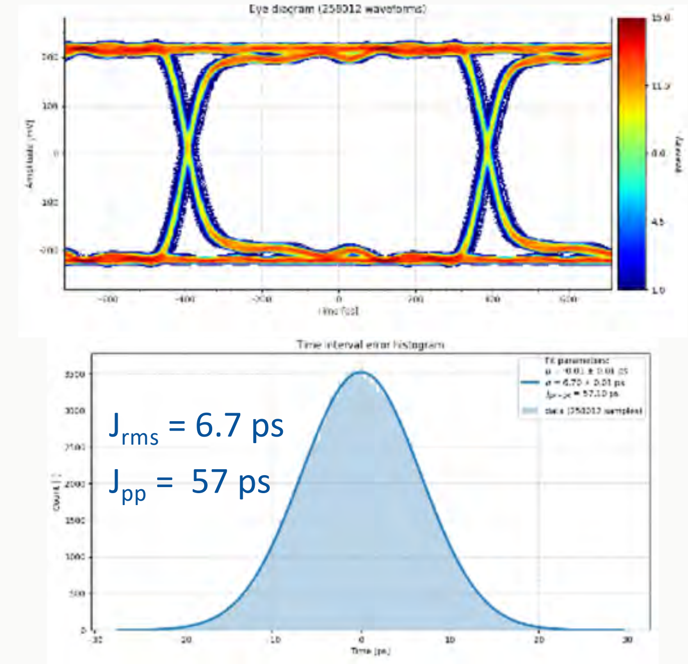
- 16-bit frame based format
  - Custom DC balance encoding
- Enables trickle configuration (writing config during data taking)
  - Important to SEE mitigation strategy
- Two trigger schemes
  - Single level (L0) or Two Level (L0/L1) with L0 = save, L1 = read
- Trigger tagging
  - Self correcting scheme in case of BC counter upset

Output Protocol:

- Aurora protocol (64b/66b encoding)
- Streams to carry multiple events (max number programmable)
- Highly compressed event format within stream
  - Varying length
  - Binary tree encoded hit maps
- Overall achieved around 25% data compression compared to RD53A
- Comes at cost of complexity in DAQ

PIXEL READOUT CHIP: LIST OF CHANGES AND NEW FEATURES

- Improved CDR/PLL design:
    - After X-ray irradiation to **600 Mrad**(-14 °C) **circuit is fully functional**, peak-peak jitter increased by only 13%
    - Better SEE susceptibility
- Improved ShuntLDO design:
    - New bandgap scheme and start-up
    - Overload/undershunt and overvoltage protection
    - Low/High power mode configuration and V_{ofs} averaging option
- Hit processing and latency buffering in pixel/regions/cores
- Triggering and data flow:
    - Support for 1 or 2 level trigger schemes
    - Extended data buffering and handling of buffer overflows
    - Optional removal of isolated hits and limiting of number of hits per core column
- Additional readout features:
    - Binary tree hit encoding and optional ToT information discarding
    - Programmable use of Aurora streams and flexible data merging on multi-chip modules
- Calibration and test features
    - Configurable Auto-trigger and High precision ToT
    - DFT scan path for effective production testing
- SEU and SET protection



Eye diagram and TIE histogram of 1.28 GB/s PRSB15 pattern with 160 MB/s input

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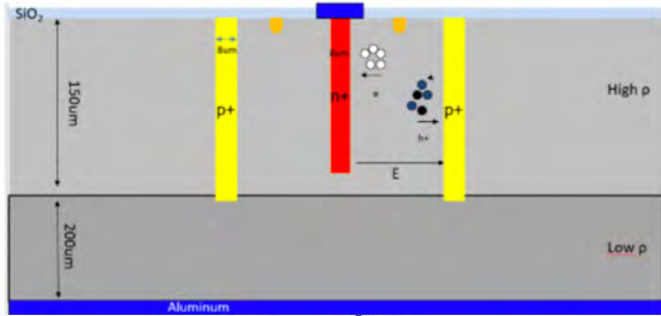
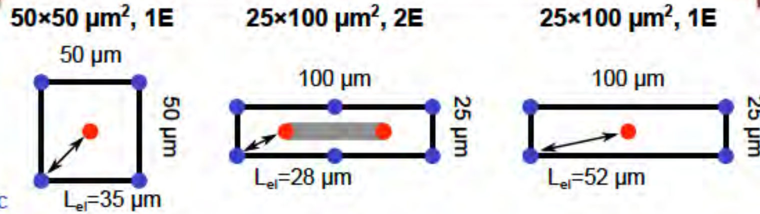
3D SENSORS



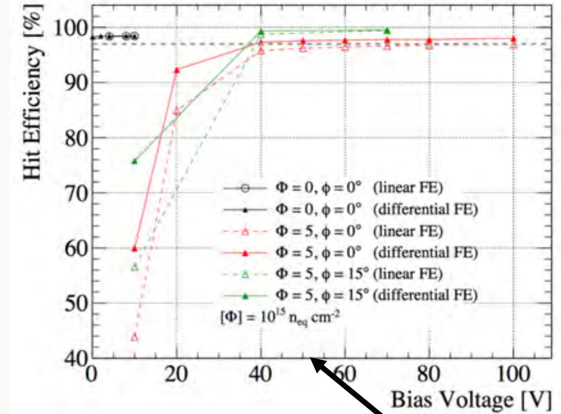


150µm active thickness + 100µm support wafer
25x100 1E for L0 barrel and 50x50 1E for L0 rings

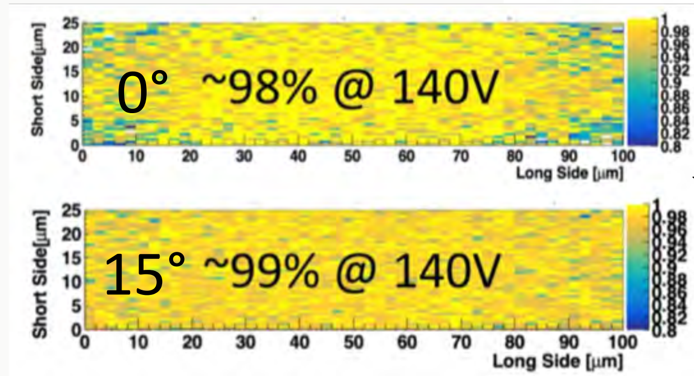
3D sensors are used only in L0
Requirements:

- Radiation hard to $10^{16} n_{eq} cm^{2}$
  Operating voltage < 250V
- Power < $10 mWcm^{-2}$
- > 97% hit efficiency

3D market survey complete



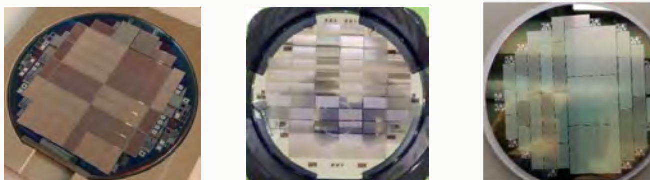
150 µm+ RD53A chip at $5x10^{15} n_{eq} cm^{-2}$



150 µm+ RD53A chip at $10^{16} n_{eq} cm^{-2}$

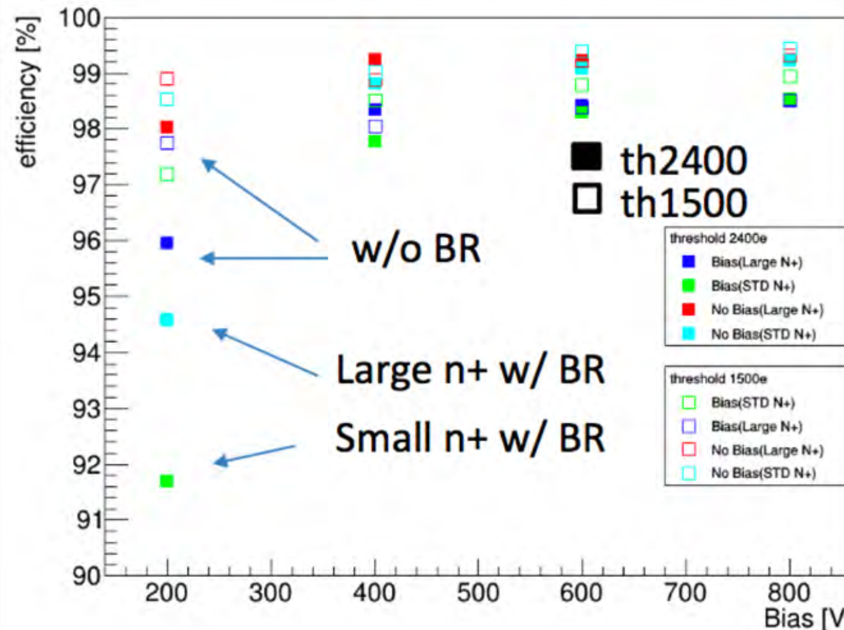
PLANAR SENSORS

- Radiation hard to $3.1 \times 10^{15} n_{eq} cm^{-2}$
- Dies of 4x4 cm2 (quads), 100µm in layer 1 and 150µm thick in layers 2,3,4
- Require:
  - Bias voltage up to 600 V (at end of life)
  - Hit efficiency > 97% (at end of life)
- Optimization ongoing for:
  - Biasing structure kept floating to reduce efficiency loss
- Market survey underway, will complete in 2020



Optimisation of biasing structures: No-bias structure and bias rail (punch-through also being used)

Test beam result for 50x50 µm² RD53A module irradiated with 70 MeV protons to $3 \times 10^{15}\, n_{eq} cm^{-2}$
> 98% efficiency for 600V

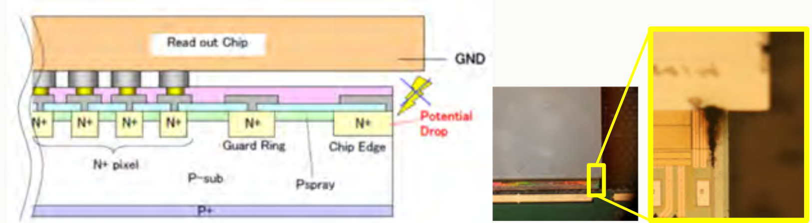


MODULES

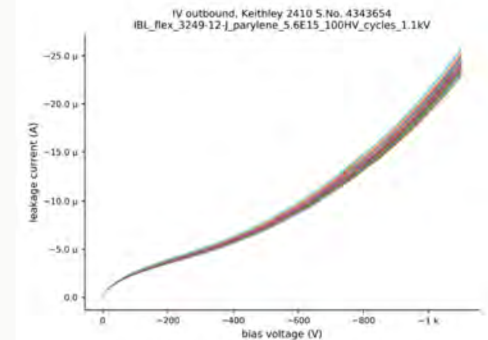
- **Hybridisation**
  - Market survey in progress
- **Wire bond encapsulation**
  - Protect against handling and corrosion
  - No candidate for full encapsulation identified after irradiation due to CTE mismatch and material becoming harder and more brittle
  - Partial encapsulation or low CTE material being investigated
- **Module assembly**
  - Using stencil method
  - Module carrier for transport and testing
- **Around 200 RD53 modules in production**
  - Exercise full production chain

Module Carrier

HV Isolation



Parylene-N used, no discharge observed on 33 irradiated modules up to 900V



Promising results after irradiation, no discharge observed 100 cycles -55 to +60 and 400 cycles to 1kV + 200 cycles to 1.1kV after 7.4 MGy
Wire bond strength retained after irradiation to 5.2 MGy

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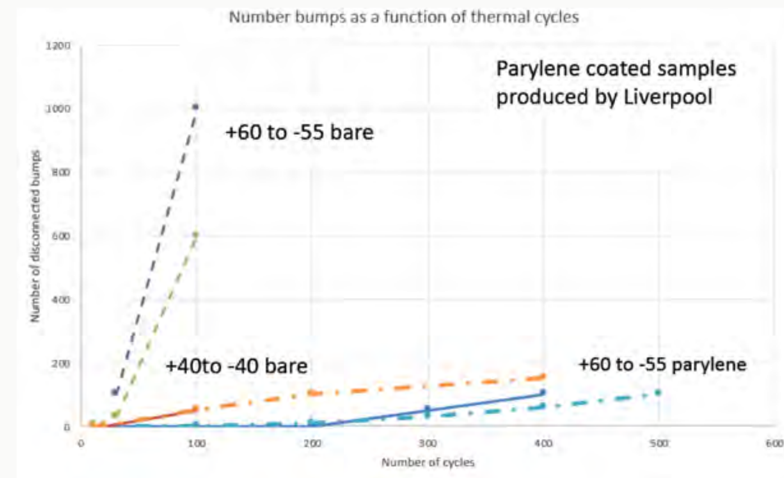
MODULES – BUMP STRESS

- **Failure of bumps observed on FE-I4 modules during thermal cycling (-55, 60)**
  - FEA models have been used to analyse thermal stresses in modules
  - Linear models and models with correct bump geometries have been studied
  - Models predict number of cycles to failure similar to observed with FEI4 single-chip modules
  - CTE mismatch with Cu in hybrid has biggest effect – optimize Cu in hybrid
  - ITkPix modules using 25µm thick copper are predicted to survive 200 thermal cycles for -55 → +60°C
  - Models predict 4000 cycles before failure for +40 → -45°C compared to spec of 400
- **Thermal cycling of single-chip modules and quads**
  - Initial bump quality is important
  - Reasonable agreement with FEA models
  - Parylene coating has a beneficial effect
- **Considerable progress in understanding the problem and engineering a solution**



Thermal cycles on single chip FEI4 modules with 48µm Cu on hybrid, with and without parylene

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CONCLUSIONS

ATLAS ITk

- Building a pixel detector for operation at the HL-LHC is challenging
  - Extreme rates and radiation hardness
  - Increased granularity
  - Low mass
- ITk pixel system has been designed to meet these challenges
  - Smaller pixels with new faster electronics
  - Low mass materials and modules
  - Serial powering
- The project is now moving from design to prototyping
- Many challenges remain
  - Large scale production
  - Learning about system effects
  - Dealing with effects of Covid-19 pandemic