The Phase 2 upgrade of CMS Inner Tracker

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CERN

Outline

CMS Inner Tracker for HL-LHC

Requirements, Layout & Performance

System aspects

System Architecture

Development of system components

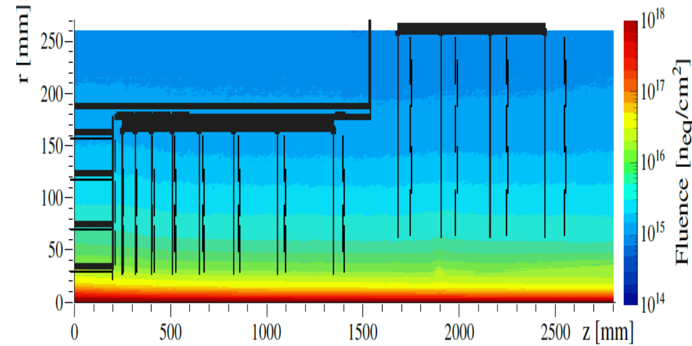
System Tests

Inner tracker Phase 2 requirements

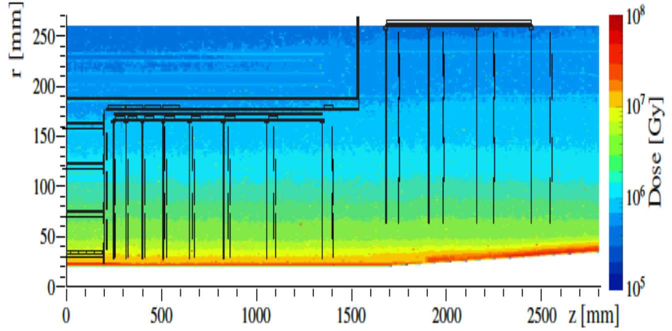
Objective:

Maintain or improve tracking capability with 200PU

8 × higher pile-up	(25 ⟶ 200 PU)
8 × higher hit rate	(⟶ 3.2 GHz/cm^2)
4 × longer latency	(3.2 ⟶12.8 µs)
	⟶ need **8** × **4 = 32** × **bigger buffers**
7.5x higher trigger rate	(100 ⟶ 750 kHz)
	⟶ need **8** × **7.5 = 60** × **bandwidth**
10x more radiation	(300 ⟶ 3000 fb^{-1})



Innermost layer: 2.3x10^{16} n_{eq}/cm^2
Outer & Service cylinder: 10^{15} n_{eq}/cm^2



Innermost layer: 1.2 Grad
Outer & Service cylinder: 100Mrad

Increased granularity (x6 smaller pixels)

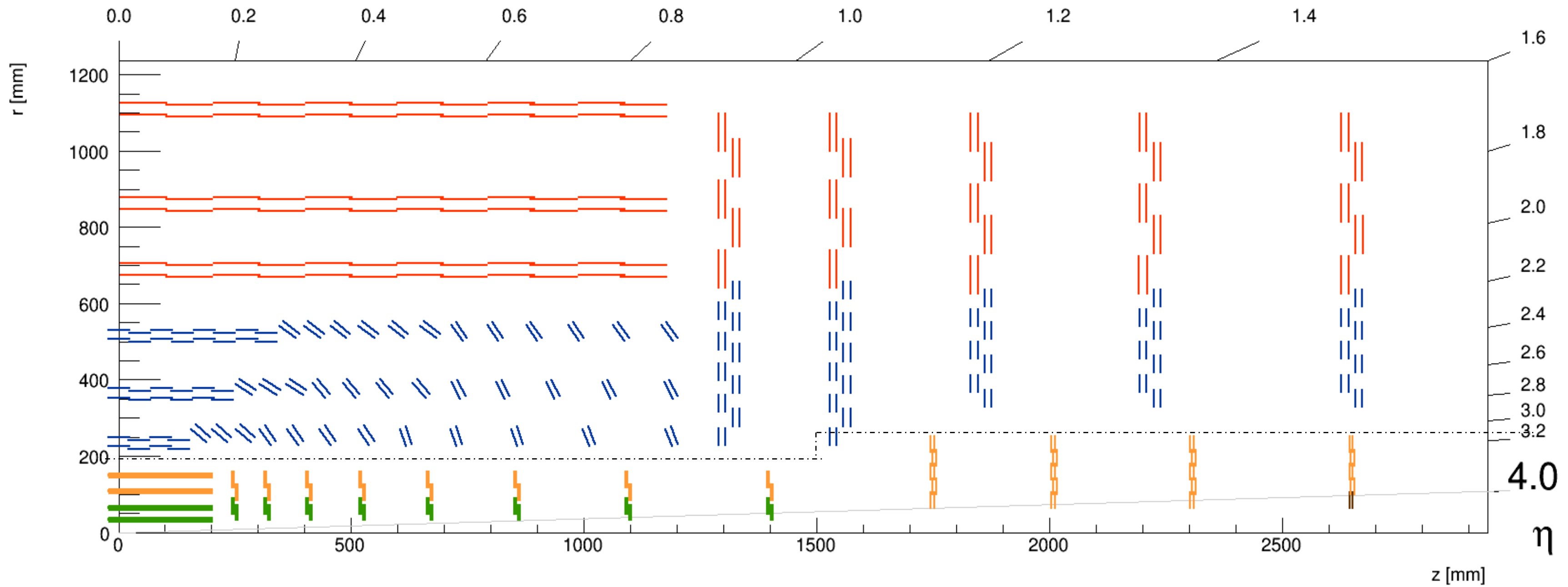
Increased detection coverage (|η|≤ 4)

Reduced material budget (light mechanics, services)

Lower detection threshold (new readout chip)

Simple installation and removal

Tracker Phase 2 Upgrade



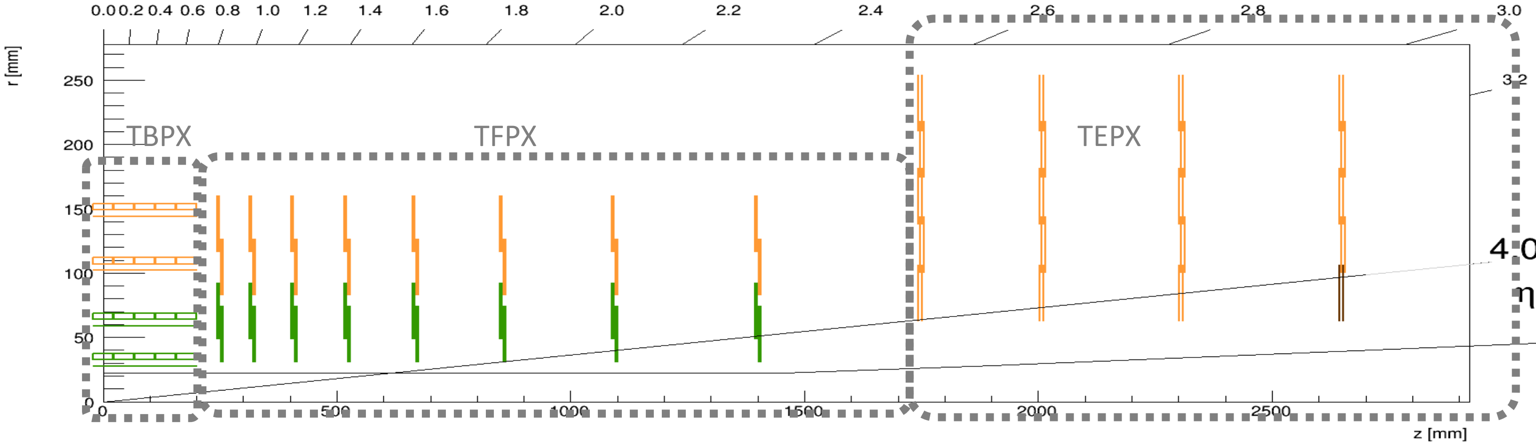
2 types of Outer Tracker:
2S (Strip-Strip sensor modules)
PS (macro-Pixel Strip sensor modules)

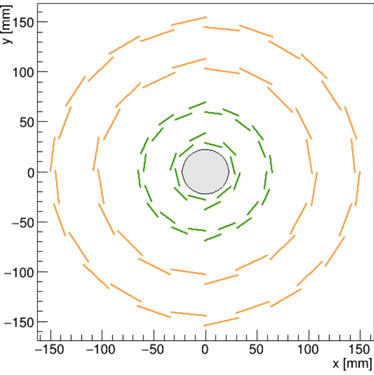
2 types of Inner Tracker modules:
2×2 Pixel Chip modules
2×1 Pixel Chip modules

Inner Tracker Layout: Extension to |η|= 4

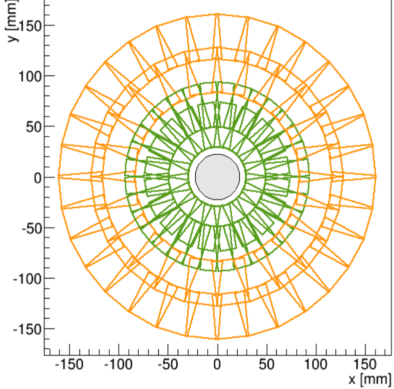
Hybrid technology

Total active surface of ~4.9 m^2 -Optimization for production of 4k modules

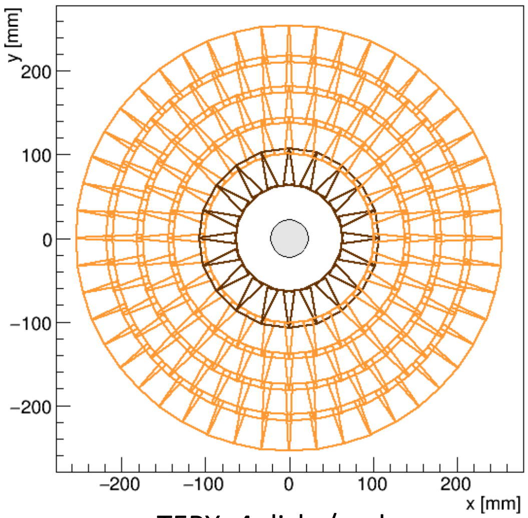




TBPX: 4 layers
4/5 modules per ladder



TFPX: 8 disks/end
4 rings/disk



TEPX: 4 disks/end
5 rings/disk

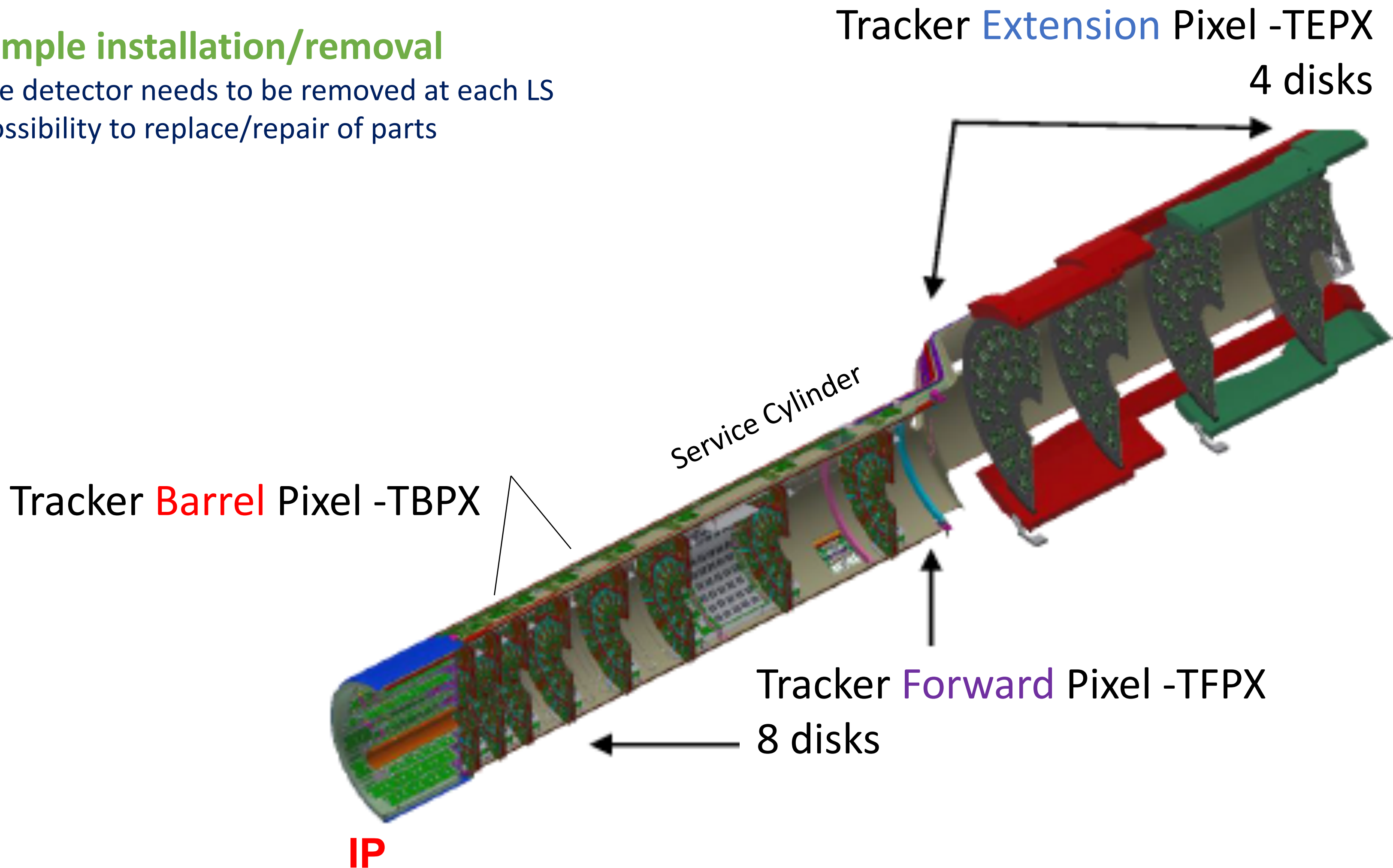
TEPX is a large and powerful luminometer and will receive extra lumi triggers.

First ring of the last disk is fully dedicated to lumi and background monitoring, with independent readout and control.

¼ CMS Inner Tracker

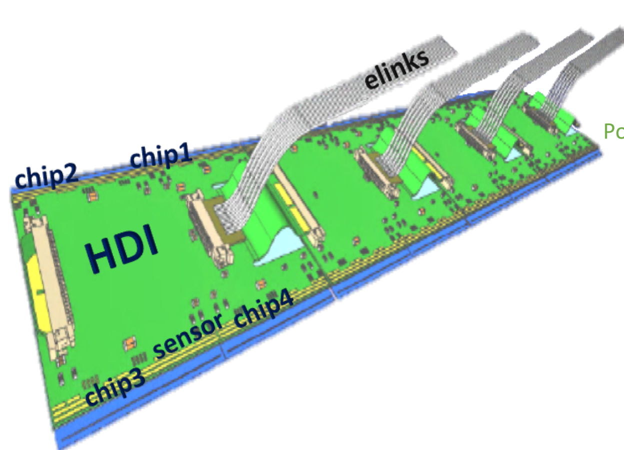
Simple mechanics
no turbines-tilted modules

Simple installation/removal
the detector needs to be removed at each LS
possibility to replace/repair of parts



System Architecture

Pixel modules serially powered



Power pigtail

On-detector

Back-end

LV (CC) / HV PS

HV

LV CC

elinks
Data & commands

LV PS (similar to OT)

LV

DTC

CTRL

TTC

DAQ

VL+

DCDC

LpGBT

VTRx+

PORTCARD

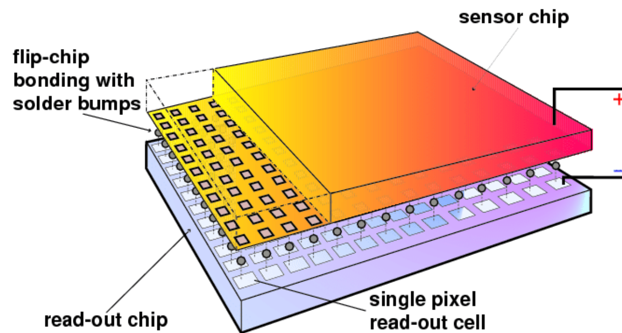
Hybrid pixel modules

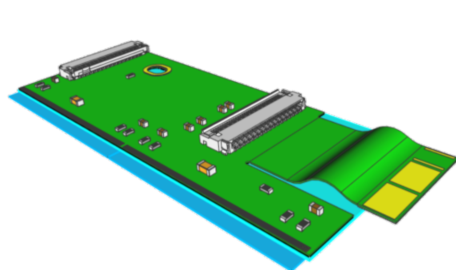
High-Density Interconnect (HDI)

to distribute signals and power to/from module

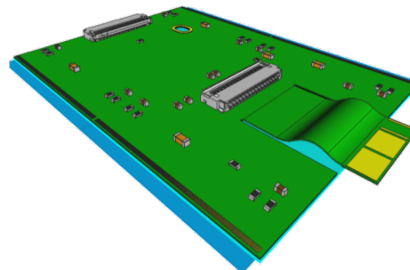
Simple module:

- Pixel chip is the only active component
  - No auxiliary electronics
- Passives: **decoupling caps** and **connectors (power and readout)**
- Wire bonding



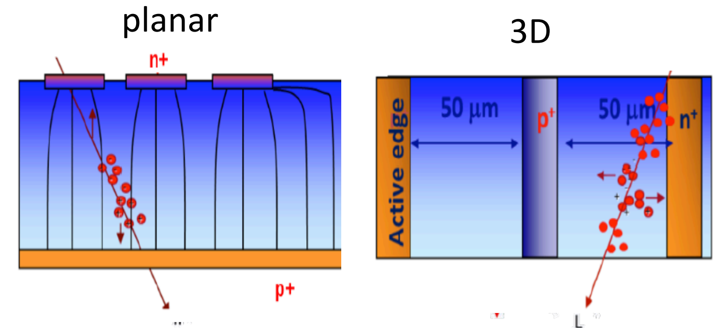


1x2 ROC module

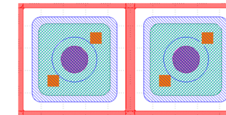


2x2 ROC module

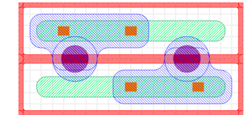
Silicon Sensor



$50 \times 50\ \mu m^2$

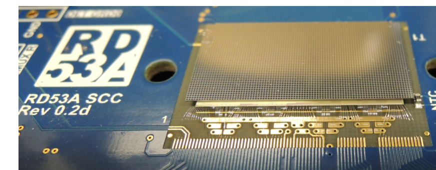


$100 \times 25\ \mu m^2$



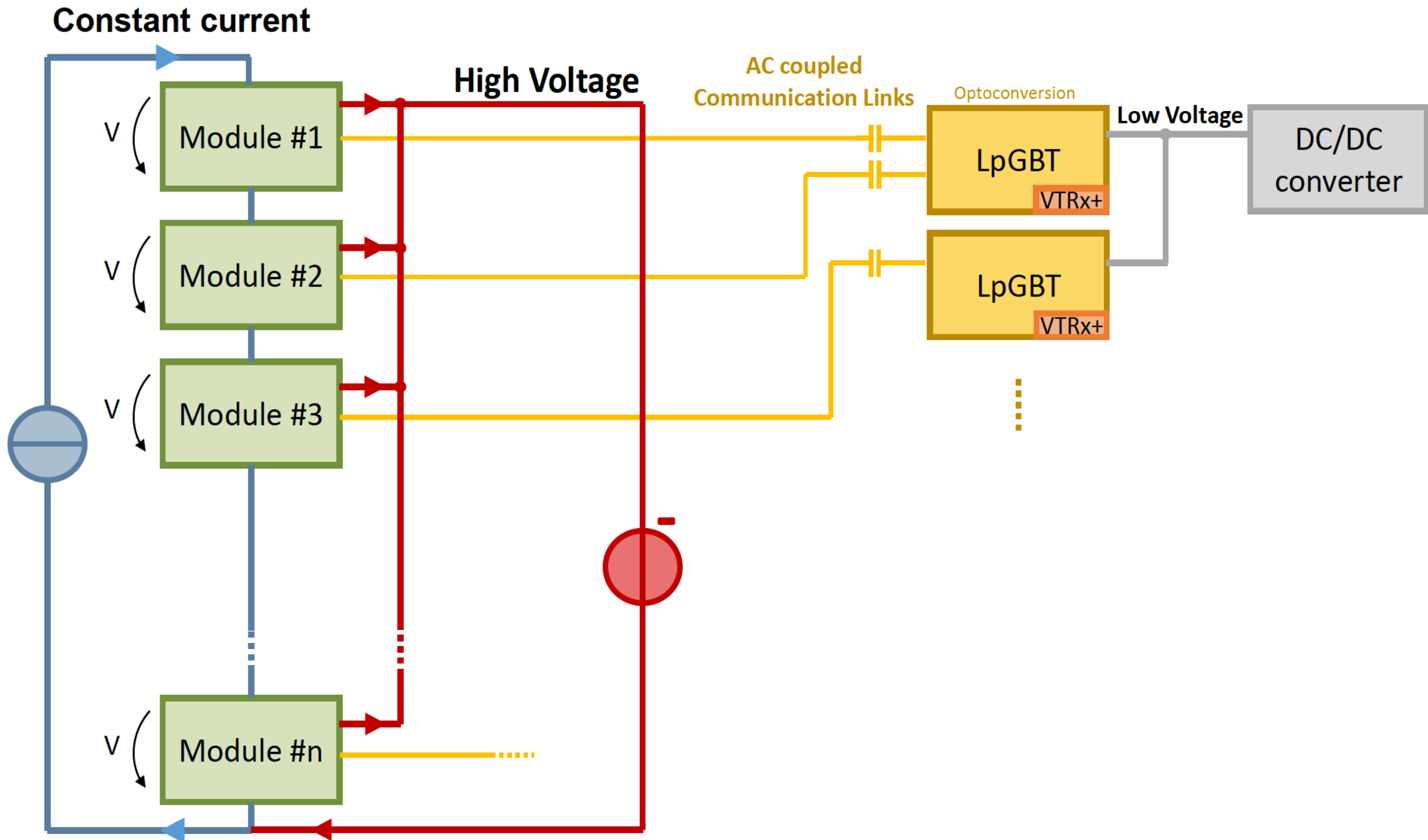
Read out electronics

RD53 chip adapted to CMS requirements
$50 \times 50\ \mu m^2$



System Architecture: Power

Electronics system is segmented in power chains.
No crossing of readout or sensor bias is done among modules of different chains.



Serial Powering across modules

Serial powering is the only viable solution for the IT system ~50 kW on-detector power

✓Low mass- Integrated on-chip - Radiation hard - Not sensitive to voltage drops- Low noise

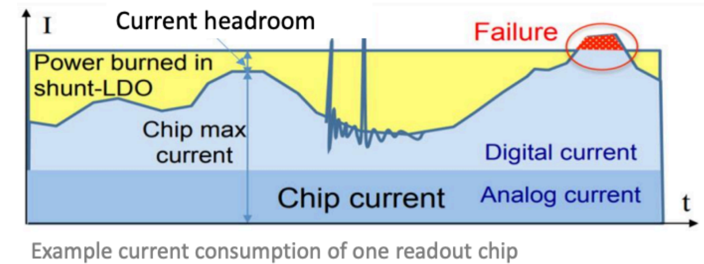
I_{in} constant, enough Iin to satisfy highest I_{load}.
Any extra current gets burnt by shunts.

I_{in} provided by module: Current shared among chips.

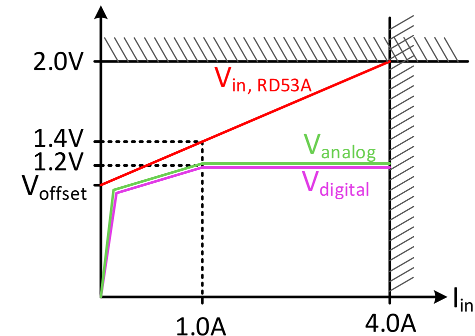
Up to 12 pixel modules serially powered
500 Serial power chains for IT system

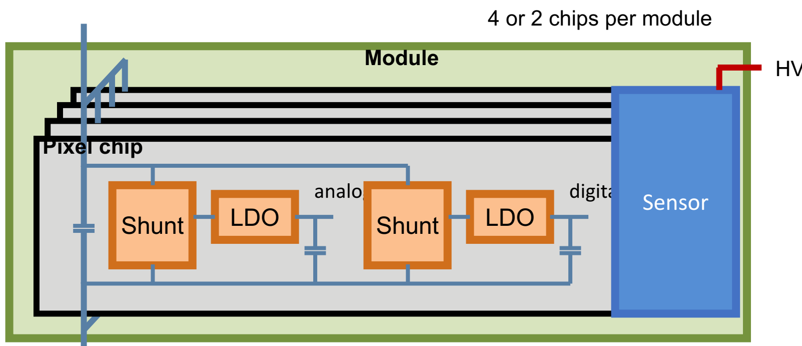
Two on-chip Shunt-LDO regulators for analog and digital supply voltages.
2A maximum input current per Shunt-LDO.

20% current headroom for stable operation in CMS IT



Example current consumption of one readout chip

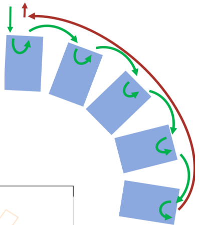


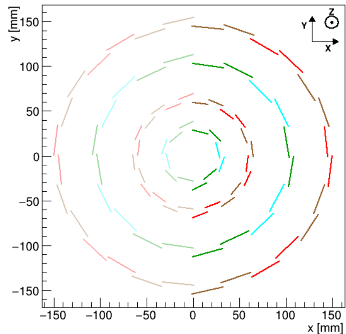


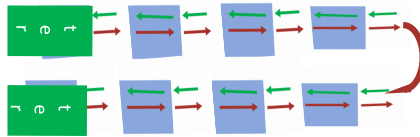
Serial Powering: Max 12 modules/chain

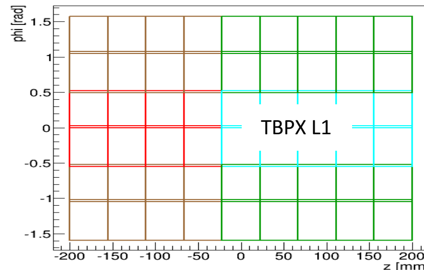
TBPX:
1 chain for 2 consecutive ladders in Phi
8 or 10 modules/chain.

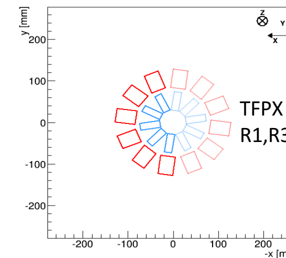
TFPX/TEPX:
1 chain(s) per (X) side /(Z) side of a ring.
5 to 12 modules per chain

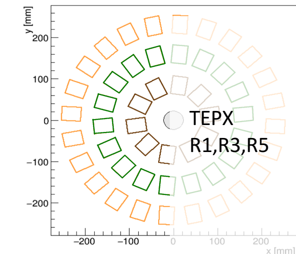


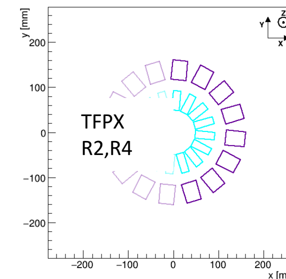


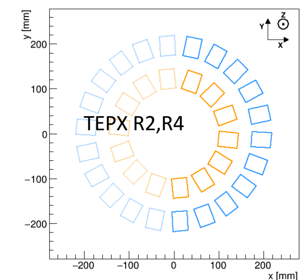






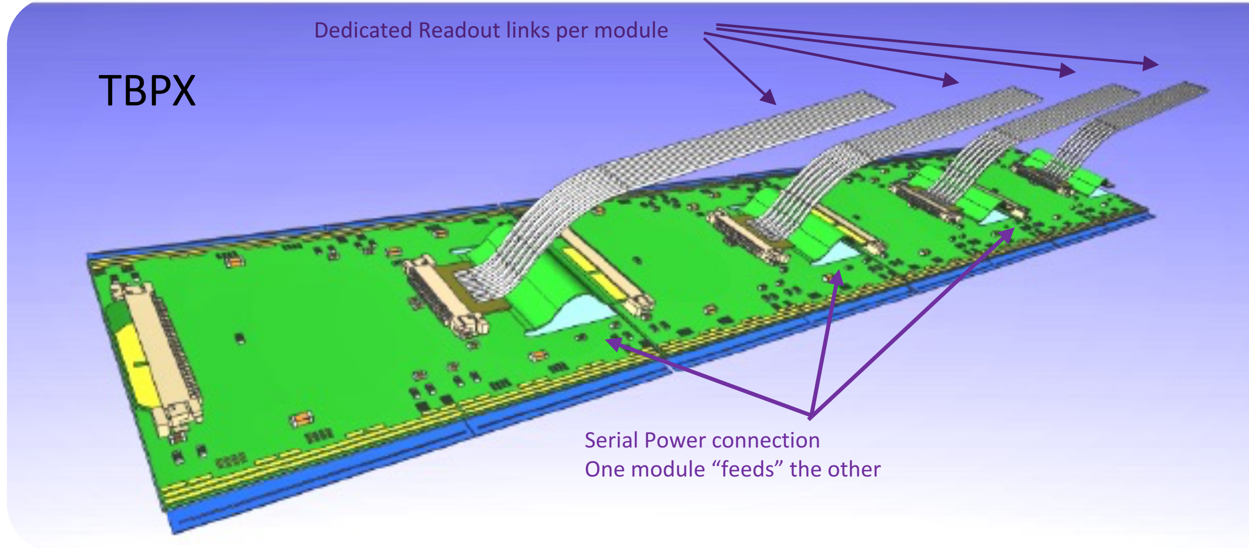


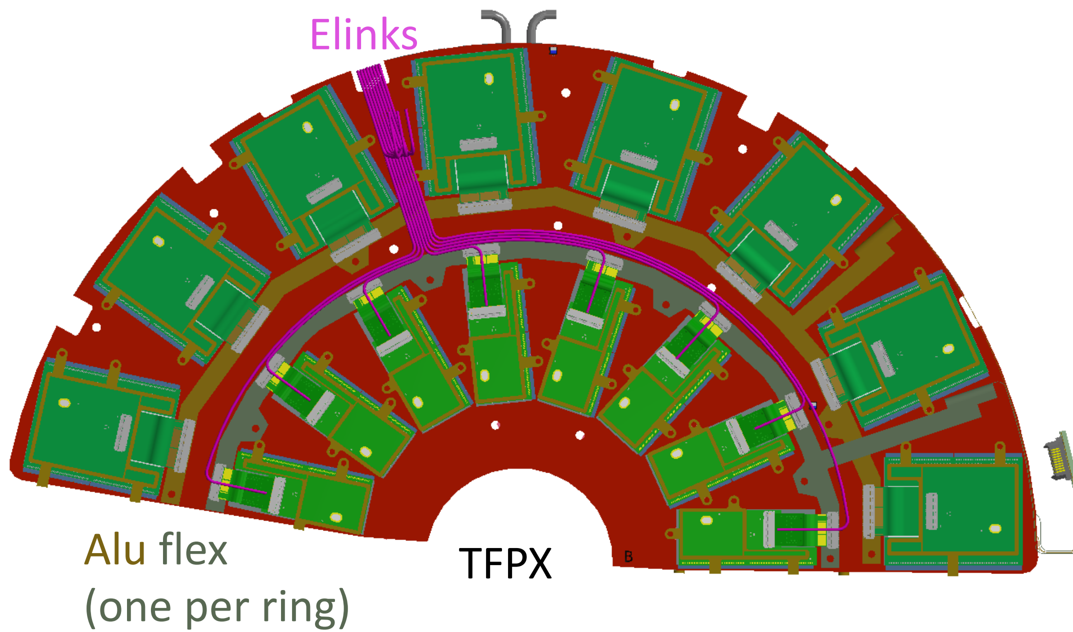


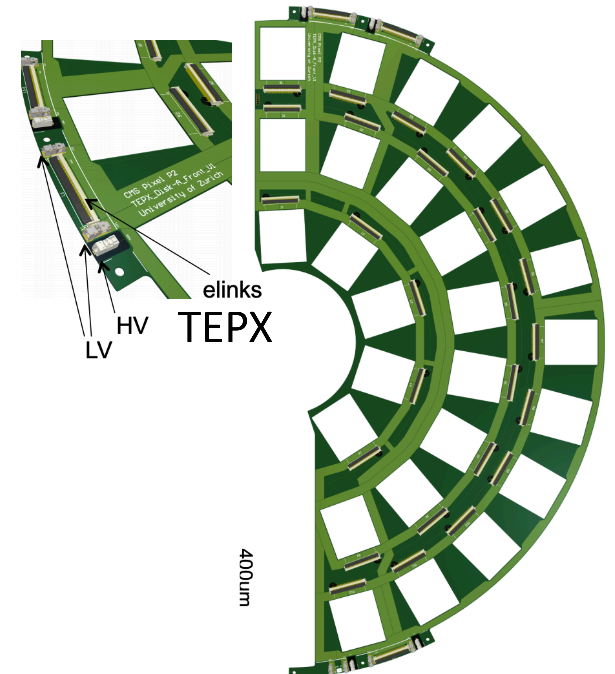


2 HV lines/ SP chain in the barrel, 1 HV line/ SP chain in the rings

Power distribution implementation



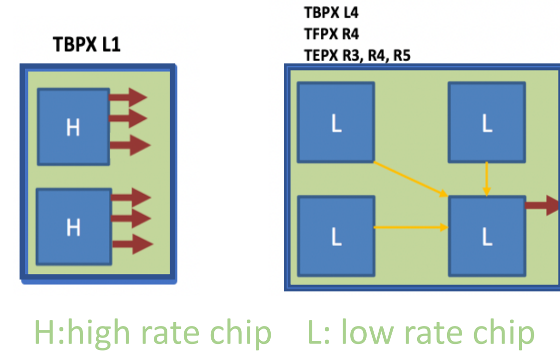




System Architecture: High Bandwidth Readout chain

Up to 6 electrical up-links @1.28 Gb/s per module to LpGBT

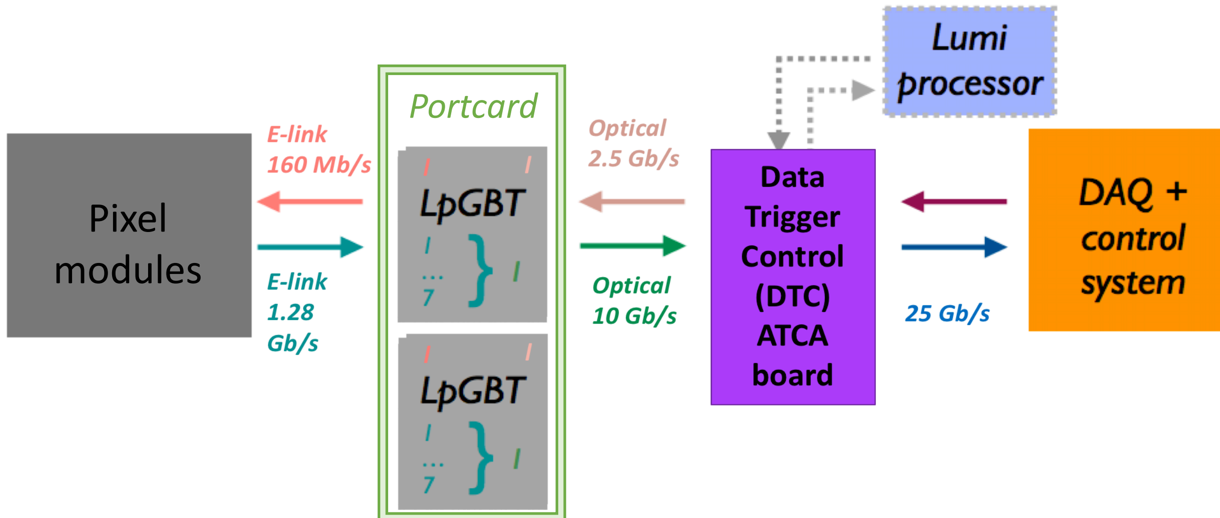
Data from L1 accept, monitoring info to DAQ and control system
Modularity depends on hit rate (location)
Efficient data formatting to reduce data rates (factor ~2)
25% bandwidth headroom on e-link occupancy



H:high rate chip L: low rate chip

One electrical down-link @160 Mb/s per module from LpGBT

Clock, trigger, commands, configuration data to modules



28 DTC (Data, Trigger, Control) boards required for CMS IT

Dedicated boards & crate(s) for TEPX LUMI/BKGD measurement

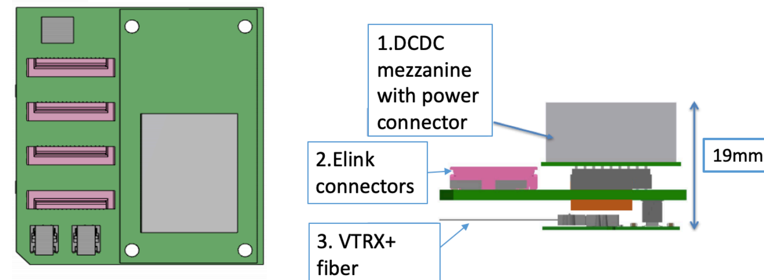
Inner Tracker Service Cylinder Counting Room

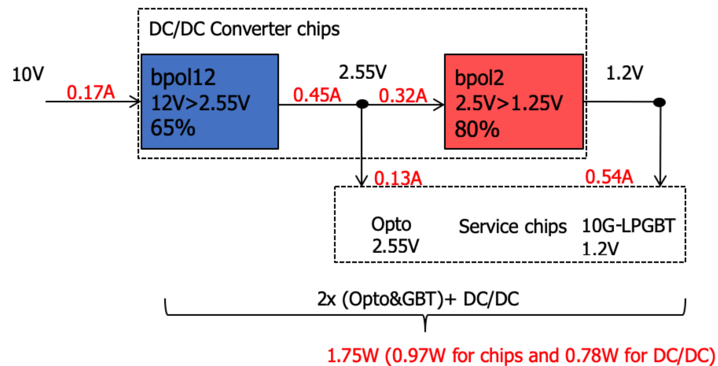
Portcard design

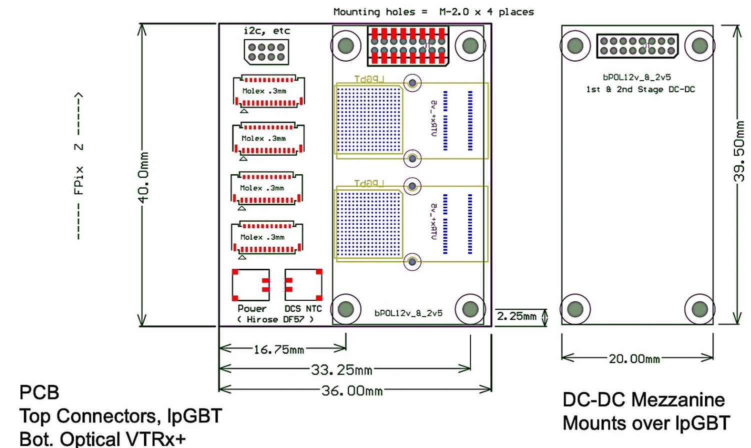
~750 portcards to readout/control CMS IT

Portcard designed in 2019:
4 Kyocera 6841 elink connectors
2 Low-power Gigabit Transceiver (LpGBT)
2 Versatile Link+, each 1 x 10.24 Gbps uplink and 1 x 2.56 Gbps downlink

powered by a mezzanine with a pair of cascaded DC-DC converters (similar to OT powering scheme)

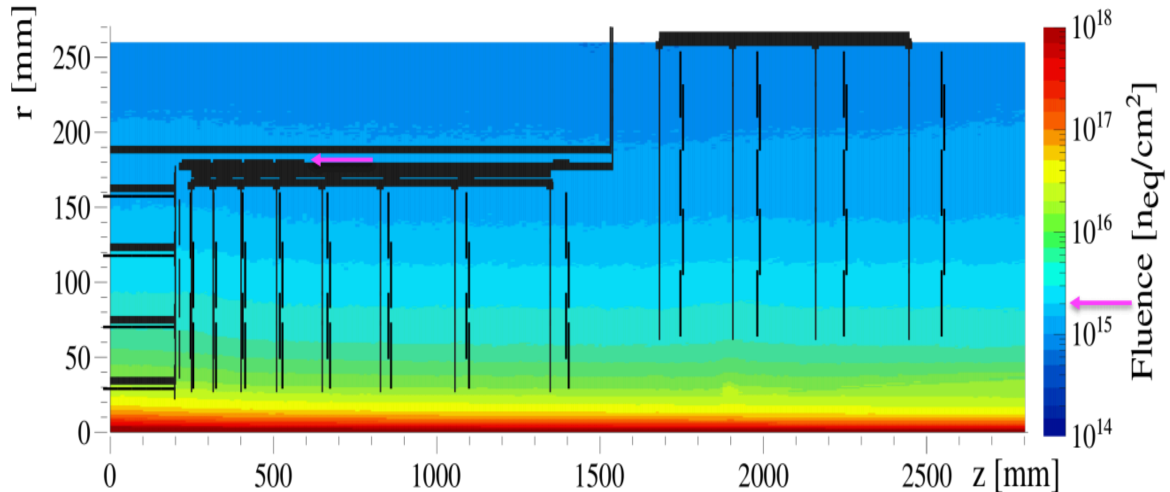




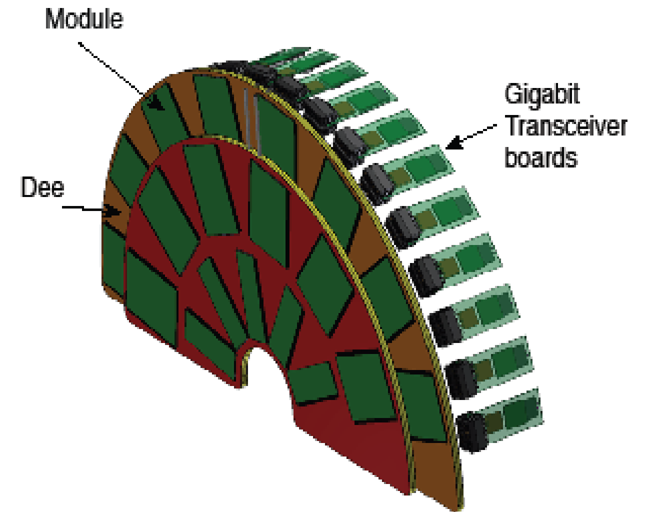


T. Nussbaum, K. Ecklund, A.Kumar Rice University

Portcard integration

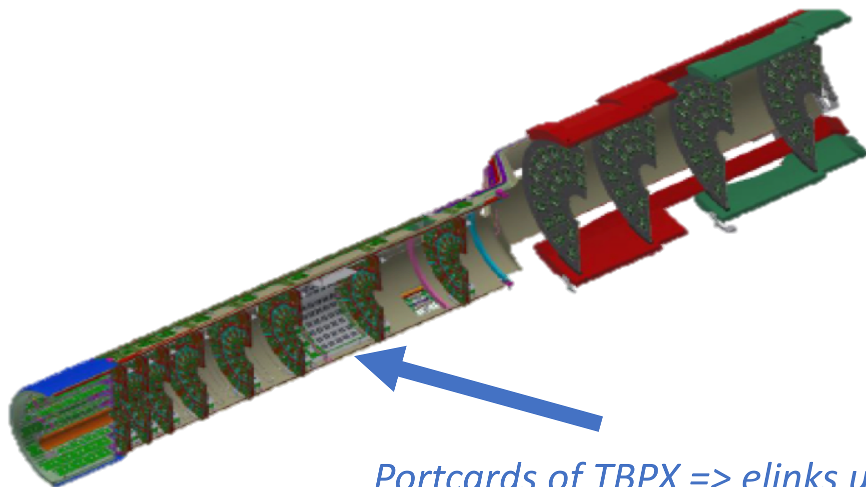


Portcards @outer radii of TFPX Disk



Optoelectronics limits (1E15 n/cm^2 fluence, 100 Mrad) impose their integration at higher radii

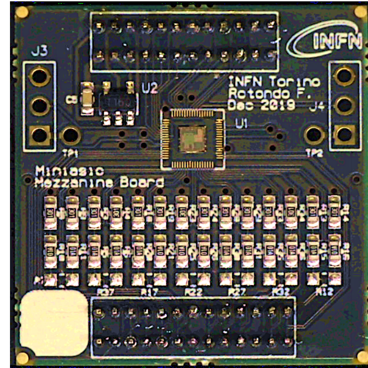
Portcards of TEPX



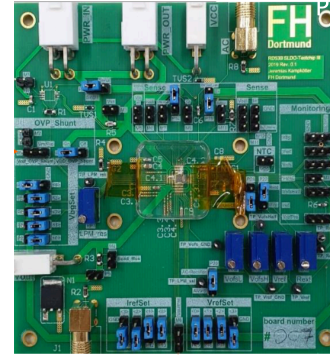
Portcards of TBPX => elinks up to 1.6m

Prototypes Under Test

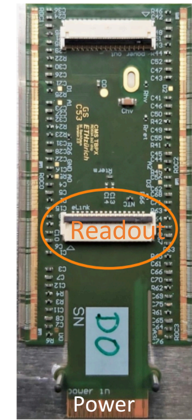
RD53A Single Chip Cards (SCC)

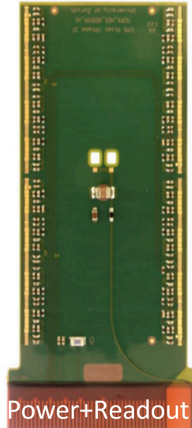


RD53B Linear AFE MiniASIC

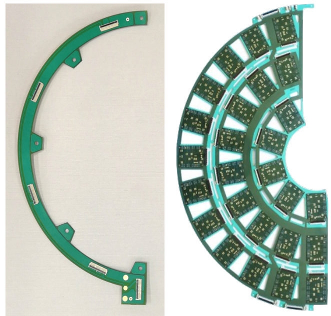


RD53B SLDO test chips

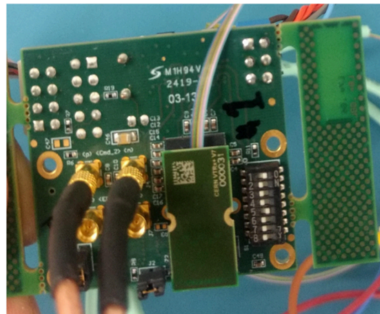




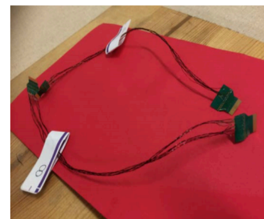
RD53A Quad modules



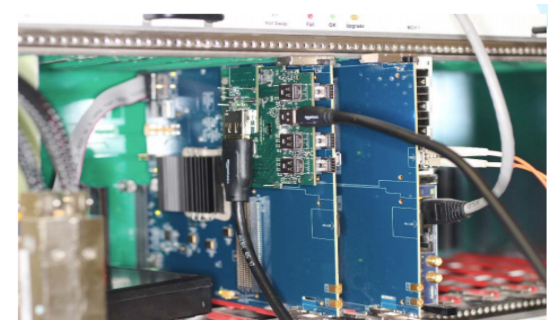
Disk-like setups



Demo Portcard



Electrical links

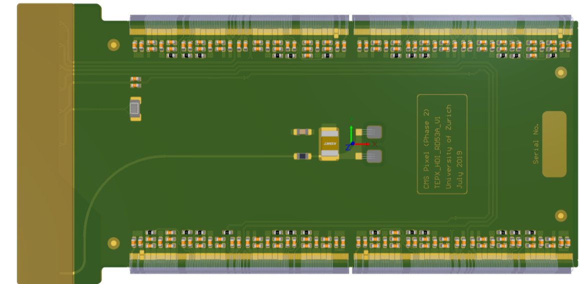


CMS uDTC (FC7) +FMC

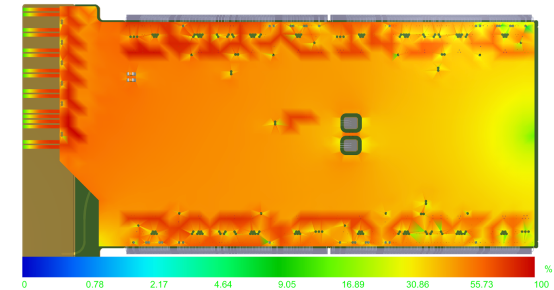
Pixel Module development

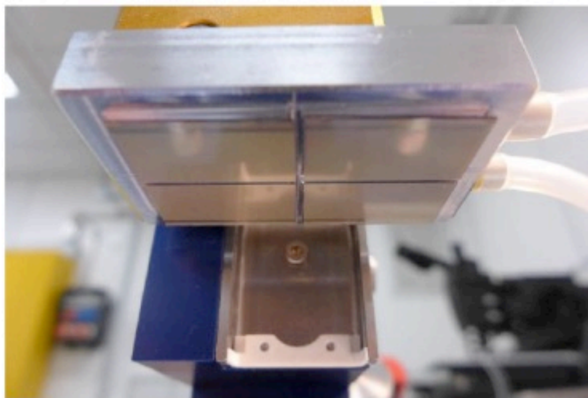
High Density Interconnect (HDI) contains only passive components (routing of signals, power, bias)

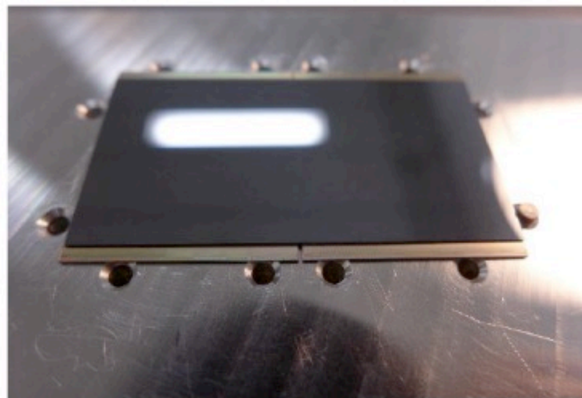
-Designed and tested three RD53A module HDI flavors:
TBPX 2x2, TBPX 1x2, TEPX 2x2
-Development of assembly tools and procedures almost finished
-Assembled and tested to date 25 digital modules in 3 sites and used extensively in system tests
Next:
-Production of demo-modules with sensors (started)
-Design of HDI for CROC-based prototypes (started)

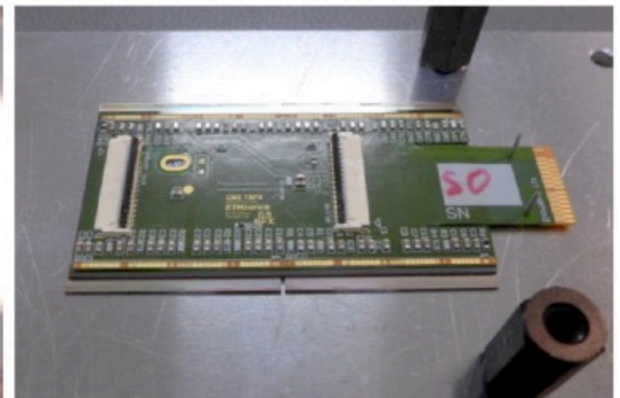


Current density in the middle HDI layer: return line





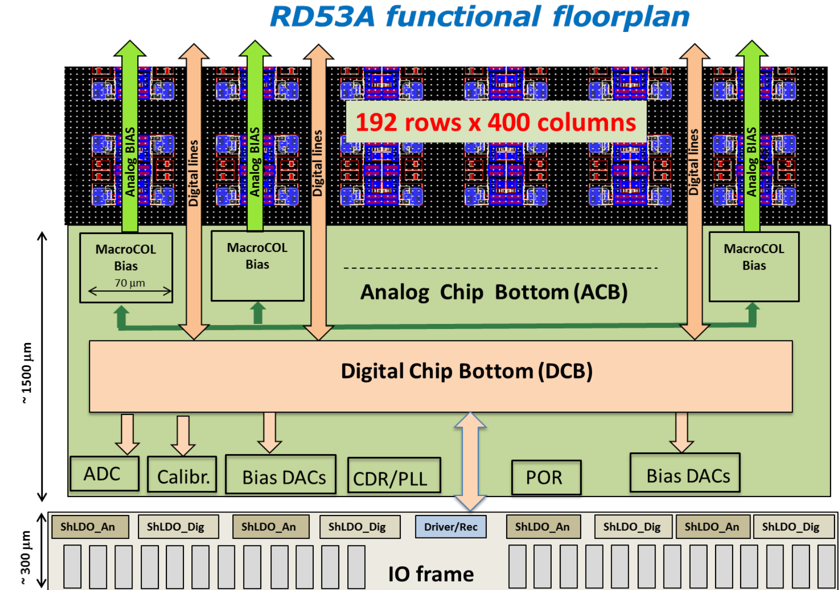


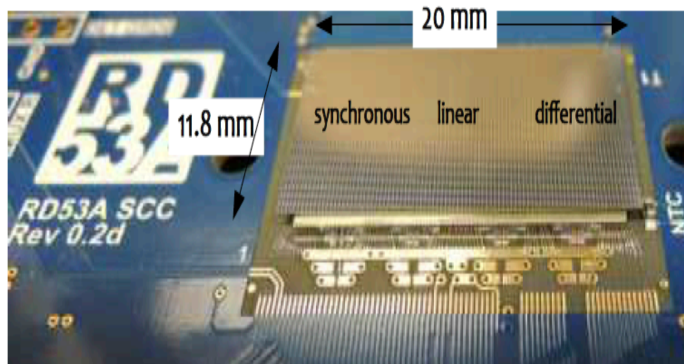


Next generation pixel chip: RD53 chip

RD53A chip (~ ½ size of final chip):
Developed by RD53 collaboration (ATLAS & CMS)
65 nm CMOS technology
Analog islands in a digital sea
50 x 50 μm² pixels
3 Analog Front-End for low threshold operation (<1ke-)
2 digital architectures
Shunt-LDO for serial power
4* **1.28 Gbps** output links
1 * **160 Mbps** control link

RD53A functional floorplan





RD53A Chip is fully functional-RD53A meeting specifications
In May 2019, **the CMS Tracker chose the Linear front-end** for the integration in the RD53B-CMS (CROC)

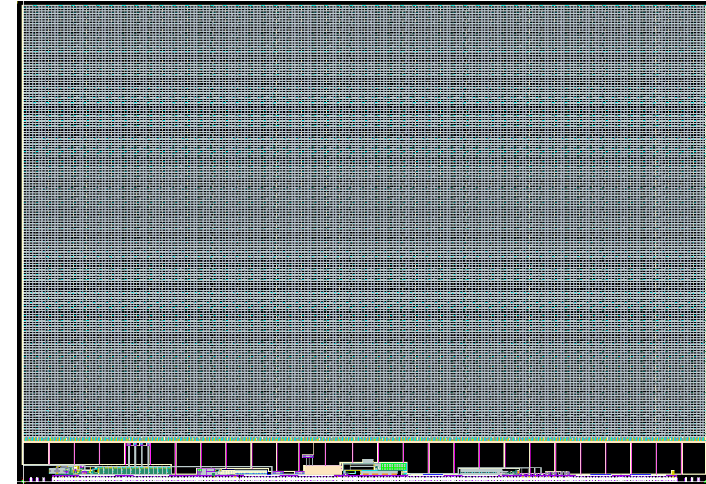
The RD53A version fulfils the CMS requirements with some limitations, like the slow timing response and the Threshold trimming DAC (TDAC) saturation effect at cold, that have been corrected and prototyped in August 2019.

Towards the CROC

Core design of RD53B common for the two experiments
ATLAS chip submitted on March 18 (6 months delay) featuring the ATLAS chosen AFE (Differential) and significanlty improved PLL/CDR and SLDO IPs (tested with miniASICs.)

Integration of the Linear Front-End in the 8x8 Pixel Core → DONE
Adapt the full chip floorplan, top-level netlist and assembly flow to the different array size and Front-End → DONE
Implement and verify few additional features requested to improve the chip calibration, monitoring and diagnostics → Started

Chip verification using data imported from CMSSW ROOT
Full chip assembly and sign-off verifications



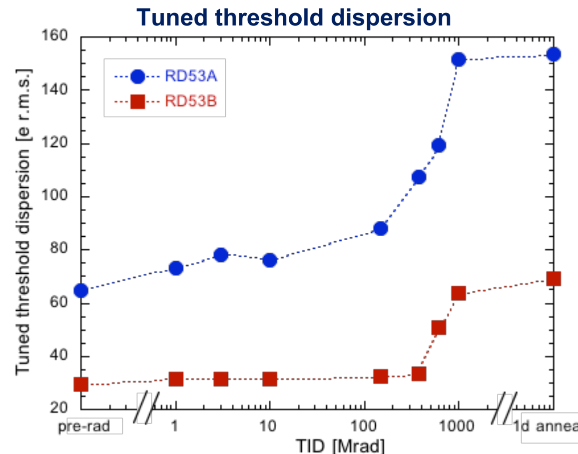
CROC floorplan
Size (including seal-ring): 21.6 mm x 18.6 mm

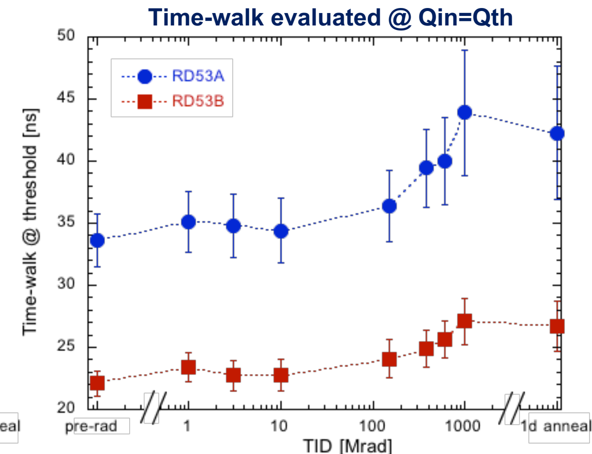
Linear FE test results

CMS Front-End (Linear FE) miniASIC thoroughly qualified

All planned improvements are achieved:
Improved Threshold trimming DAC and 5th bit
Improved Comparator to decrease time walk

Excellent test results vs TID





L. Gaioni, INFN Bergamo/Pavia

F. Loddo, INFN Bari

SLDO test chips: New features for CROC

Campaign in 2019 to evaluate new features on 3 test chips.
Review in Jan '20 to decide on CROC enabled features Tests combined with RD53A confirmed improvements

✓ **Improved startup behavior:**
Common bandgap regulator for Analog/Digital SLDOs

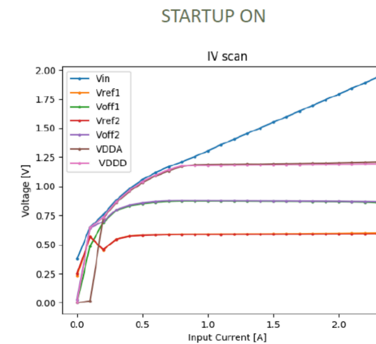
✓ **Overvoltage protection (OVP):**
Voltage clamp to avoid exceeding 2V input

✓ **Vofs averaging mode (configurable):**
To be decided based on system tests with CROC

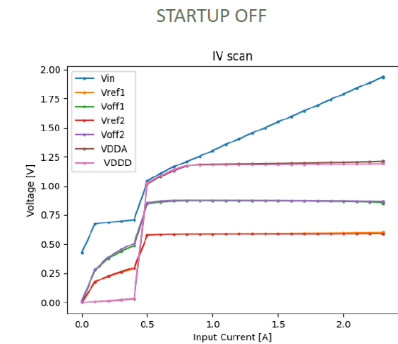
✗ **Undershunt protection:**
Reduces $Vout$ in case of *some* overload cases

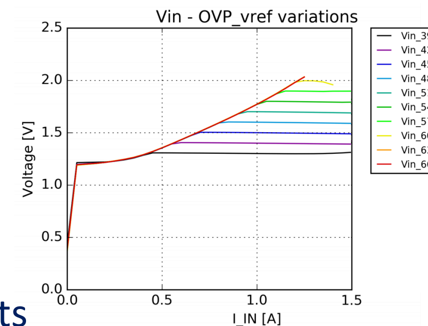
✗ **Low power mode:**
Enabled by *extra* AC signal for detector integration tests

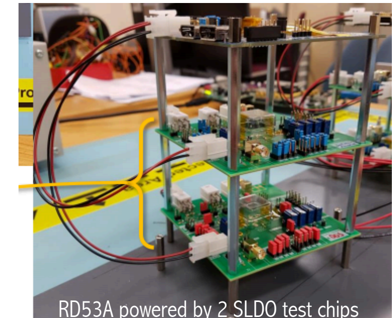
STARTUP ON



STARTUP OFF

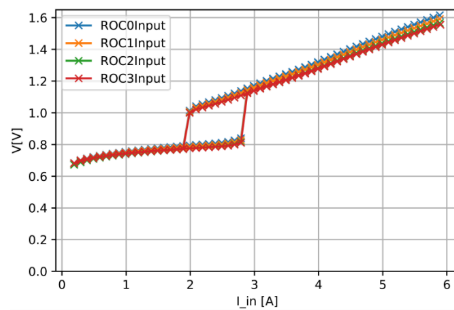


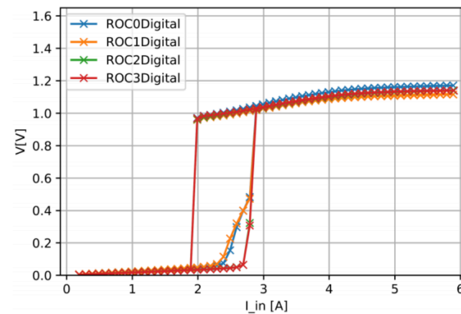


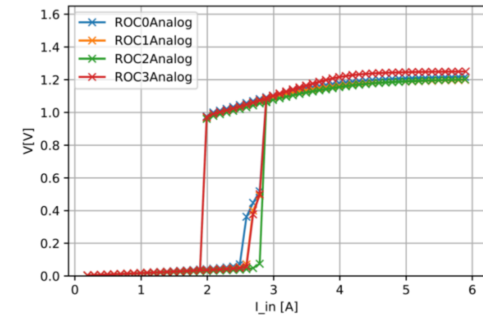

RD53A powered by 2 SLDO test chips

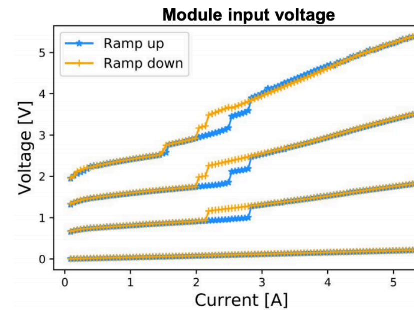
RD53A digital modules
Current sharing & SP operation

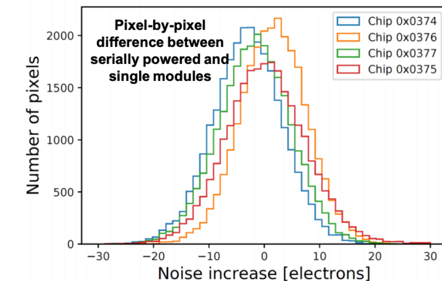
Start-up VI show the known RD53A late start-up issue (fixed in RD53B)
No noticeable noise increase from SP operation









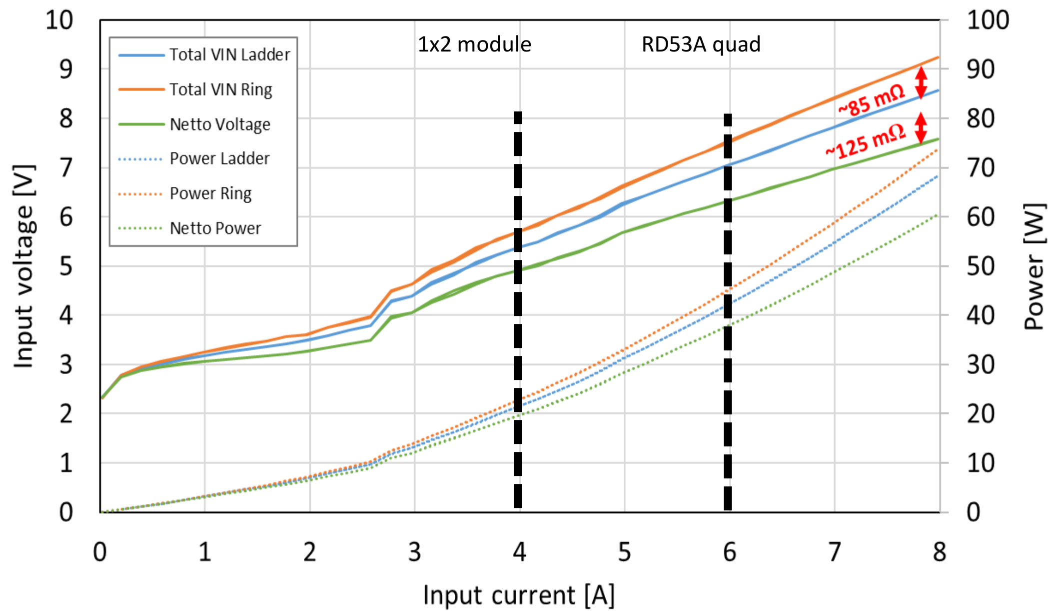


V. Perovic, ETHZ

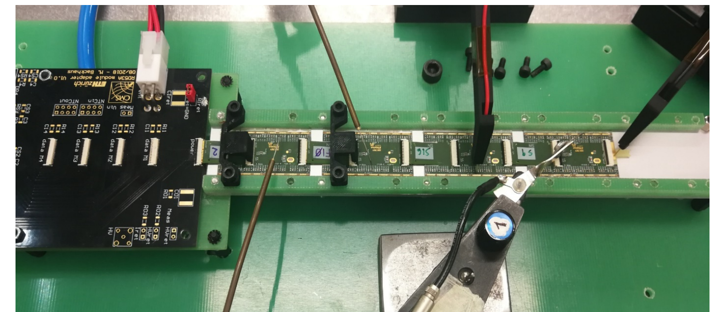
RD53A quad modules serially powered: Ring & Ladder

Successful operation with Vdrop matching simulations.

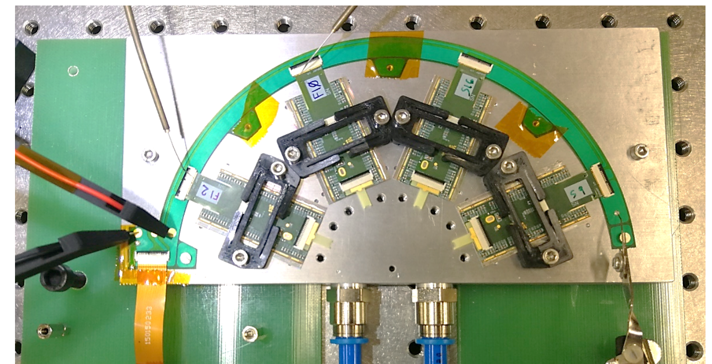
IV curve for whole structure with 4 modules
(excluding input connection)



Barrel structure power chain using module pigtails



Ring structure with Alu-flex power distribution



D. Koukola, CERN

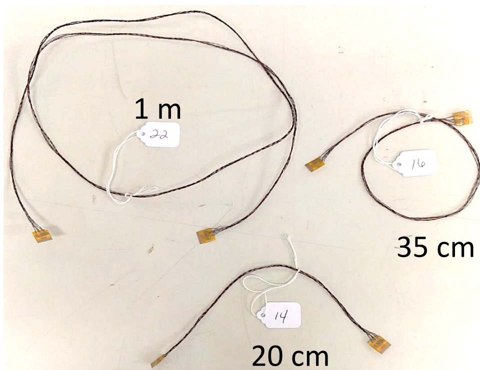
Elinks prototypes

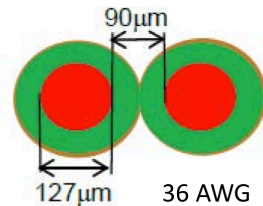
AWG36 has been used to readout SCCs and modules successfully electrically and optically.
Still considering AWG36 or flex for the disks.

Prototypes with 5 diff. pairs (4 up-links, 1 down-link) to readout RD53A digital modules.

Copper + polyamide Twisted Pairs up to 1.4m:
AWG 36 or AWG 34, not shielded

Flex Prints (straight 35cm and bifurcated 40cm):
Cu mass =1.5oz (~52.5µm thick) and Cu Back plane



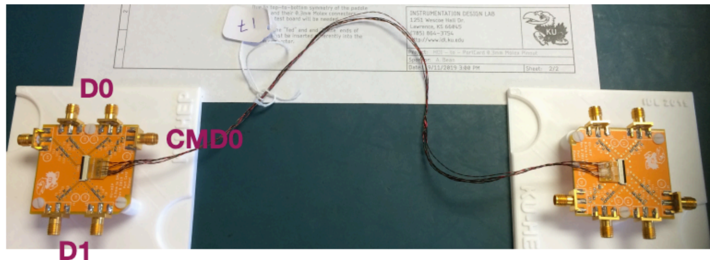


Gamma irradiation at Sandia Labs in Dec 2019 with 80-110 MRad
Thermal Cycle TP_20cm and TP_35cm up to 55° C for 4 hours

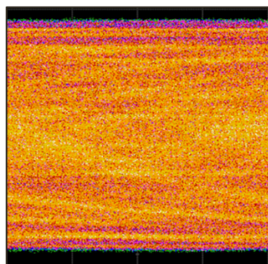
All TWP passed continuity tests, measured same DC resistance
No measured difference in eye diagrams – to be repeated to higher fluences.

Elinks + RD53A SCCs: Signal Amplitude & Pre-emphasis

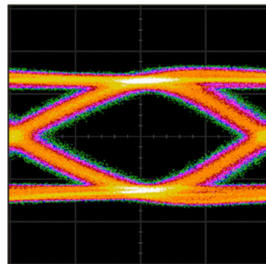
TWP and flex elinks achieve eye height and jitter specs (satisfy LpGBT input) by tuning TAP settings.



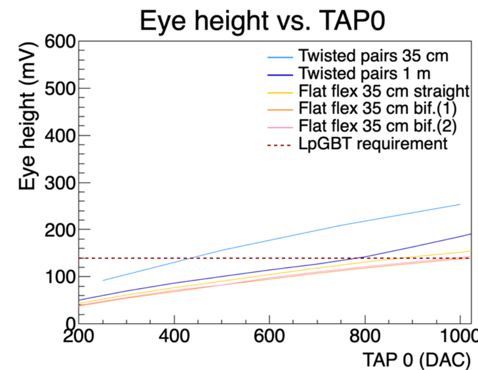
Example: flat flex cable long side (CFF 005)

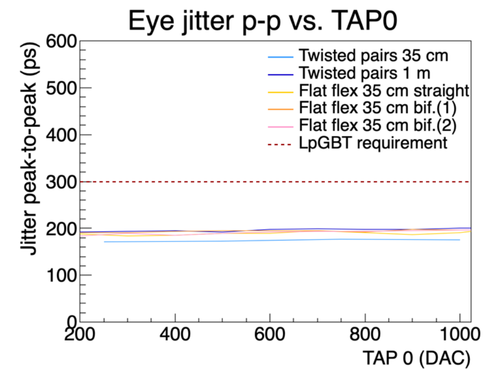


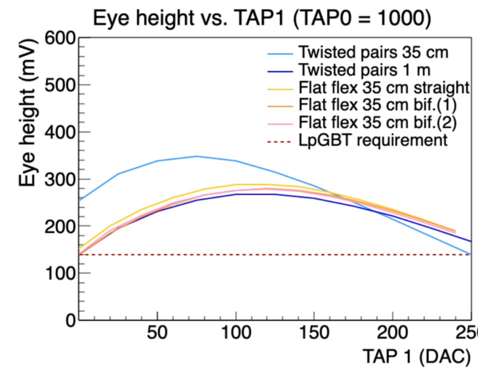
No pre-emphasis

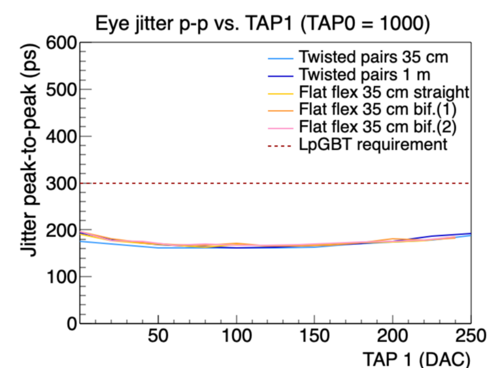


Pre-emphasis







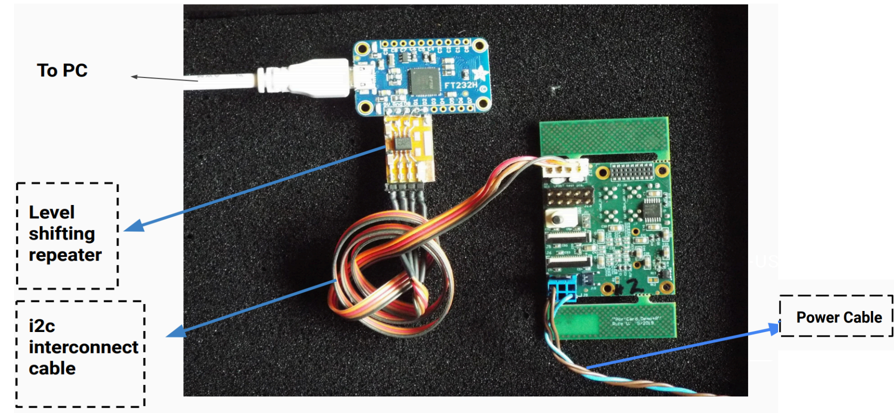


N. Emriskova, CERN

Demo Portcard

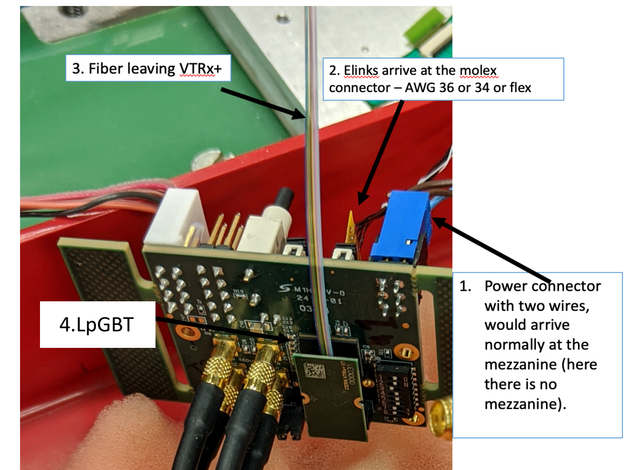
Prototype:
2 elink connectors: 2up/1down, 4up/1down
1 LpGBT
1 Versatile Link+
Extra I2C connector for lpGBT configuration

Debugging features:
Switches (lpGBT mode)
MCX (coaxial) connectors: 1up/1down
Direct powering



Successful operation and BER tests using demo portcard
lpGBT configured through I2C (next step: optical configuration)
Slow control of lpGBT and RD53A using python scripts
RD53A can generate PRBS7 → BER tests using either lpGBT or FPGA pattern checker

BER tests VS
- **LpGBT Sampling point (phase)**
- **LpGBT Equalization (recovering high freq.)**
- **RD53A Pre-emphasis (boosting high freq.)**



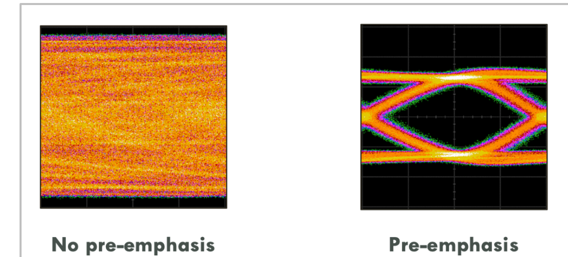
More portcards, DC-DC mezzanine available in March 2020
Ready to continue with optical configuration and realistic powering.

T. Nussbaum, K. Ecklund, A.Kumar Rice University

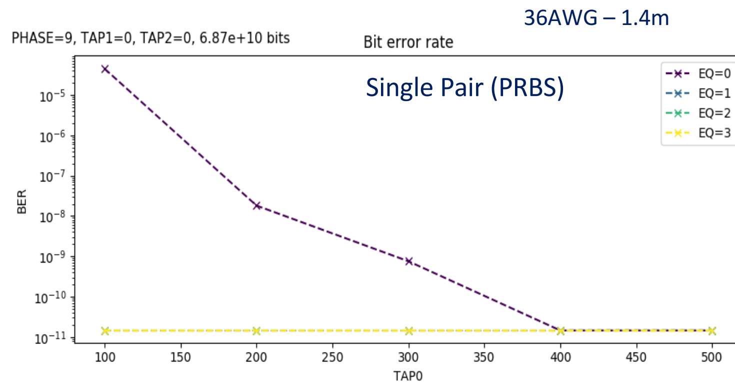
Portcard test setup: SCC

Performed tests with elinks up to 1.4m with BER<1e-11

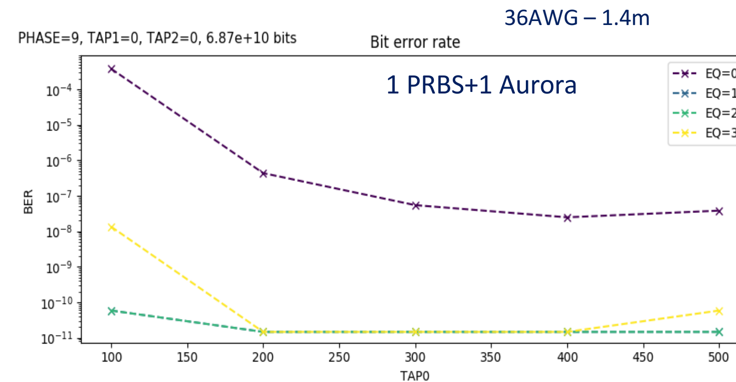
Able to lock with moderate down-link driving strength
Cross-talk tests showed promising results
To be repeated with multiple modules



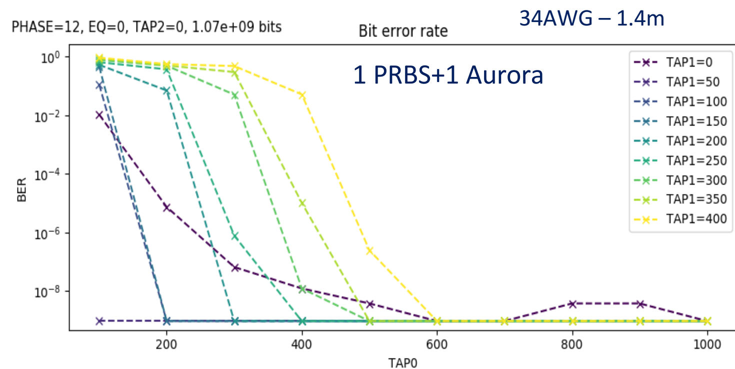
36AWG – 1.4m



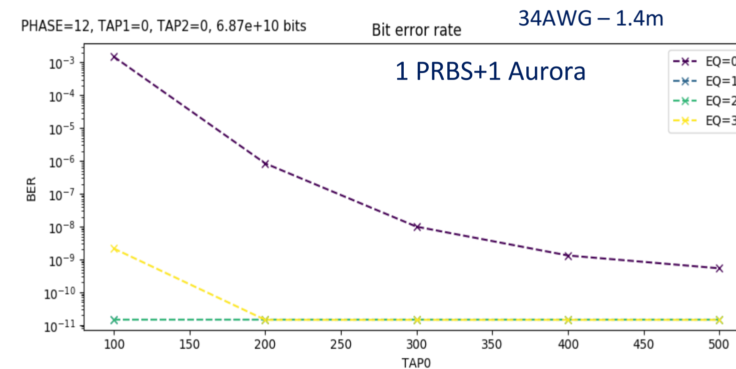
36AWG – 1.4m



34AWG – 1.4m



34AWG – 1.4m

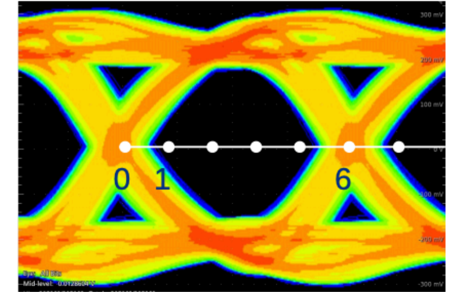


S. Wertz, UZH

Portcard test setup: TBPX/TEPX module

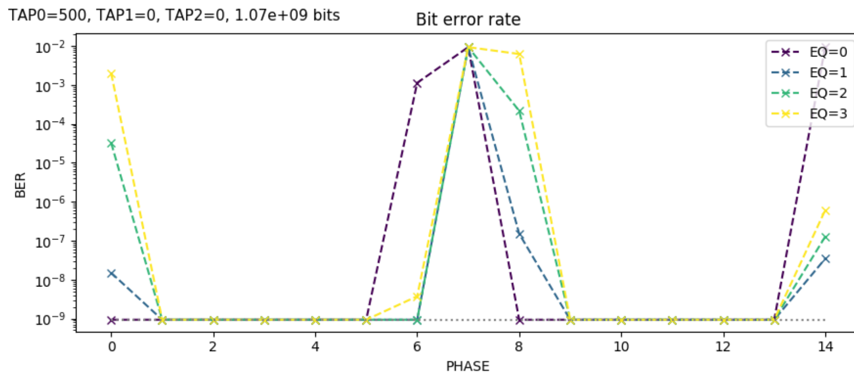
BERTs on up-links reached "low" BERs (<1e-9)

HDI reflections combined with PLL issues made difficult establishing link
Able to lock only with slower clock (40 MHz instead of 80 MHz)
Requires high down-link signal driving strength

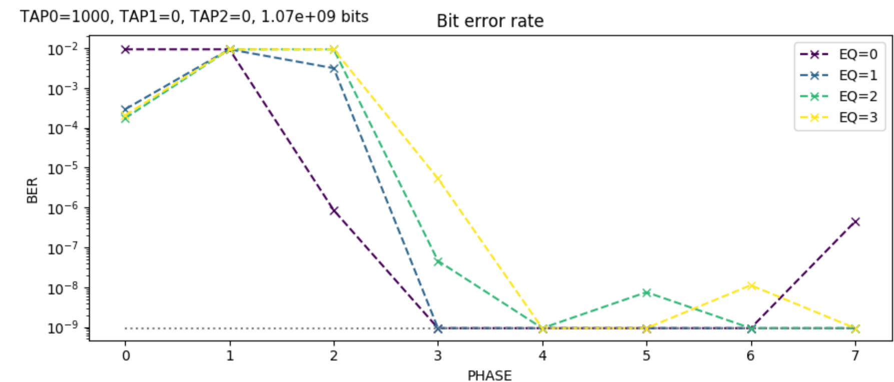


Issues -> Fixes:

PLL in RD53A known to be unreliable → fixed in RD53B
Significant duty-cycle dist. (DCD) → new PLL will be less sensitive to DCD
Reflections due to TBPX HDI (impedance matching) → new TBPX HDI design with better impedance for CMD link



Fix for PLL: downlink pattern = clk (instead of sync)



Fix for Z mismatch = clk 40 MHz (instead of 80 MHz)

Summary

- **System architecture choices for low mass services and high bandwidth readout**
  - Serial powering defines the system modularity (sensor bias and readout independent per SP chain)
  - Optical components as close as possible (radiation hard limited)
  - LpGBTs connected to modules with low mass elinks
- **Preparing for final CMS pixel chip submission in Oct 2020**
  - Demonstrator RD53A chip working – ATLAS submission in March 2020
  - LIN miniASIC excellent results
  - Significantly improved PLL/CDR and SLDO IP blocks
- **First successful power and readout system tests performed with RD53A modules in 2019**
  - System tests with RD53A quad modules in SP chains and readout tests
  - Low mass elinks and optical conversion prototype tested successfully achieving low BER
  - Using DAQ developed for uDTC based on FC7 boards