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CMS muon upgrade overview and interface to L1

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on behalf of the CMS Collaboration

ACES 2020
CERN

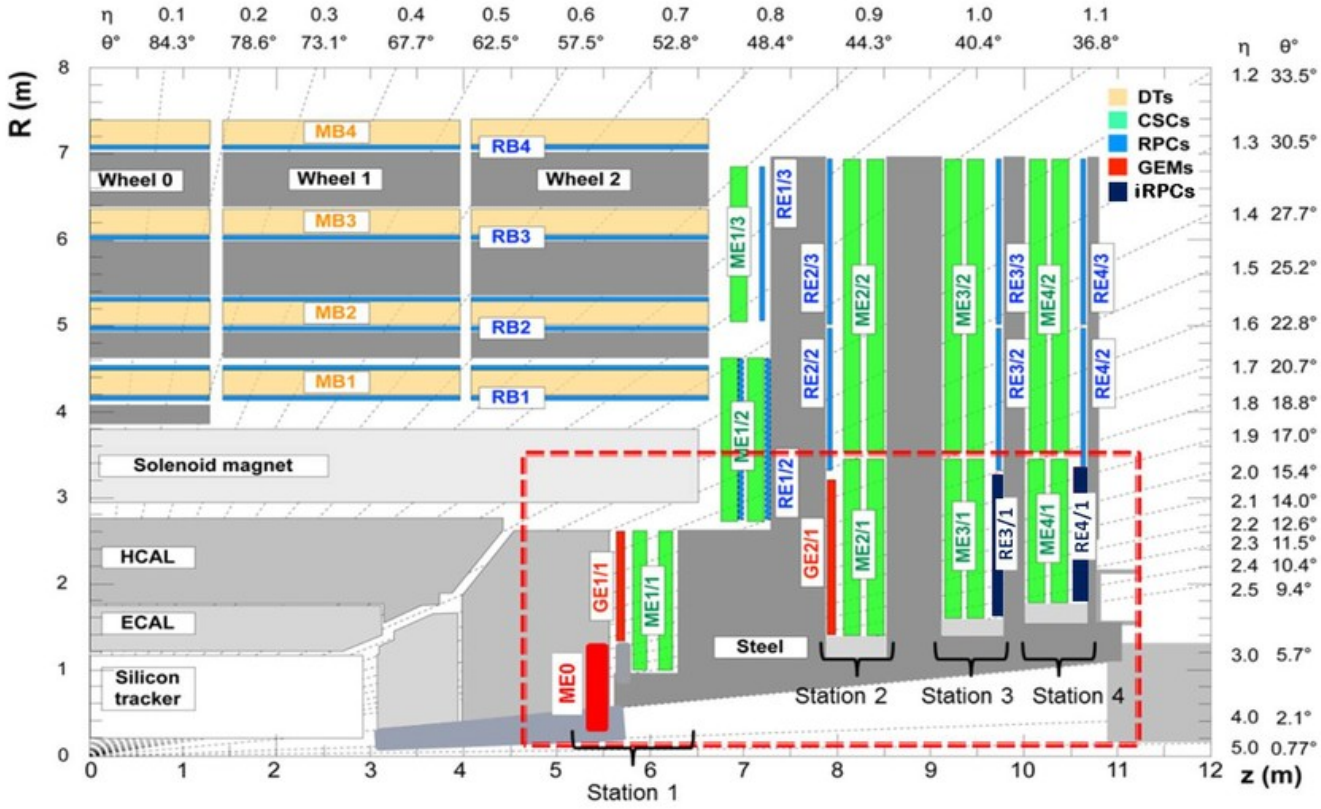
Muon Upgrade Scope

Replace electronics to cope with HL-LHC L1/DAQ specs:

- **DT:** on-detector and BE
- **CSC:** selective on-detector and all BE
- **RPC:** off-chamber readout/control

Increase redundancy forward system:

- **GE1/1:** 2 extra points
- **GE2/1**: 2 extra points
- **ME0:** 6 layers, eta-coverage is extended from 2.4 to 2.8
- **RE3/1 and RE4/1:** 1 extra point per station



Improvement of timing in trigger primitives:

- **DT**, **RPC**: sub BX resolution

Large fraction of the upgrades already completed before LS3!

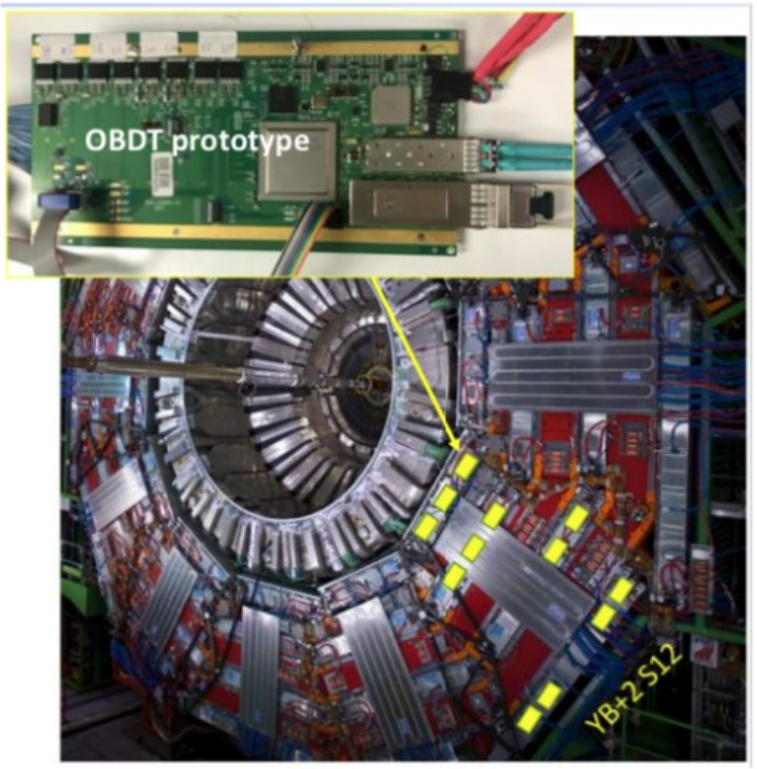
Drift Tubes (DT)

DT upgrade overview

- 940 new front-end boards (OBDT)
- 96 back-end boards
- improved performance
- capability to comply with HL-LHC requirements
- installation in LS3

Move trigger primitive (TP) functionality to back-end:

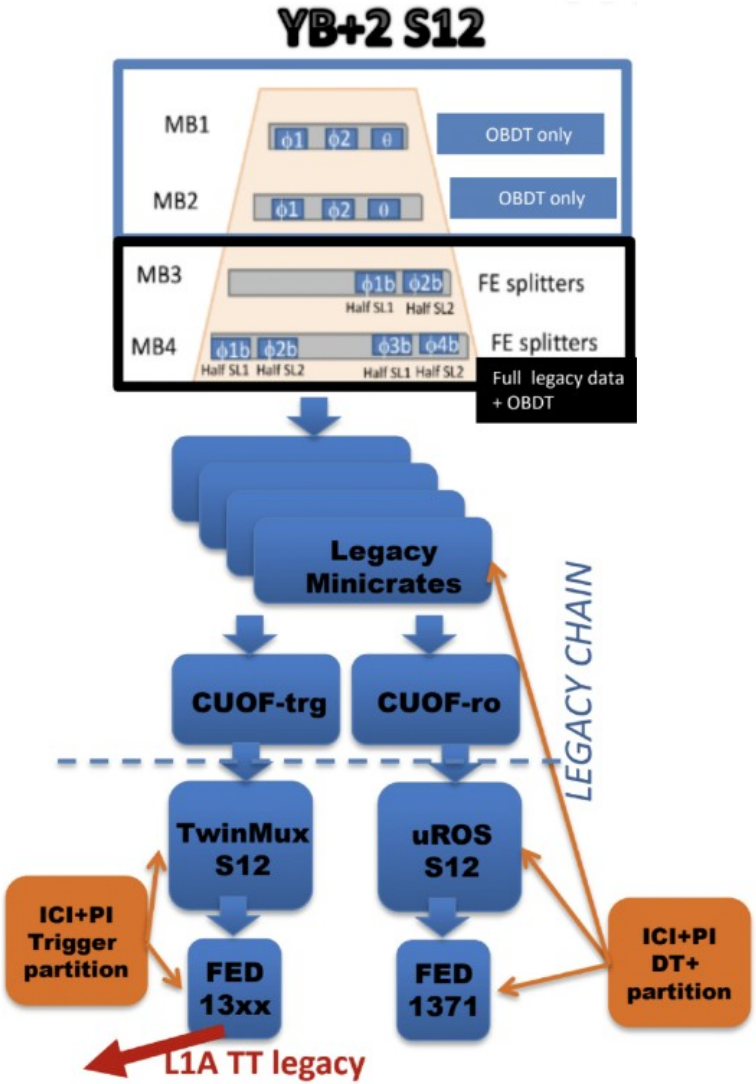
- higher efficiency (using more than 4 layers to form TPs)
- more flexibility to combine DT and RPC hits for TPs
- better timing at L1 trigger

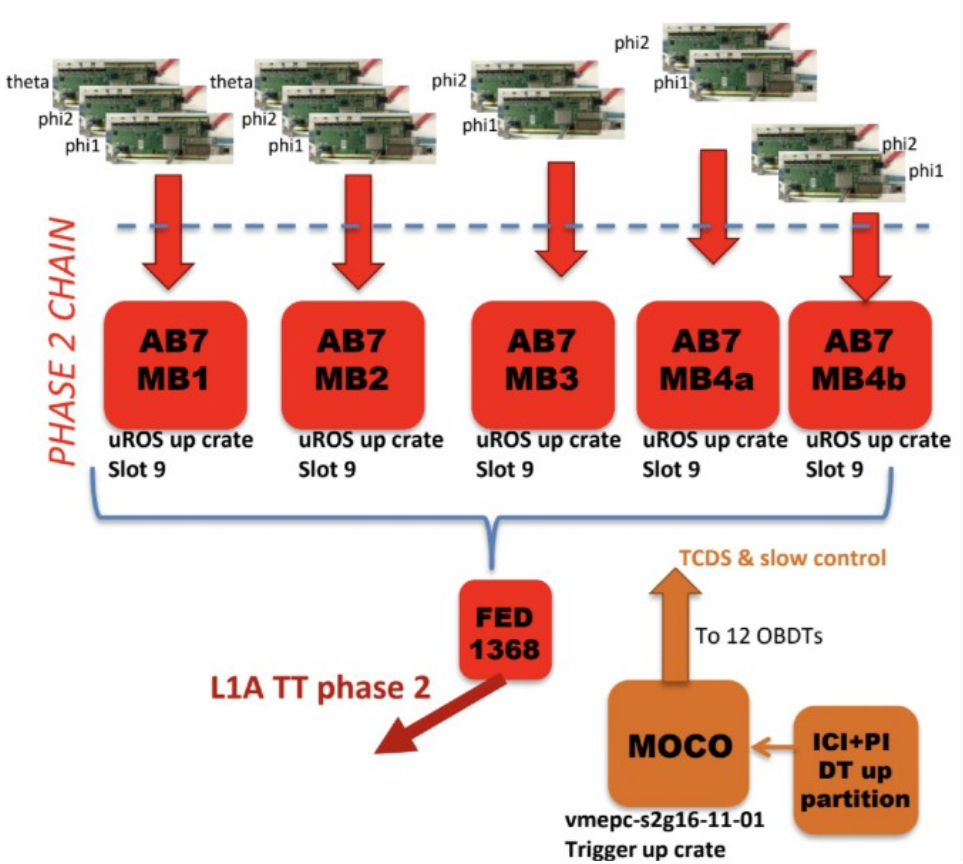


phase 2 slice test:

- one full sector with prototypes of new electronics and mechanics
- new and legacy electronics read out in parallel
- triggering on phase 2 TPs

DT: Slice test trigger and readout path

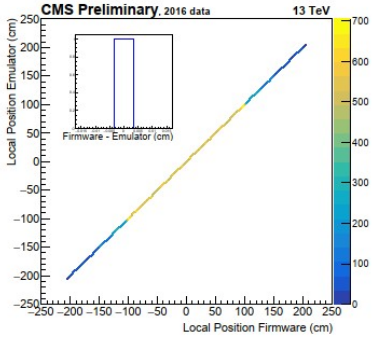


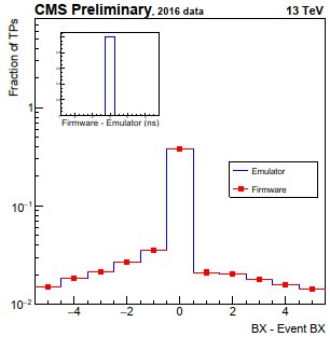


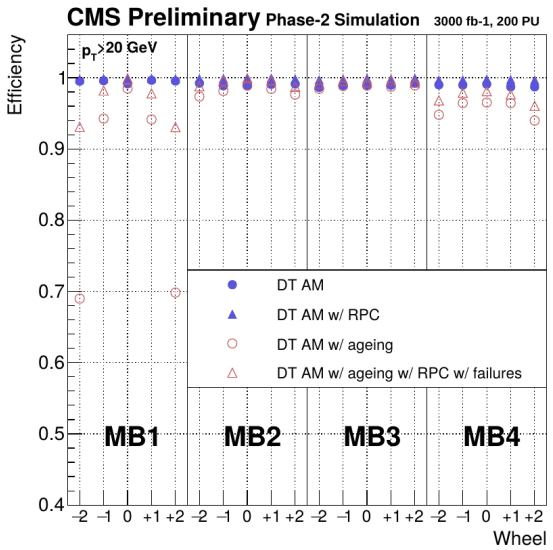
DT: Analytical Method (AM)

In addition to new electronics, new algorithm for TP generation at HL-LHC
→ profits from better time binning (1 ns instead of 12.5 ns)

- computes TP's crossing time, position, and local direction
- resolution close to current offline resolution
- algorithm implemented in firmware and in software as emulator shows good agreement







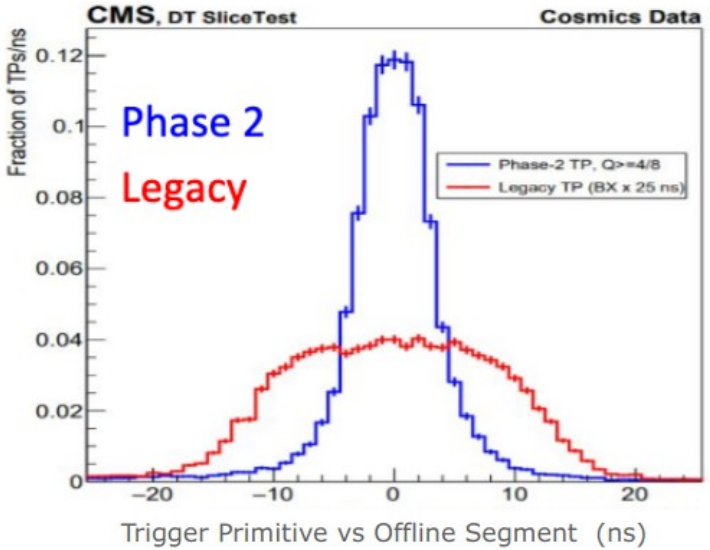
- TP efficiency w.r.t. reconstructed segments
- DT-only efficiency decreases due to aging, mostly in MB1 external wheels where aging effects are larger
- RPC helps recovering efficiency

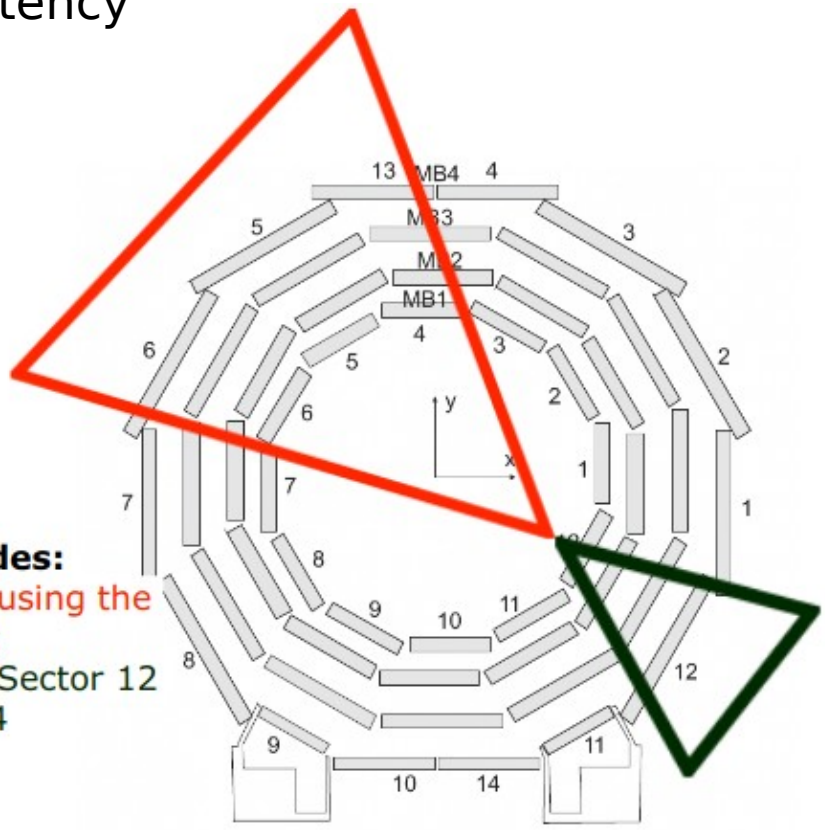
DT: phase 2 slice test

Extended cosmic runs taken at P5:

- event by event comparisons show full consistency
- OBDT architecture and firmware validated

Sub-bx time resolution
@ L1 demonstrated





Data Taking Modes:

1. Cosmic trigger using the opposite quadrant
2. Cosmic trigger Sector 12 with MB3 and MB4
3. Test Pulse

→ poster on DT Slice Test by Bilal Kiani

Cathode Strip Chambers (CSC)

CSC upgrade motivation

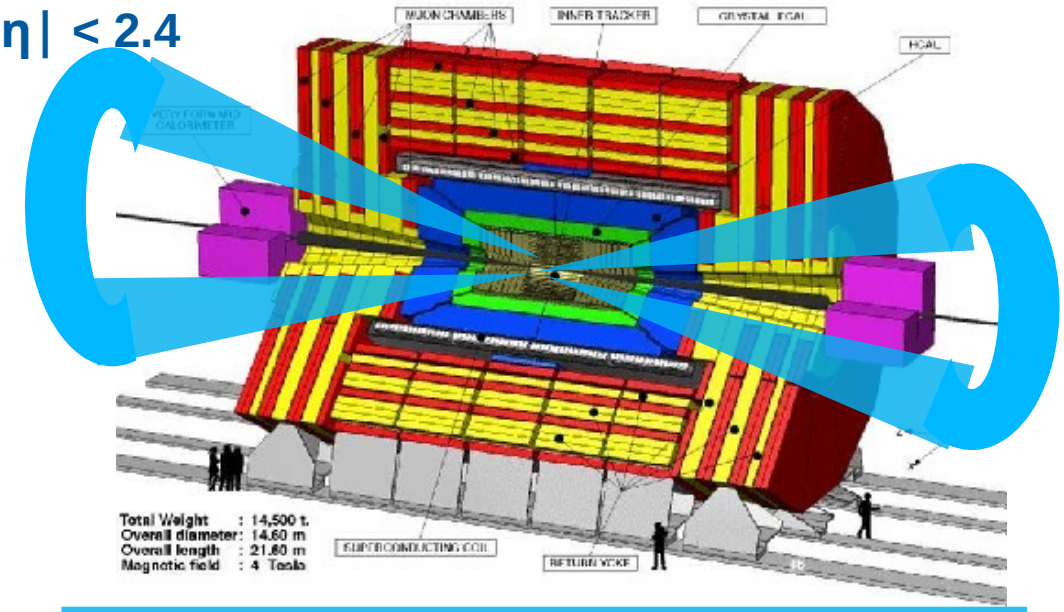
Electronics upgrade of the high-eta CSCs (innermost rings)

Limiting factors of the present electronics:

- **L1 trigger rate:** old CFEBs do not have enough buffering for chambers closest to beamline
- **Longer L1 trigger latency:** required for new track trigger
- **Output bandwidth** (ALCT, DCFEB, ODMB, FED) and **pipeline length** (ALCT) not sufficient
- GBTx programming to mitigate EEPROM failures experienced in 2017 in high-occupancy CSCs (ME1/1)

HL-LHC schedule imposes changes after LS3, but CMS **installation opportunity in LS2**

$1.6 < |\eta| < 2.4$

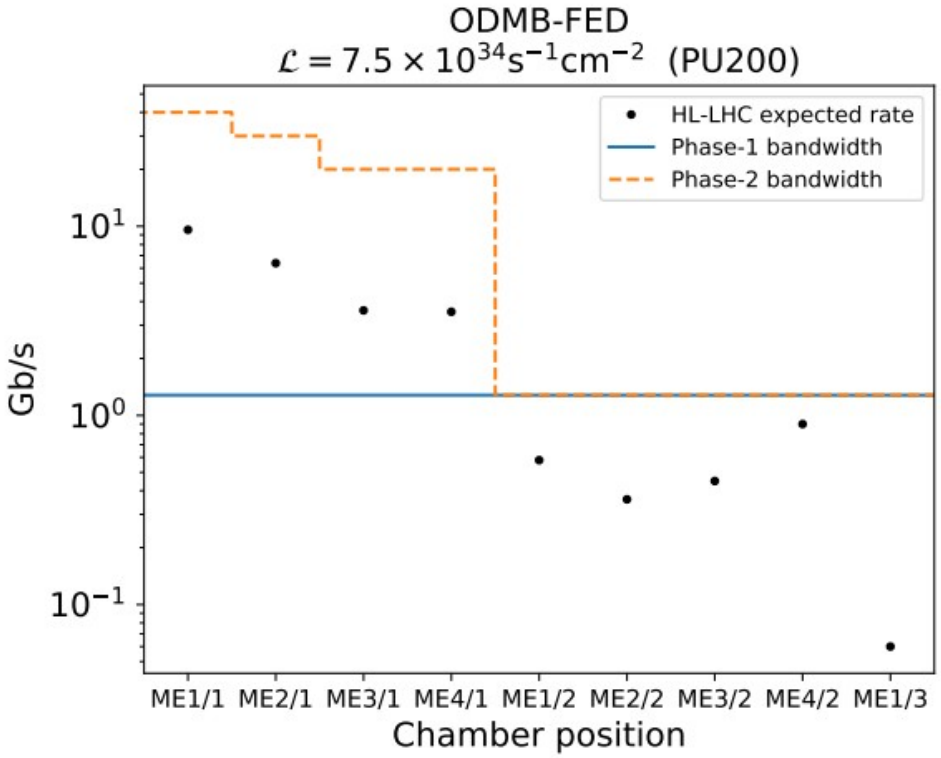


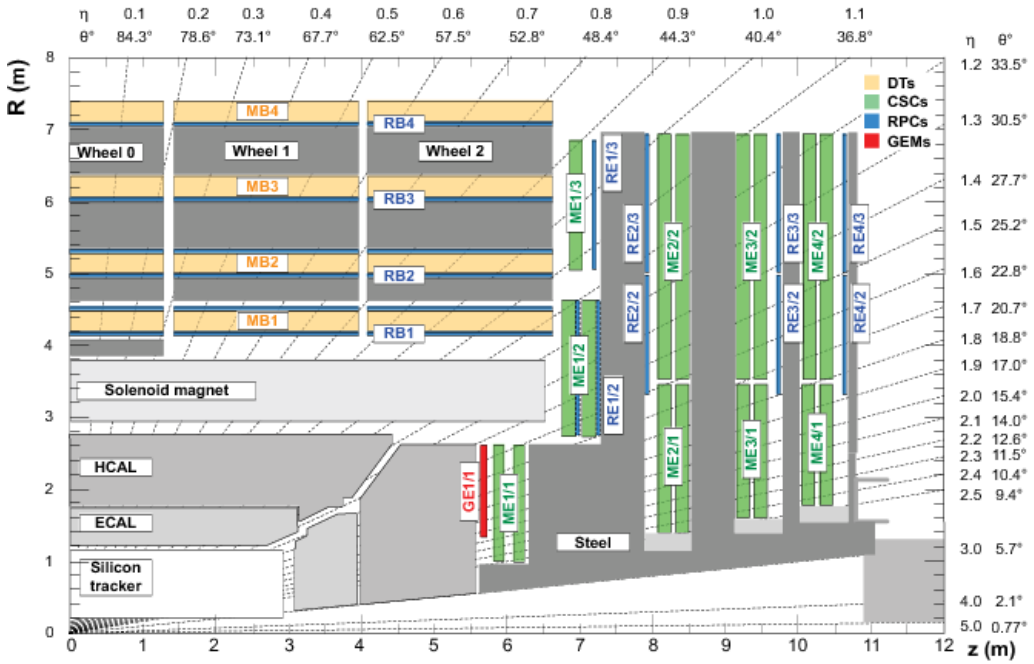
Approximate angular region of the inner rings:
ME1/1, ME2/1, ME3/1, ME4/1
= 180/540 chambers

CSC upgrade motivation: data output

Bandwidth of ODMB output (currently 1 Gb/s) insufficient for expected HL-LHC rates

→ upgrade of optical links and redesign of backend with ATCA technology

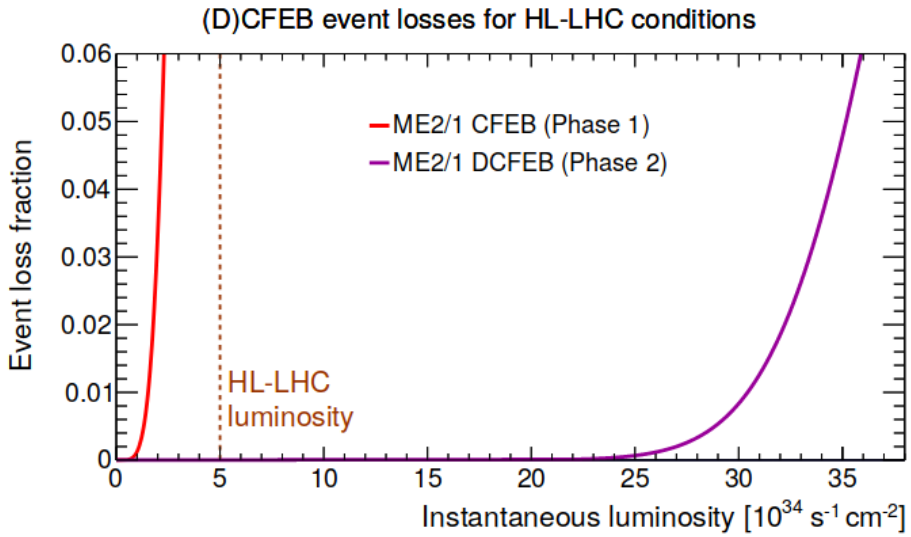


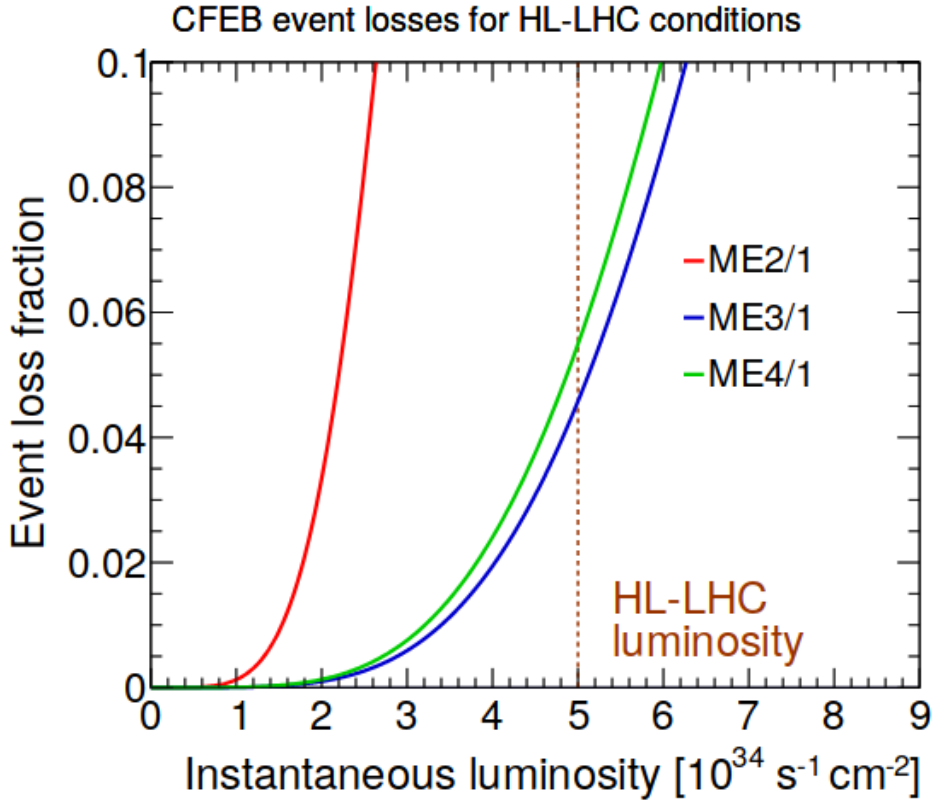


CSC upgrade motivation: front-end

Expected data loss with current electronics due to:

- insufficient buffer size of front end electronics
- longer latency requirements
- insufficient output bandwidth due to higher L1 trigger rates and occupancy





Expected to lose entire ME2/1 ring with current CFEB
→ no data loss with upgraded DCFEB

Radiation hardness

Electronics need to survive high rate of collision and background particles, especially in inner ring chambers

→ new boards and components (optical transceivers, regulators, EPROM, …) underwent radiation tests

at CHARM, CERN (mixed hadron spectrum)

Texas A&M cyclotron (neutrons)

UC Davis cyclotron (protons)

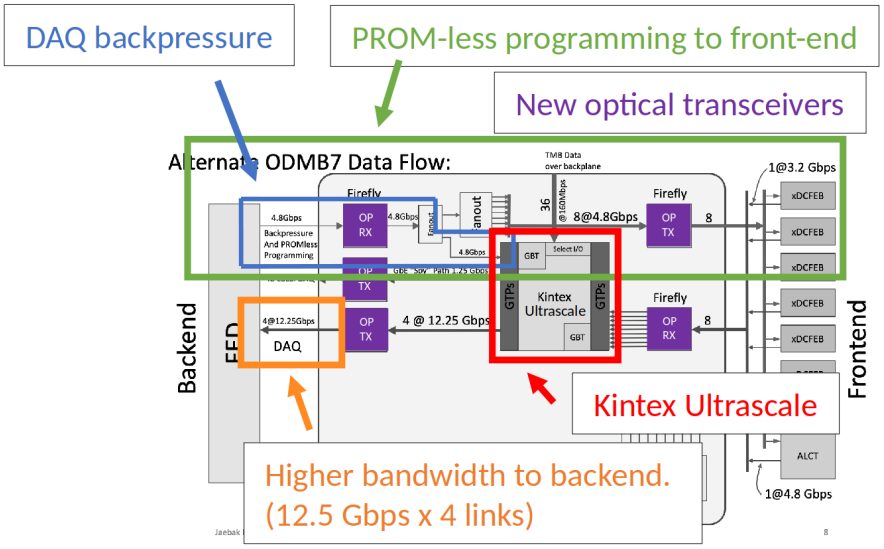
- total integrated dose up to 300 Gy
  (3x expected 100 Gy for 3000/fb at HL-LHC)

- susceptibility of electronics to single-event upsets (SEUs)
  change of state caused by one single ionizing particle striking a sensitive node in a micro-electronic device
  - study SEU rate and electronics deadtime

ODMB and FED system: status and plans

ODMB located in peripheral crates, to be upgraded during LS3

- schematics and layout done
- procuring equipment and preparing for board testing
- successful irradiation tests of Firefly, more components will follow
- next: pre-production fabrication



New features of ODMB7/5

FED system:

- several types of DMBs/ODMBs to interface with
- planning 9 boards with 100 RX (60 CSCs) each (in total 900 RX, 180 TX needed)
- FED will program 2 types of boards via PROMless (xDCFEB, ALCT)
- pilot system at P5 (end Run 2) very useful to gain experience and improve fw
  → exploring possibility to continue running this system in Run 3

Gas Electron Multiplier (GEM)

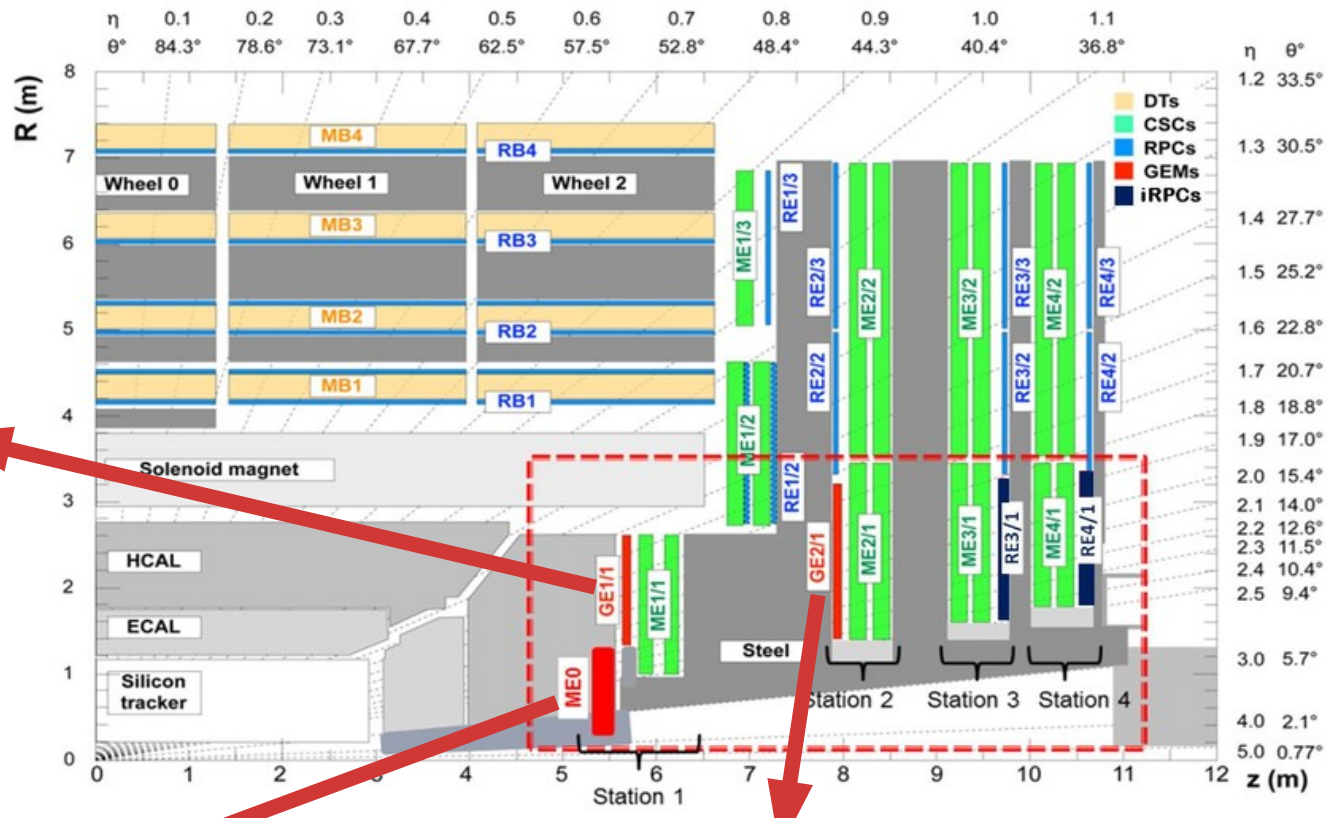
GEM overview

new detectors

→ new front-end and back-end electronics

GE1/1 (LS2):

- all chambers produced
- half already installed → commissioning ongoing
- FE electronics integration and validation ongoing for second half



ME0 (LS3):

- very high expected particle rate (up to 142 kHz/cm^2)
- testing and development ongoing with prototype electronics

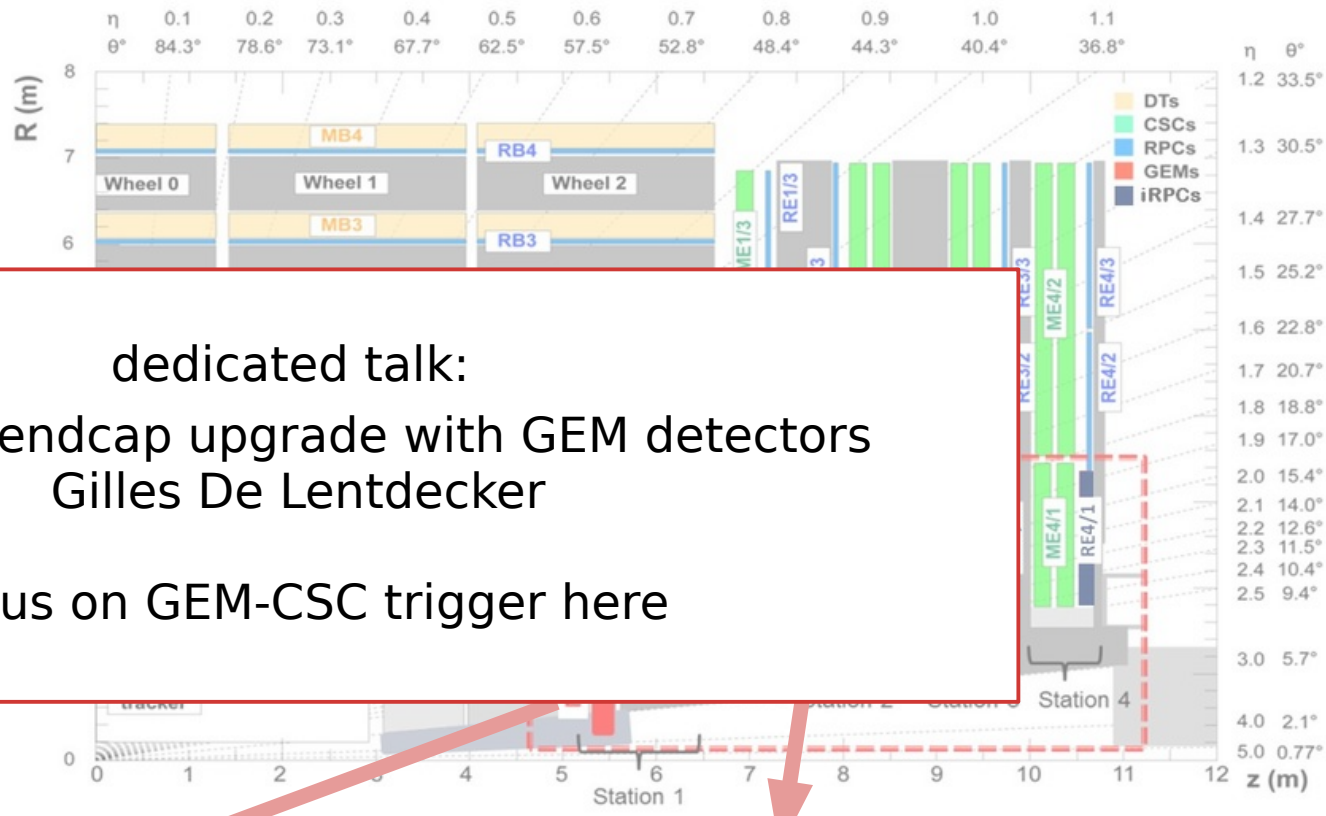
GE2/1 (before LS3):

- similar to GE1/1
- design improvements from GE1/1 experience

GEM overview

new detectors

→ new front-end and back-end electronics



GE1/1 (LS

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- half alrea
  → commi
- FE electr
  and valid
  second h

dedicated talk:

CMS muon endcap upgrade with GEM detectors
Gilles De Lentdecker

focus on GEM-CSC trigger here

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- very high expected particle rate (up to 142 kHz/cm^2)
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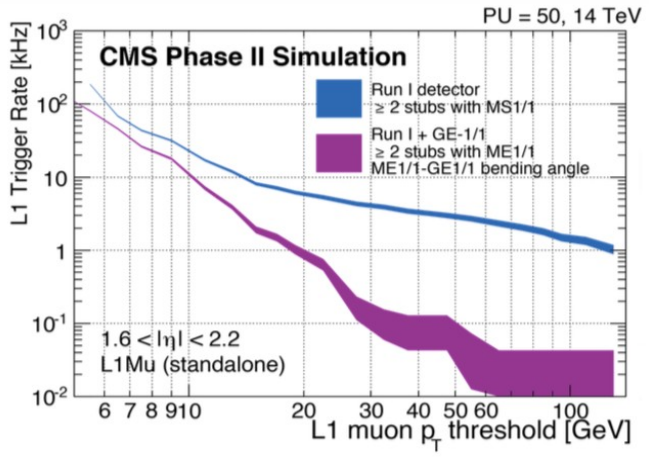
GEM-CSC trigger

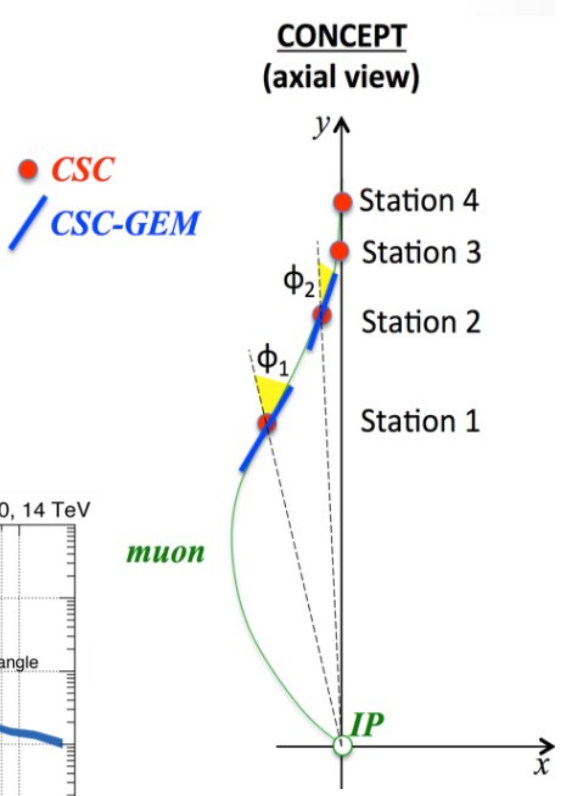
GE1/1 and GE2/1 next to CSC chambers:

- combine CSC and GEM information
- boost segment-finding efficiency
- disentangle combinatorial “ghosts” in CSCs (short strips in GEMs)
- muon direction within a station

→ greatly improves triggering

→ large physics impact:
Higgs, EW measurements and new physics searches (e.g. long-lived particles decaying to muons)





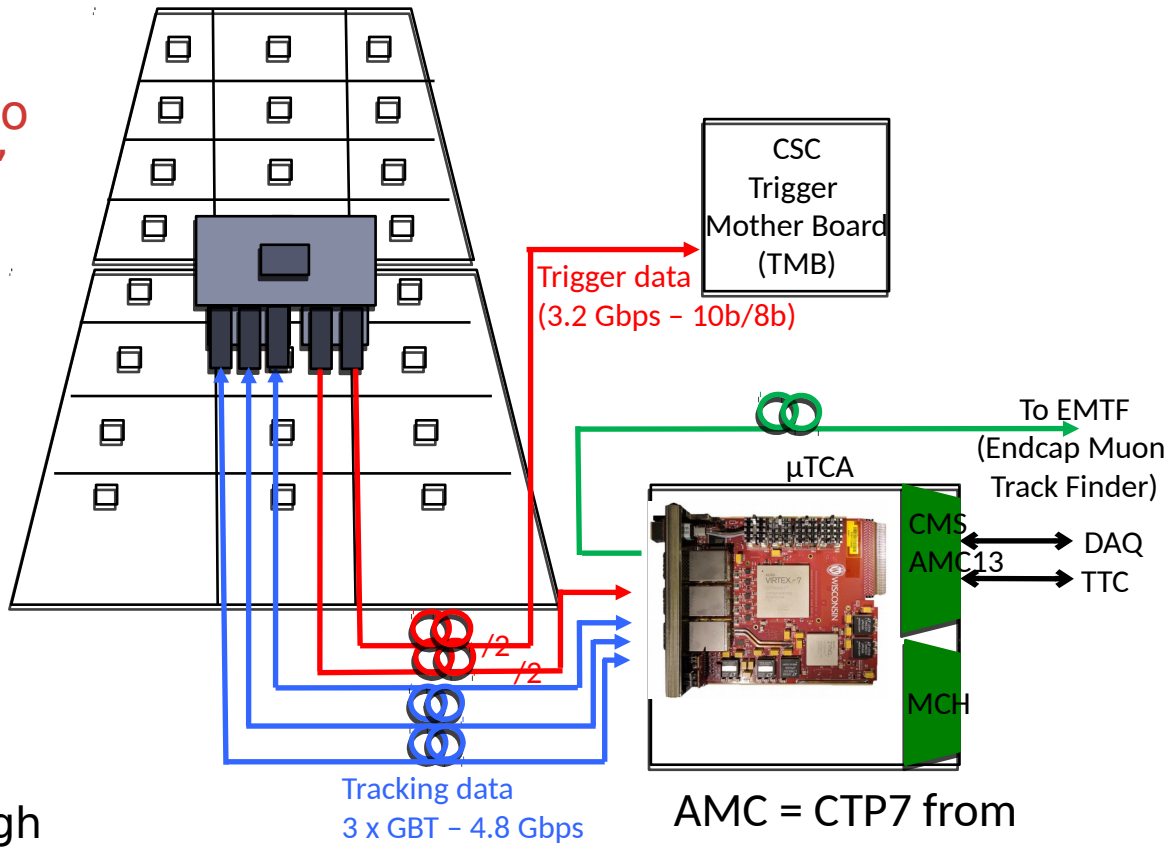
GEM-CSC trigger

Trigger data sent to CSC OTMB and Encap Muon Track Finder (EMTF)

New CSC OTMB design will allow receiving trigger primitives from GEM neighbouring muon system to form CSC+GEM “super-primitives”

ongoing developments to:

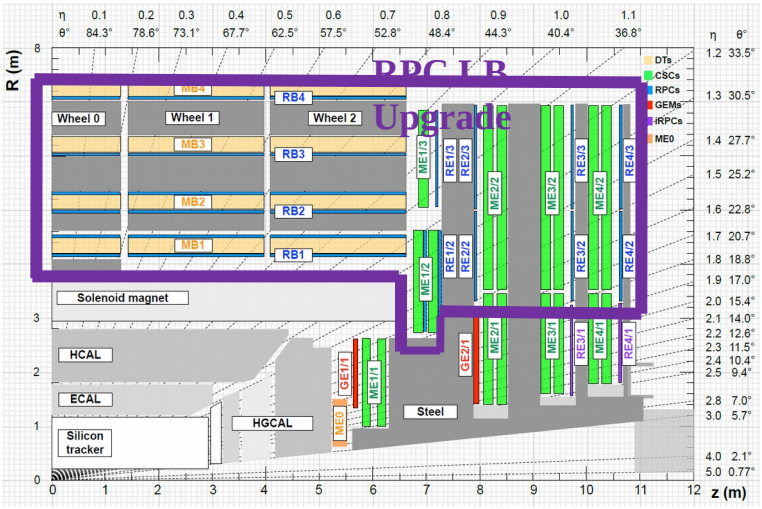
- improve position and bending resolution
  → control trigger rate by cutting out low-p_T muons at EMTF level
- implement GE1/1-ME1/1 trigger
  → improve CSC trigger efficiency with additional redundancy from GEM
- extend reach of CSC trigger for high multiplicity signatures from exotic origins



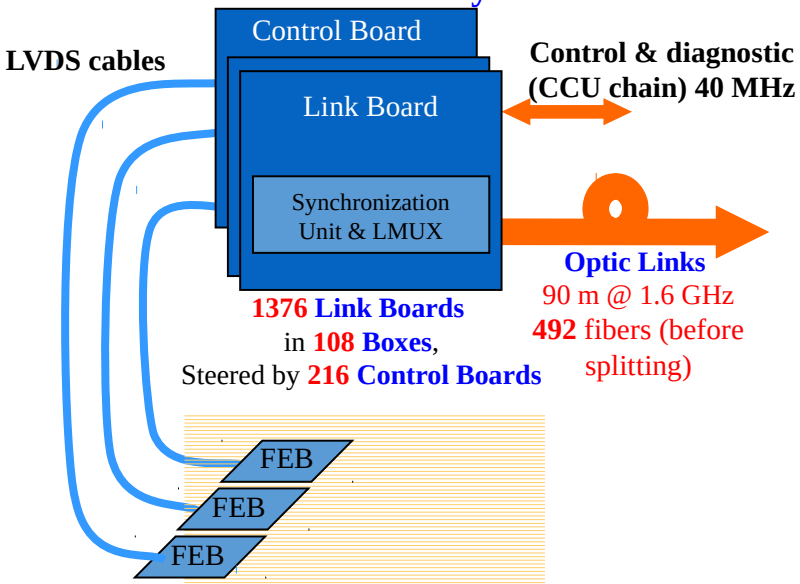
AMC = CTP7 from CMS Trigger upgrade

Resistive Plate Chambers (RPC)

RPC Link System upgrade (LS3)



Present Link Board System

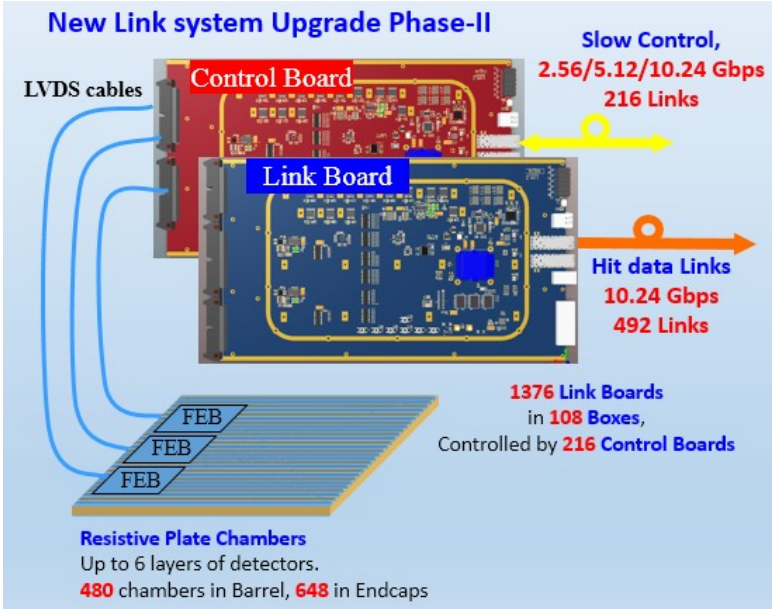


Upgrade Motivation

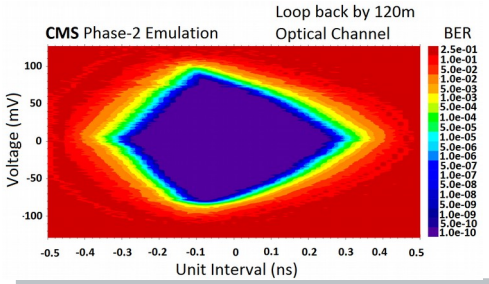
- CMS trigger system based on 25 ns sampling, despite intrinsic RPC resolution
- Data transmission speed 1.6 Gbps
- Control, diagnostic and monitoring of Link system designed based on CCU ring (combination of copper cable and fiber), very susceptible to electromagnetic interference
- CCU ring not very fast, 40MHz bandwidth shared between 12 control boards
- Most rad hard electronic components are obsolete
- Electronic aging of Link system (13 years old by end of LS2)

RPC Link System features and status

1. FPGAs are KINTEX-7
2. Muon hit time: 1.56 ns TDC timing resolution
3. Master Link board output data rate : 10.24 Gbps
4. Control Board communication with slow controller at 10.24 Gbps
5. Embedded internal buffer (DDR3) : 1.28 Gbyte
6. Radiation mitigation: TMR + Internal Scrubbing
7. Scrub rate of entire FPGA (real time SEU detection and correction) : 13ms (SEU rate at balcony : every 413000 ms)



→ Initial validation of link board final prototype has started



Data Transmission

Two FPGAs through 120m optical fibers:

- opening eye efficiency: 50 - 55%
- stable error free ($<10^{-14}$) during 48h test runs

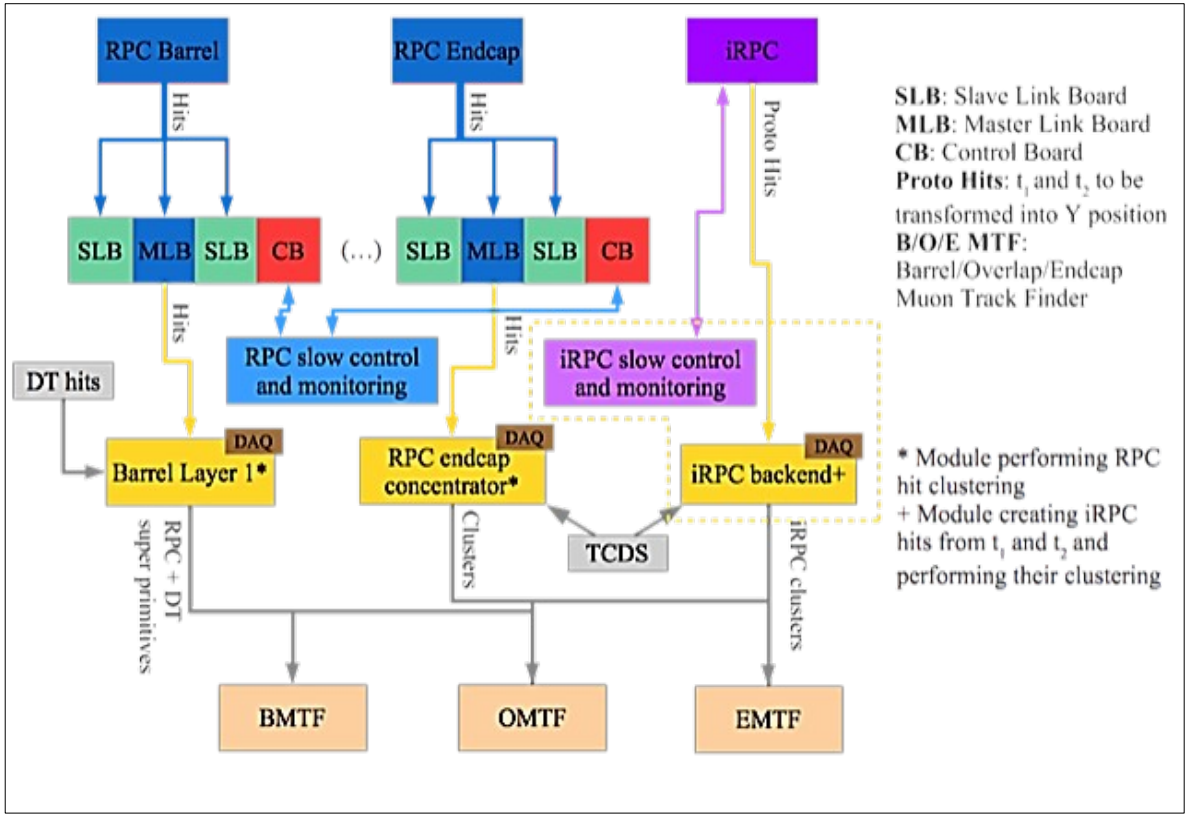
RPC Layer-1 Trigger and new Link System hits data frame format

Item	Header + FEC	Number of Hits (1..14)	No. Strip (1..96)	Sub-bx	LB No.	...	BCN	BC0	Partition delay	End of Data
Bit	24	4	7	4	4	...	12	1	3	2

10.24 Gbps bandwidth
→ each frame has **256 bits/bx**
(32 bits/bx with current Link System)

Frame contains

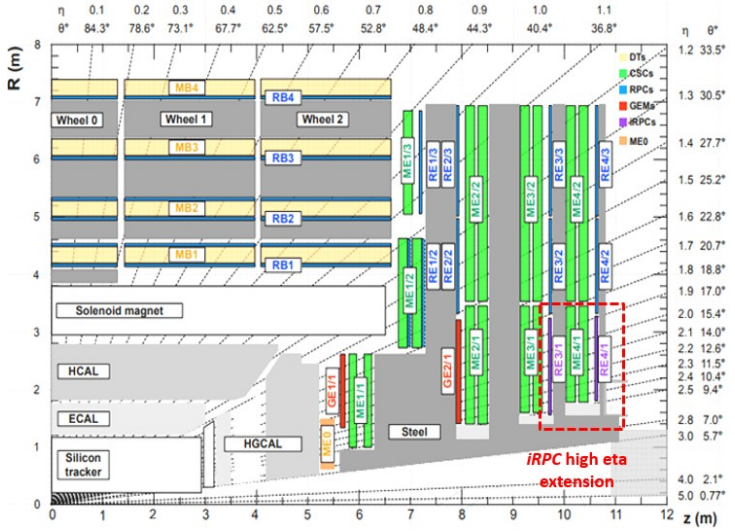
- number of hits
- **fired strip number** with **sub bx** timing information
- partition delay, in case not all hits fit inside one frame and are sent in next frames

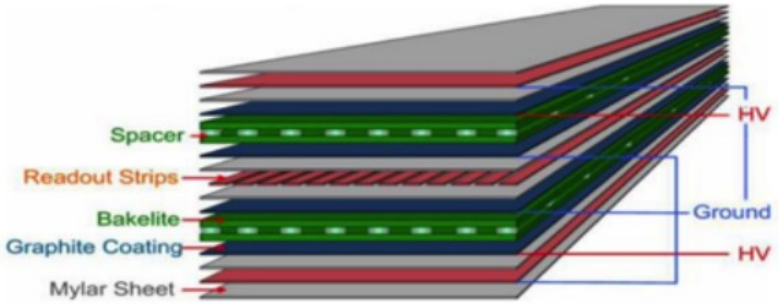


RE34/1

Scope:

- 72 new iRPC (improved RPC)
- dedicated FE and BE electronics
- services (LV, HV, gas cooling)
- installation: YETS 23/24 (backup LS3)





	Present system	iRPC
$\|\eta\|$ coverage	0 – 1.9	1.8 – 2.4
Max expected rate (SF = 3 included)	600 Hz/cm^2	2 kHz/cm^2
η resolution	~ 20 cm	~ 2 cm
T resolution	12.5 ns**	< 1 ns

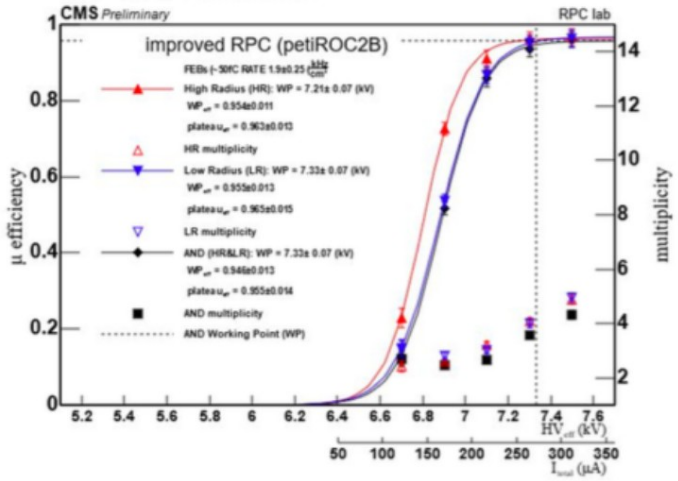
RE34/1 FE electronics validation

FEBv0: A board that contains:
- ➢ **1 PETIROC2A ASIC + FPGA (Cyclone 2)**
- ➢ Ethernet-based communication was conceived to read out the strips PCBV0 (44 strips)

FEBv1: This was intended to come closer to the final board to be compatible with CMS DAQ:
- ➢ **2 petiroc2A(B) + FPGA Cyclone V**
- ➢ Ethernet-based communication is used to read out the strips PCBV1 (48 strips)

Validation of FEB_V1

- An iRPC with **FEB_{V1}** was tested using a cosmic muon trigger made with shielded scintillators
- Efficiency plateau is≈95% with≈2kHz/cm2 of background and a threshold of 50fC
- Upgraded teststand to work inside GIF++
- irradiation tests are planned for Sep 2020 and then again in 2021 with the final rad-hard version



Summary

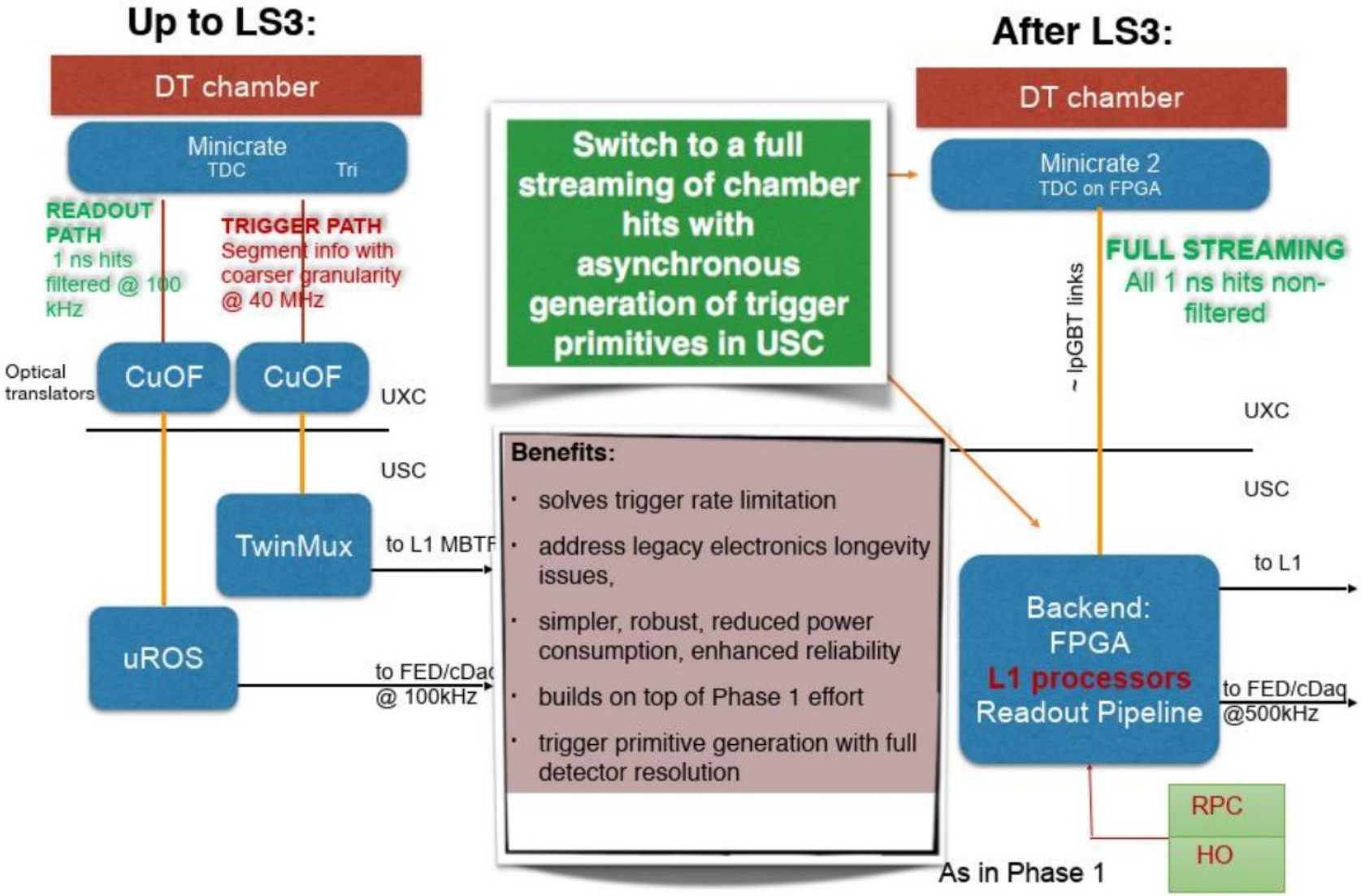
- Major electronics upgrade of existing muon systems
- Addition of new detectors, requiring new electronics
- Compatibility with HL-LHC L1/DAQ specs, but also:
  - improve timing resolution
  - extend eta coverage
  - improve on the triggering
  - improve radiation tolerance

have a look at DT slice test poster tomorrow morning

stay connected for GEM talk!

Backup

DT: Upgrade scope



The Analytical Method

The algorithm is developed in three steps:

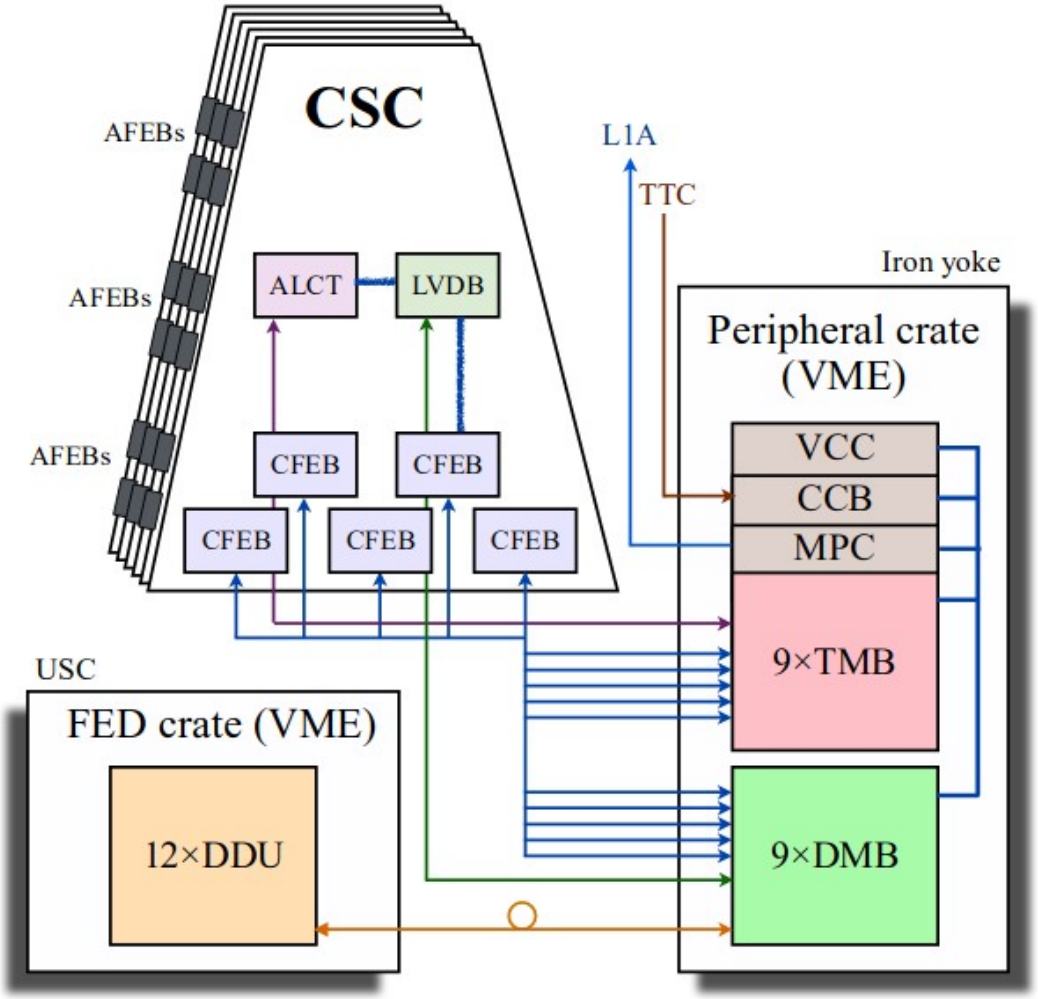
- **Grouping**: selects patterns of 3 or 4 DT fired cells compatible with a straight line in a single SL and their sub-patterns of 3 cells.
- **Fitting**: for each group of cells identified, computes unambiguously the BX using the mean-timer property and the track parameters using exact formulas from χ^2 minimization.
- **Correlation**: attempts a combination of compatible tracks from single SLs, re-computing SL track parameters and profiting from the larger lever arm.

Different cleaning filters applied at several stages.

- After building the AM DT primitives and clustering the RPC hits, the information from both subdetectors can be combined into a **superprimitive** (SP), exploiting the redundancy and complementarity of the two subsystems and combining DT spatial resolution and RPC time resolution.

CSC Electronics

- strips are read out and processed by **Cathode Front-End Boards (CFEBs)**
- wires are read out and processed by the **Anode Local Charged Track (ALCT) board**
- **Low Voltage Distribution Board (LVDB)** is providing power to the boards
- **Trigger Motherboard (TMB)** and **Data Motherboard (DMB)** are located in peripheral crates located at the periphery of the endcap disks
- backend: data sent from DMB to **detector dependent unit (DDU)** in Front End Driver (FED) crate (= interface between front end electronics and global CMS data acquisition system)



Upgrade scope

LS2

Anode Local Charged Track electronics: replace mezzanine cards to **increase latency capability and output bandwidth**

LS2

Low Voltage Distribution Boards: replace to provide voltages and currents for Digital Cathode Front End Boards

LS2

Trigger Motherboard: replace with optical Trigger Motherboard to receive Digital Cathode Front End Board trigger data, increased algorithmic power

LS2

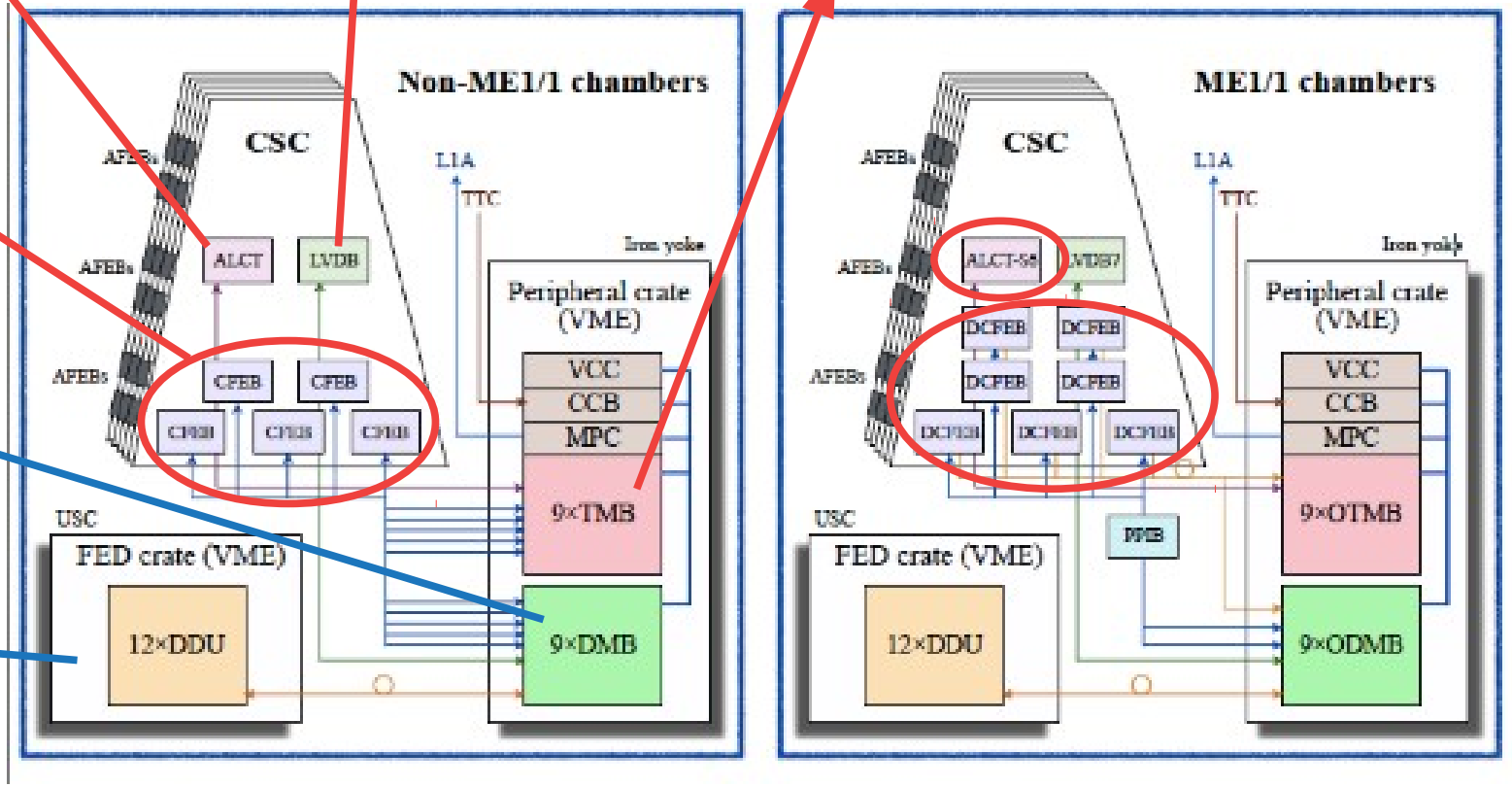
Cathode Front End Boards: replace with Digital Cathode Front End Boards with **increased latency and rate capabilities**

LS3

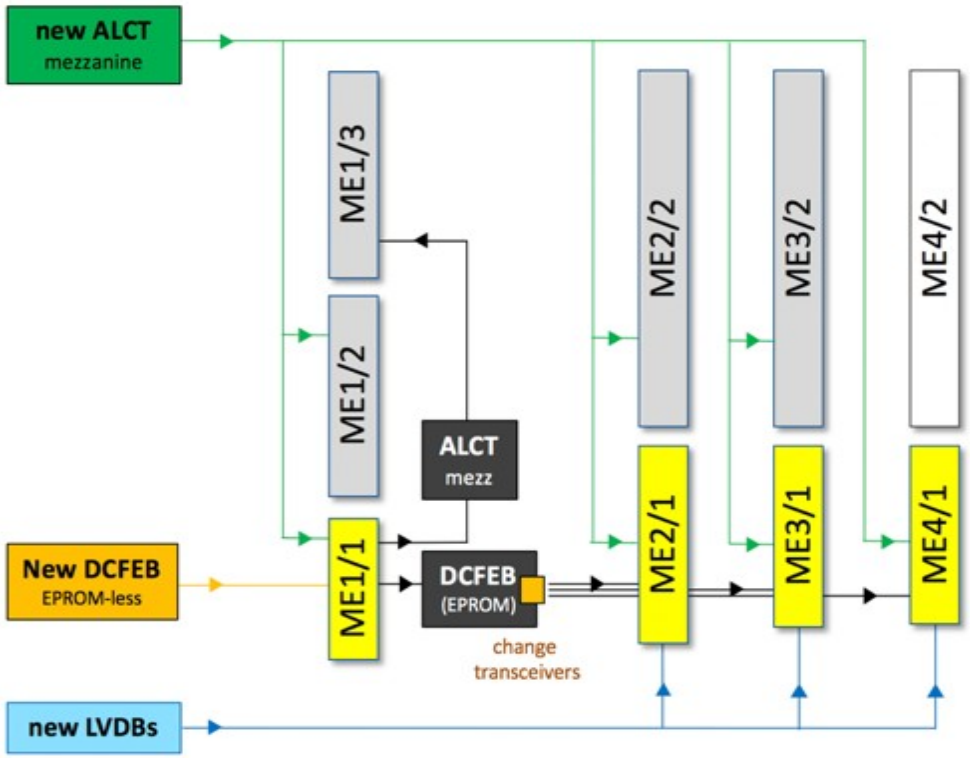
Data Motherboard: replace with optical Data Motherboard to receive Digital Cathode Front End Board data

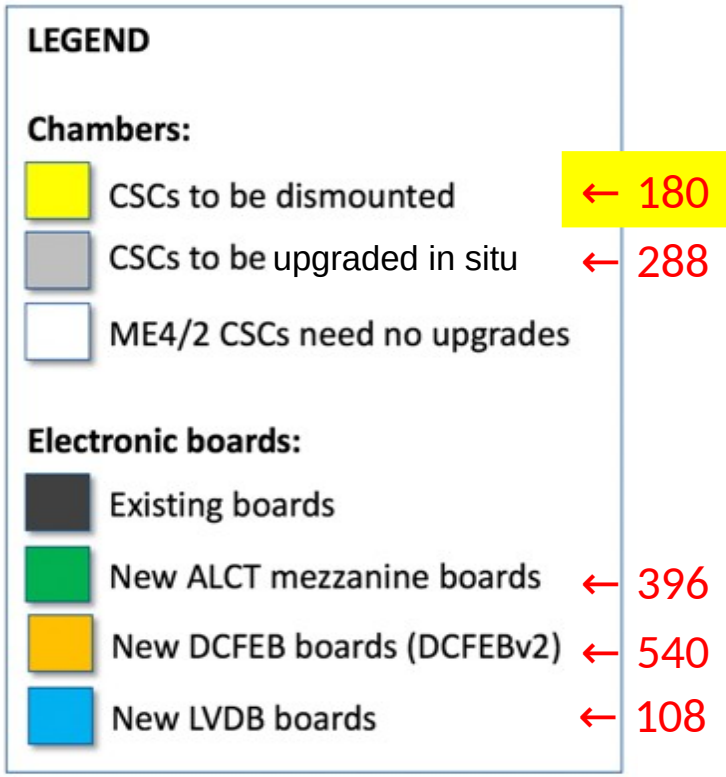
LS3

Front End Driver: **increased data volume**, number of links



CSC: LS2 upgrade effort





+ OTMBs (peripheral crates) ← 108

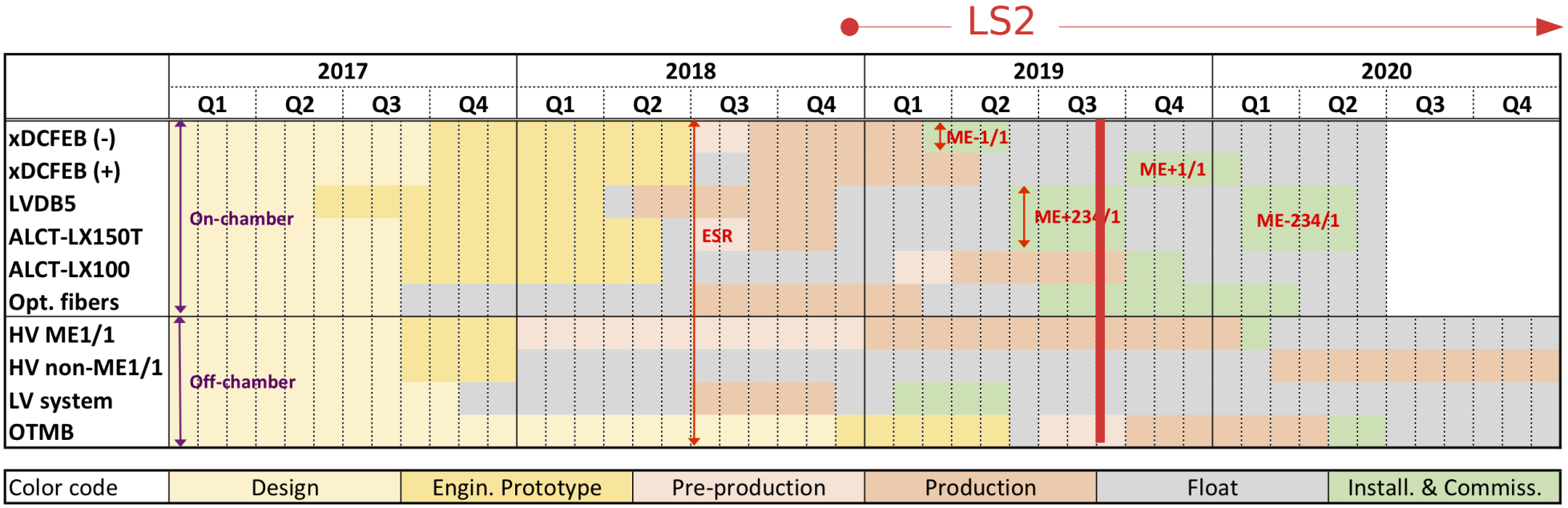
+ HV system: custom system with higher current monitoring resolution, as used on other rings to have homogeneous system

+ LV system: to provide appropriate voltages and currents to the new electronics

Timeline

LS2 (2019-2020) : on-chamber electronics (DCFEB, ALCT, LVDB)
+ Trigger Motherboard (OTMB)
+ general services (LV, HV)

LS3 (2024-2026) : Data Motherboard (ODMB) + backend
+ high bandwidth optical links

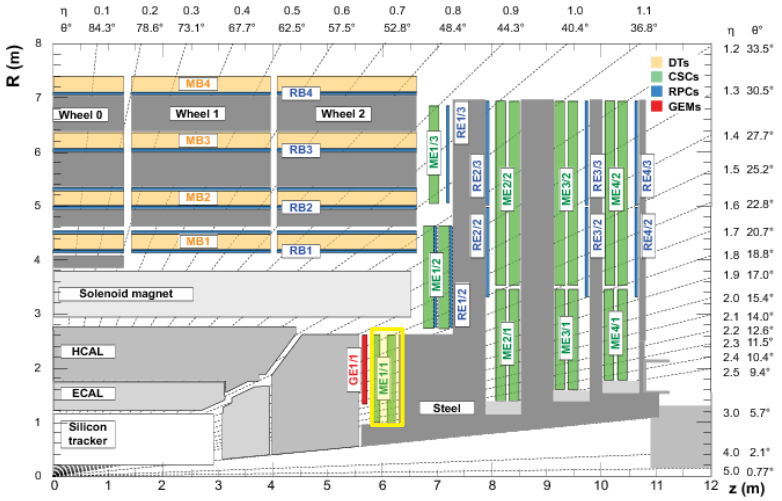


New Digital Cathode Front End Board (xDCFEB)

LS2

Remote programming of FPGA via Gigabit optical Transceiver (GBTx) as alternative to programming via EEPROM after experiencing instances of EEPROM corruption in 2017

Replacing existing DCFEBs (installed in LS1) on inner ring of station 1 (ME1/1) to enhance operational stability at highest radiation doses (~10kRad for 3000/fb at HL-LHC)



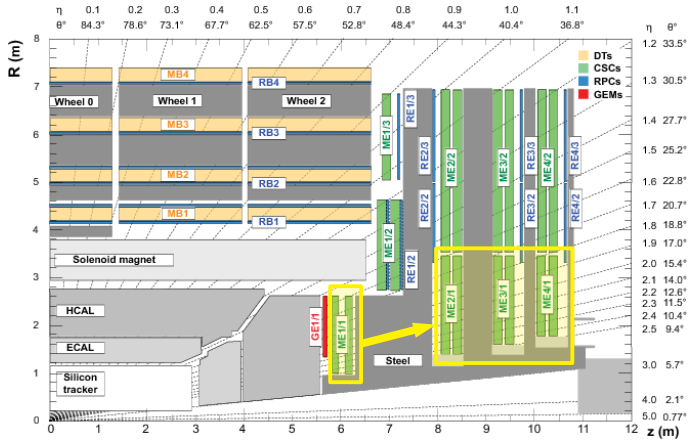
Digital Cathode Front End Board (DCFEB)

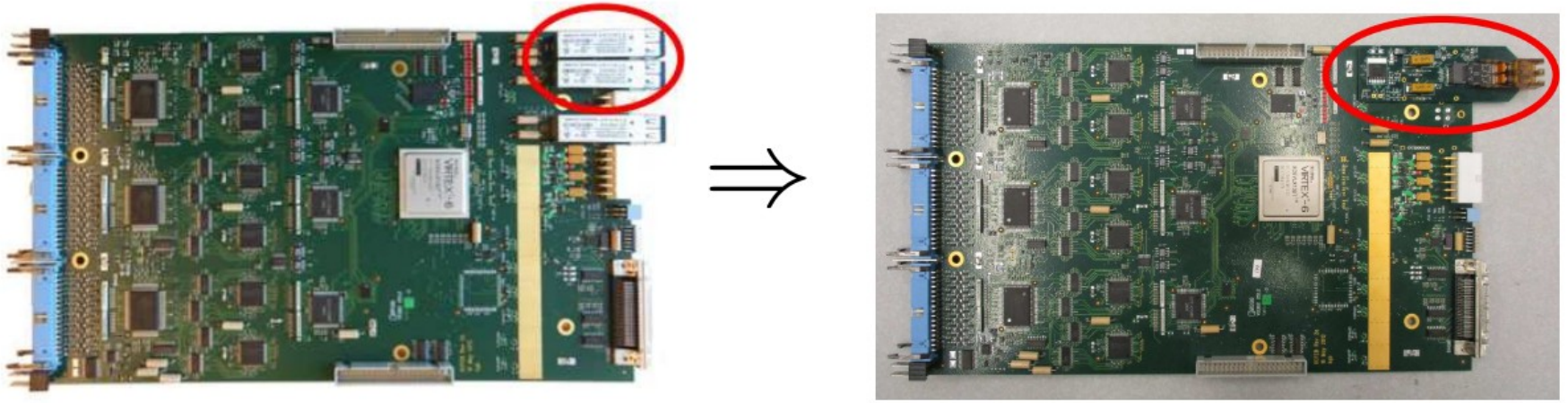
LS2

Existing DCFEBs from inner ring of station 1 (ME1/1) are being installed on CSCs of inner ring of stations 2, 3, 4 (lower radiation dose)

Additionally, replacement of optical transceivers:

- 6 (10) failing (no output light) Finisar optical transceivers in 2018 (2017)
- Temporary optical link loss due to SEU (~1/day in 2018)
  - recovered by powercycling the DCFEB
- Replace Finisars by VTTx's (SEU immune)



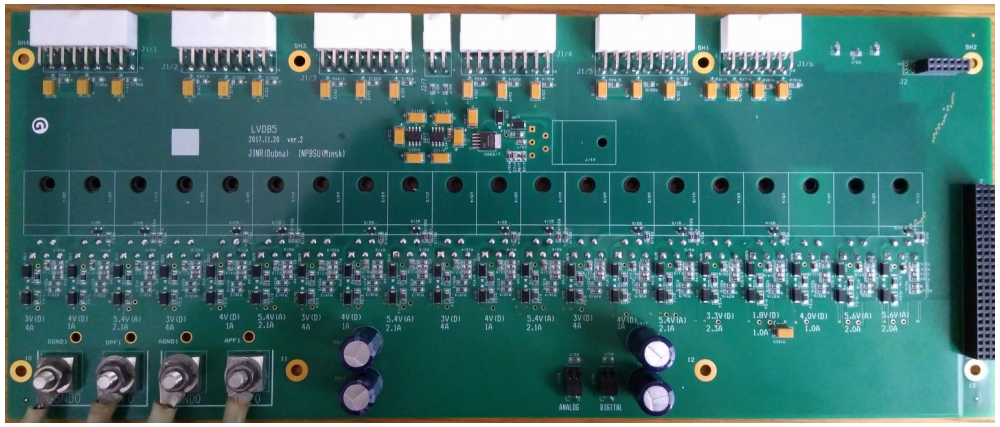


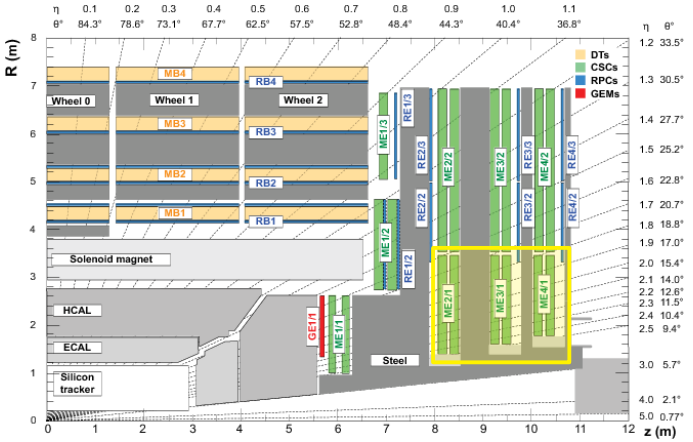
Low Voltage Distribution Board (LVDB)

New LVDB to provide increased current and appropriate voltages to the DCFEBs in inner rings of stations 2,3,4 (ME234/1)

LS2

- being installed and tested (48h burn-in test)
- LV system also upgraded to supply the necessary currents
  - additional power supplies and improved partitioning





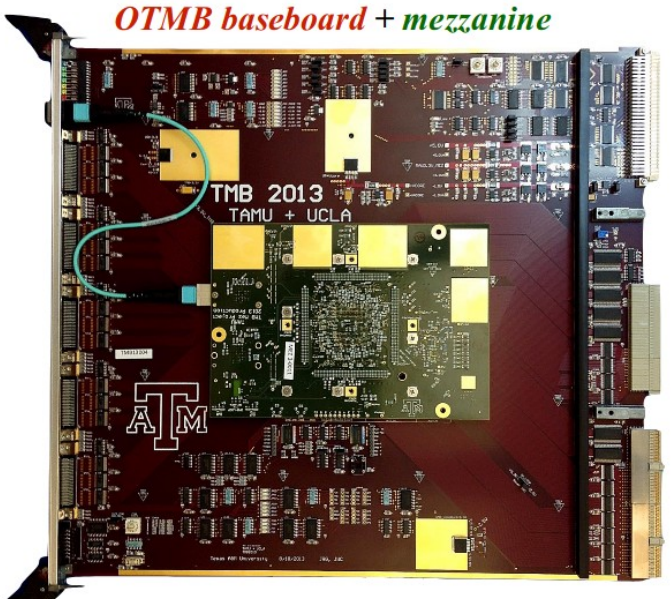
Optical Trigger Motherboard (OTMB)

Trigger Motherboard of inner rings of stations 2,3,4 (ME234/1) need to be upgraded to Optical Trigger Motherboards (OTMBs) to receive trigger data from the DCFEBs by optical fibers instead of copper cable (TMB)

- More powerful FPGA for providing increased algorithmic performance.
- New design will allow receiving trigger primitives from future GEM neighbouring muon system to form CSC+GEM “super-primitives”

  → ongoing developments to:

  - improve position and bending resolution
  - implement GE1/1-ME1/1 trigger
  - extend reach of CSC trigger for high multiplicity signatures from exotic origins



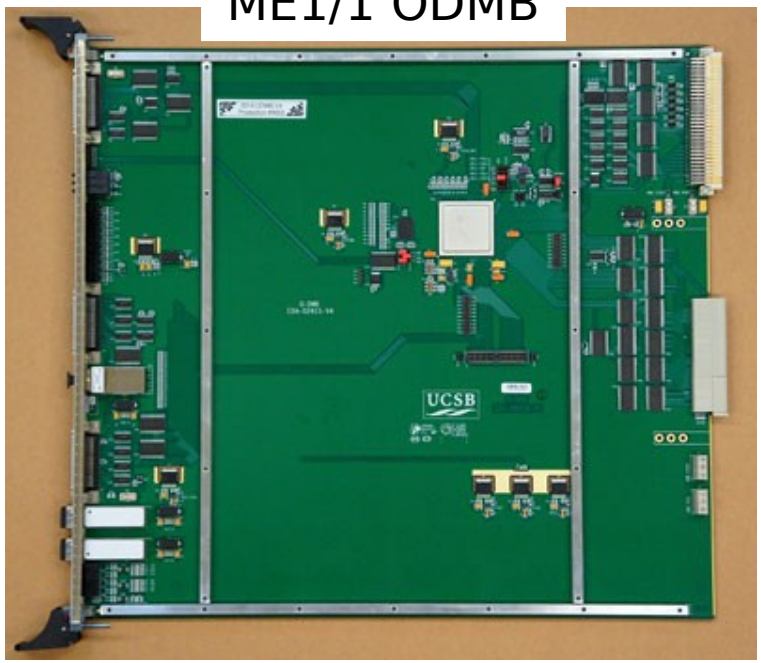
Optical Data Motherboard (ODMB) and backend

Optical Data Motherboard (ODMB) to receive data from DCFEBs through optical fibers and with larger output bandwidth

LS3

- Started designing new boards
  - baseline is ME1/1 ODMB installed in LS1
  - Artix 7 FPGA instead of Virtex 6
- Production planned for 2020-2021

ME1/1 ODMB



Firefly

SEU cross section

$$= \frac{\#\ \text{SEUs}}{\text{Uptime} \times \text{Average flux}}$$

SEU in full HL−LHC lifetime

$$= \frac{\#\ \text{SEUs}}{\text{Uptime} \times \text{Average beam radiation}} \times 1\text{kRad}$$

TDR: "The TIDs for the peripheral crates, situated on the periphery of the detector, are between 0.2 and 0.8 kRad."

Radiation Test Results

Run	DUT	Single fiber SEU	Persistent fiber SEU	Persistent device SEU
1	12 Tx	0	1	4
2	4 Rx Tx	10	1	1
3	12 Tx	2	2	9
4	4 Rx Tx	44	0	1

Used Poisson statistics for errors

With 45 MeV Protons

DUT	Single SEU cross section (cm^2/optic device)	Persistent SEU cross section (cm^2/optic device)	Single SEUs in full HL-LHC lifetime(1 kRad)	Persistent SEUs in full HL-LHC lifetime (1 kRad)
12 Tx	$(8.8 \pm 8.7)\times10^{-12}$	$(7.9 \pm 2.0)\times10^{-11}$	0.05 ± 0.05	0.45 ± 0.11
4 Rx Tx	$(2.2 \pm 0.3)\times10^{-10}$	$(1.2 \pm 0.7)\times10^{-11}$	1.27 ± 0.17	0.07 ± 0.04
12 Rx	$(2.47 \pm 0.3)\times10^{-10}$ (Oct. 31, 2017)		1.41 ± 0.17	

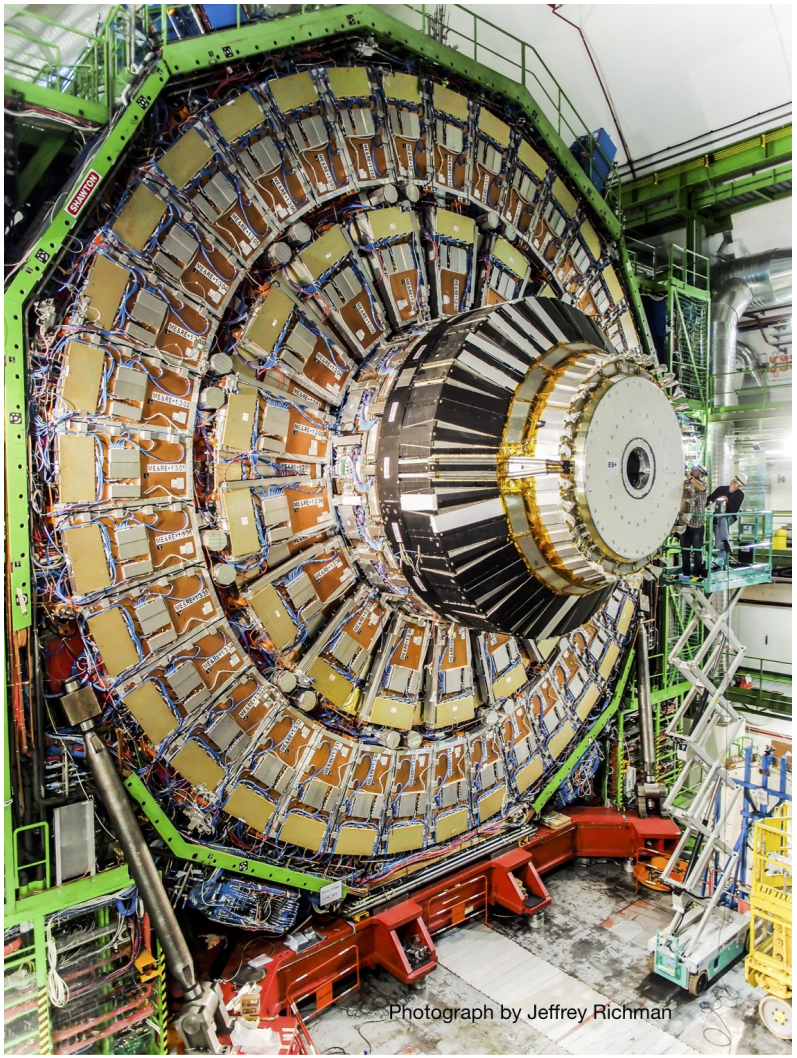
SEU = single SEU + persistent SEU

Optics	# optics	Firefly SEUs in full CSC during HL-LHC lifetime(1 kRad)
12 Tx	72 (ODMB7/5)	36 ± 9
4 Rx Tx	180 (ODMB7/5)	241 ± 32 (2 per month)
12 Rx	360 (ODMB7/5+OTMB)	508 ± 62 (4 per month)

LS2 upgrade: size of the project

LS2 schedule includes 15 months (Mar 2019 – Jun 2020) of continuous work to upgrade electronics of **180 CSCs** (33% of the total CSC system)

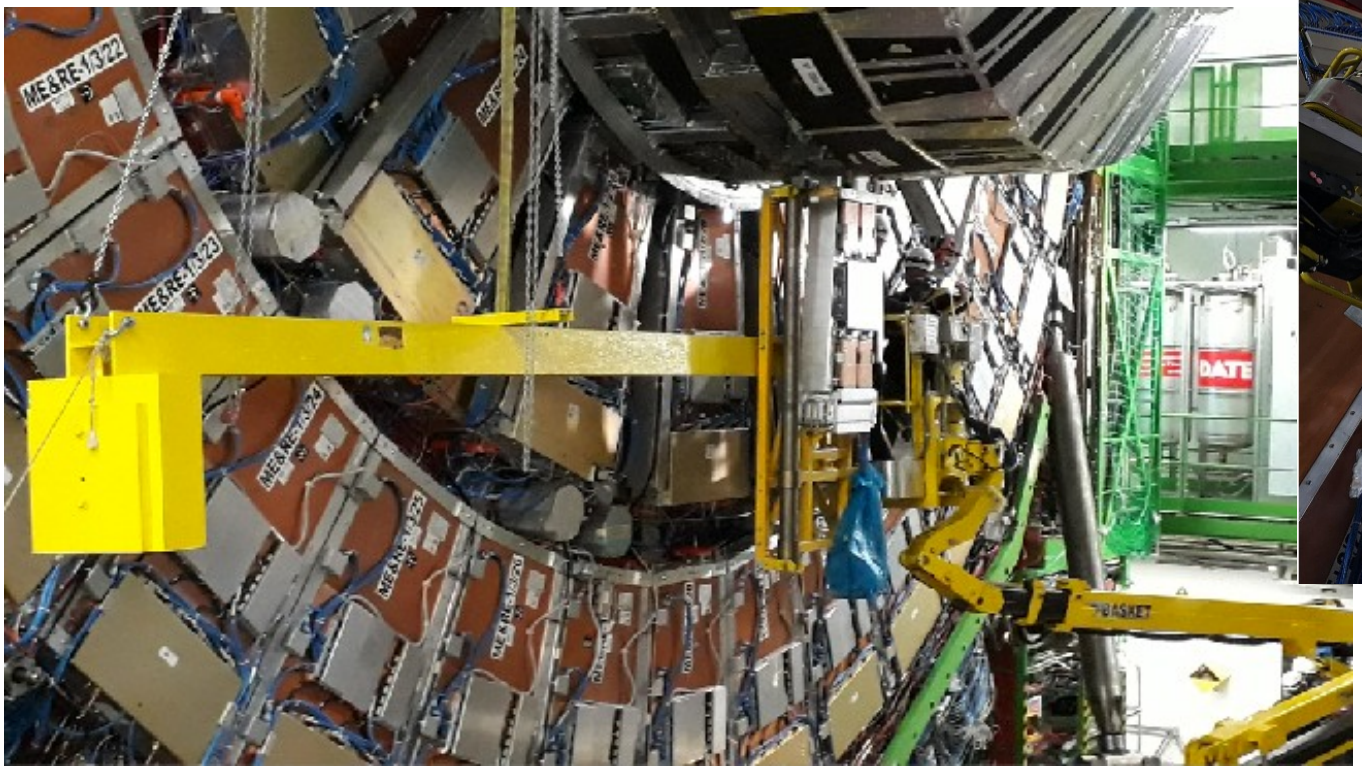
- 504 DCFEBs to replace and refurbish
- 540 CFEBs to replace
- 108 LVDBs to replace
- 468 ALCT mezzanines to replace on extracted chambers and in situ
- 108 TMBs to replace

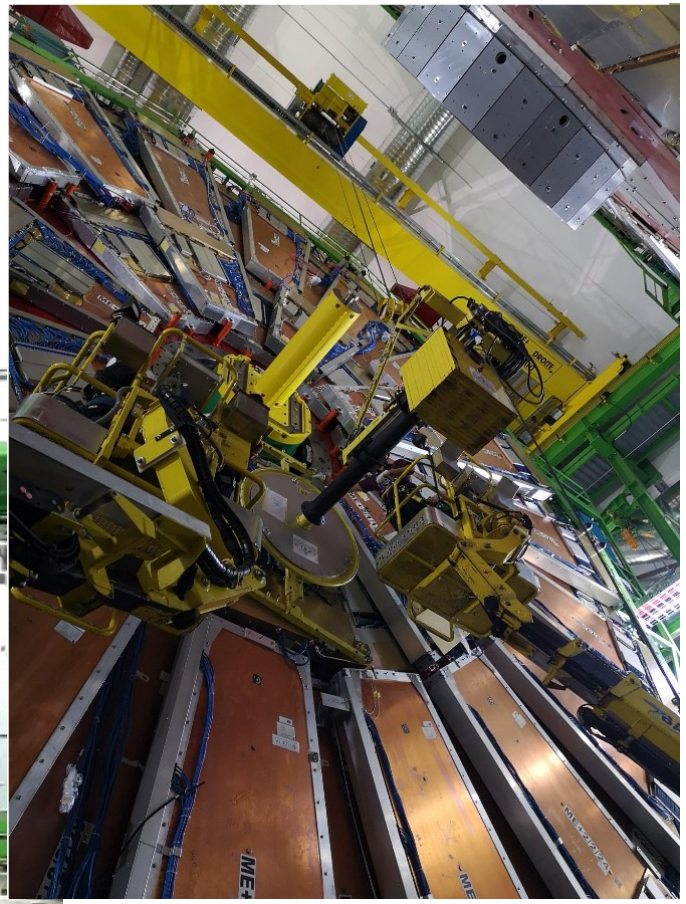


Electronics refurbishment workflow

Chamber extraction (and reinstallation):

CSCs are extracted from the CMS apparatus and transported from underground cavern (-100m) to dedicated lab at the surface





- up to 190 kg / chamber
- up to 1.5 m x 2 m

Electronics refurbishment workflow

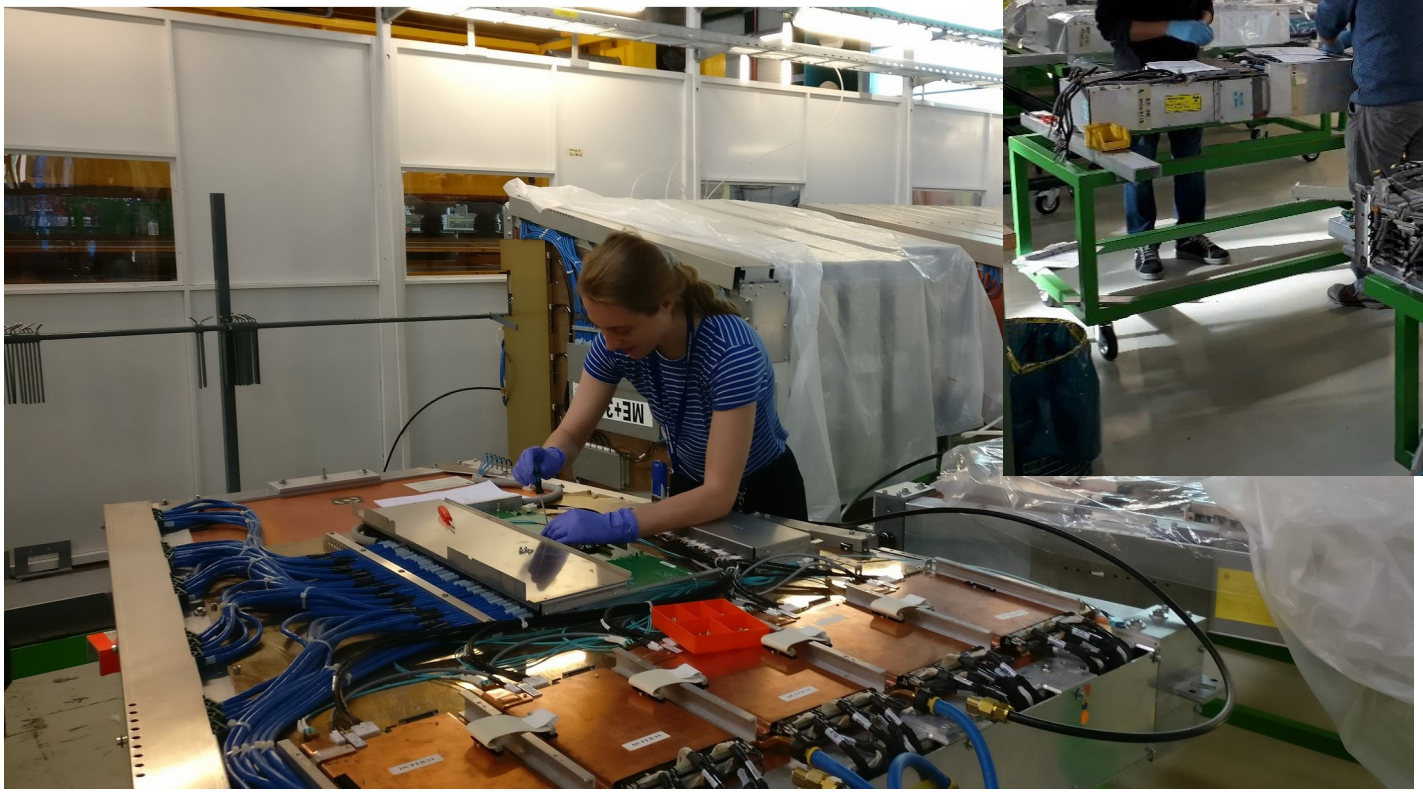
CSC lab:

- storage of chambers
- board replacement
- testing of new electronics

Electronics refurbishment workflow

Electronics replacement:

~ 20 people alternating shifts weekly to refurbish and test the chambers



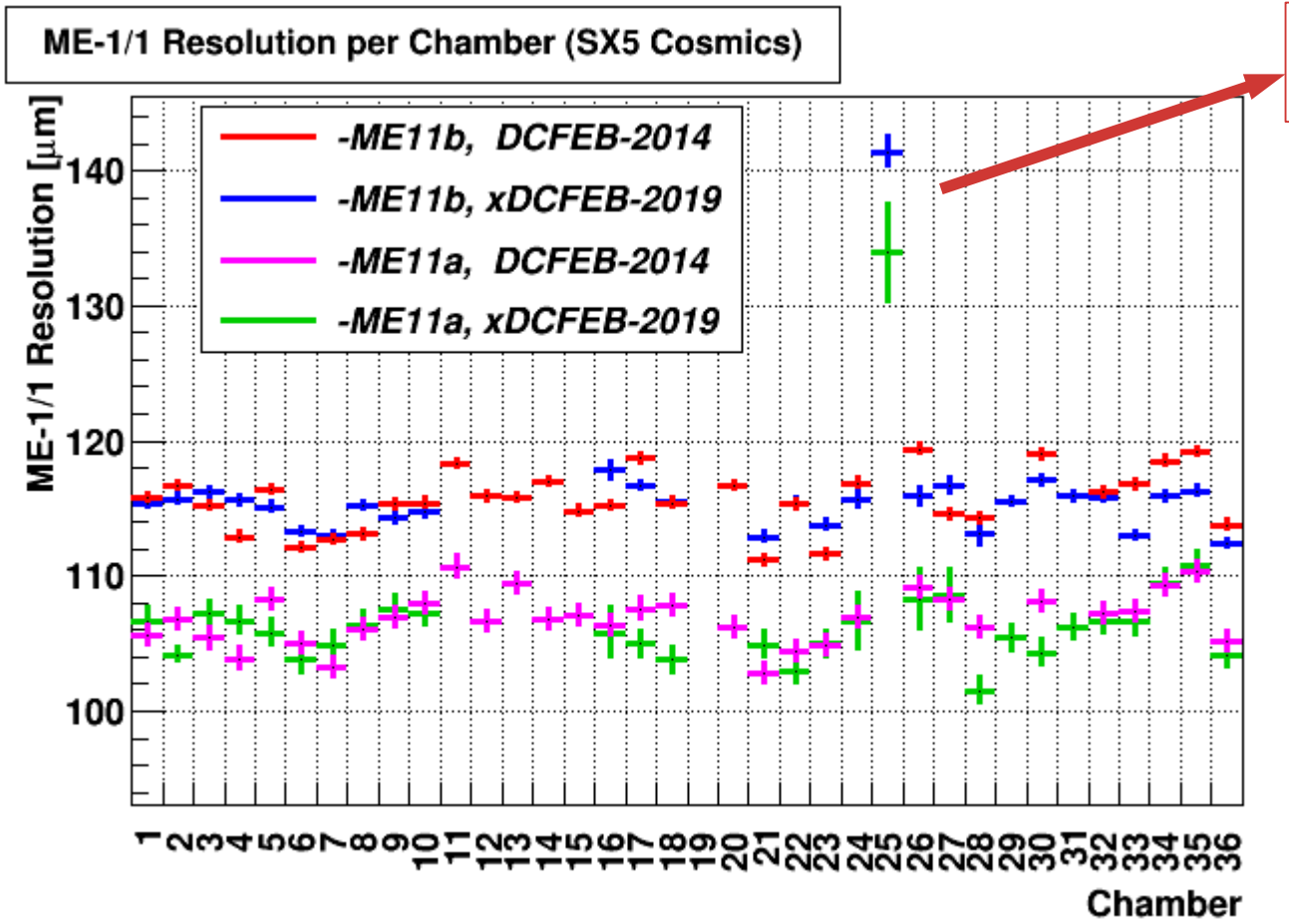
Electronics refurbishment workflow

Refurbishment of electronic boards in a specialized workshop due to the (low) activation of the boards (< 0.1 µSv/h):

- (de)soldering of components
- time-consuming radiation measurements, tracking, transport

Status of the LS2 Upgrade

First part of upgrade finished:
refurbishment of ME-1/1 chambers (DCFEB and ALCT mezzanine replacement)



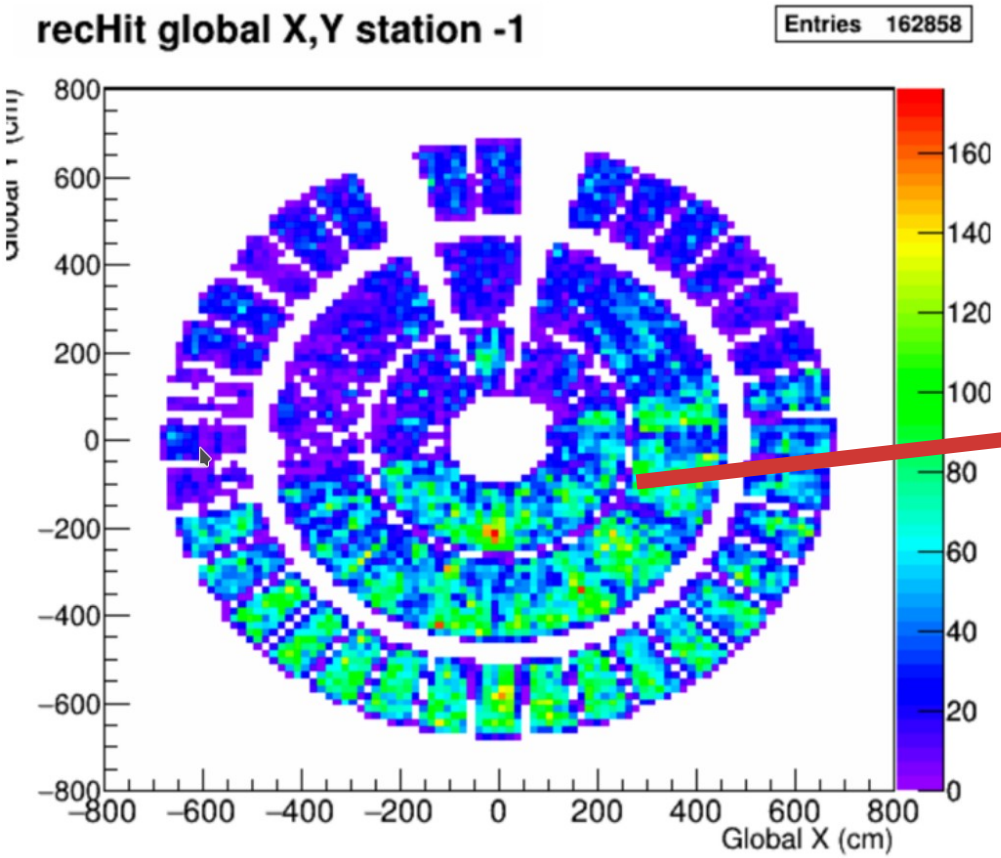
outlier due to lower gas gain at lower HV setting

Performance of ME-1/1 studied using data from cosmic runs taken during testing in lab before re-installation:

- good segment quality (mainly 6-hit segments)
- good spatial resolution, consistent with earlier cosmics data in similar conditions

Status of the LS2 Upgrade

First part of upgrade finished:
refurbishment of ME-1/1 chambers (DCFEB and ALCT mezzanine replacement)



Refurbished chambers successfully participated in a run together with other subdetectors of CMS!

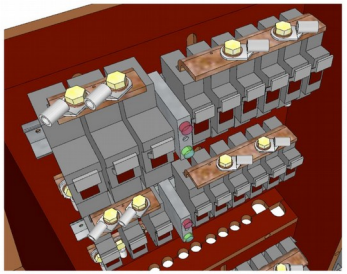
hit occupancy during a cosmic run, triggering on the bottom part of the detector
(most useful to get decent statistics for the central detectors, dedicated runs with top-only triggers are taken as well to illuminate the top chambers)

Services: LV – HV - fibers

Low Voltage system is being upgraded because of increased power requirements of new DCFEBs and ALCTs:

LS2

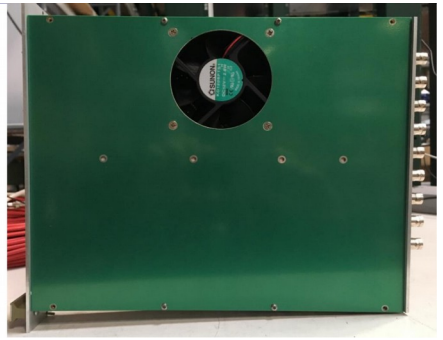
- LV Wiener Maraton system (air cooled)
- upgrade of station 2,3,4 inner rings (first endcap) ongoing



junction box

High Voltage:

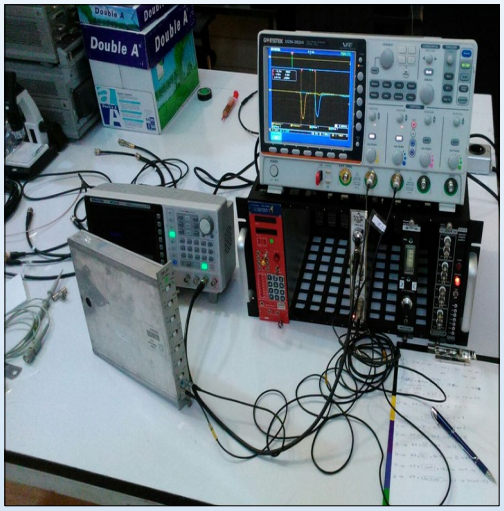
- upgraded to cope with the increased chamber currents expected at HL-LHC fluxes
- station 1 inner ring: replace Caen based system with custom system (with higher current monitoring resolution) as used on other rings to have homogenous system
- tested and ready to be deployed any time



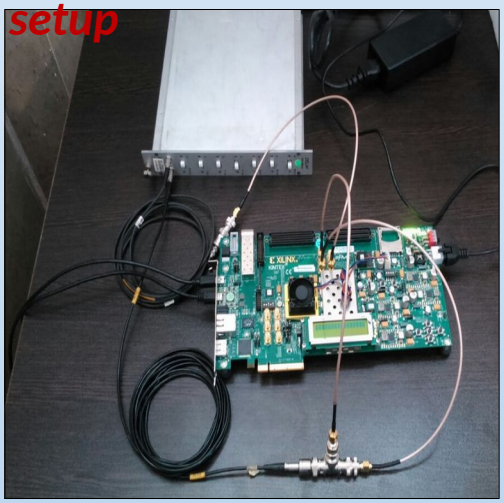
Fibers:

- connecting DCFEBs to OTMB (LS2) and ODBM (LS3)
- ready for installation on station 2,3,4 inner rings (first endcap)

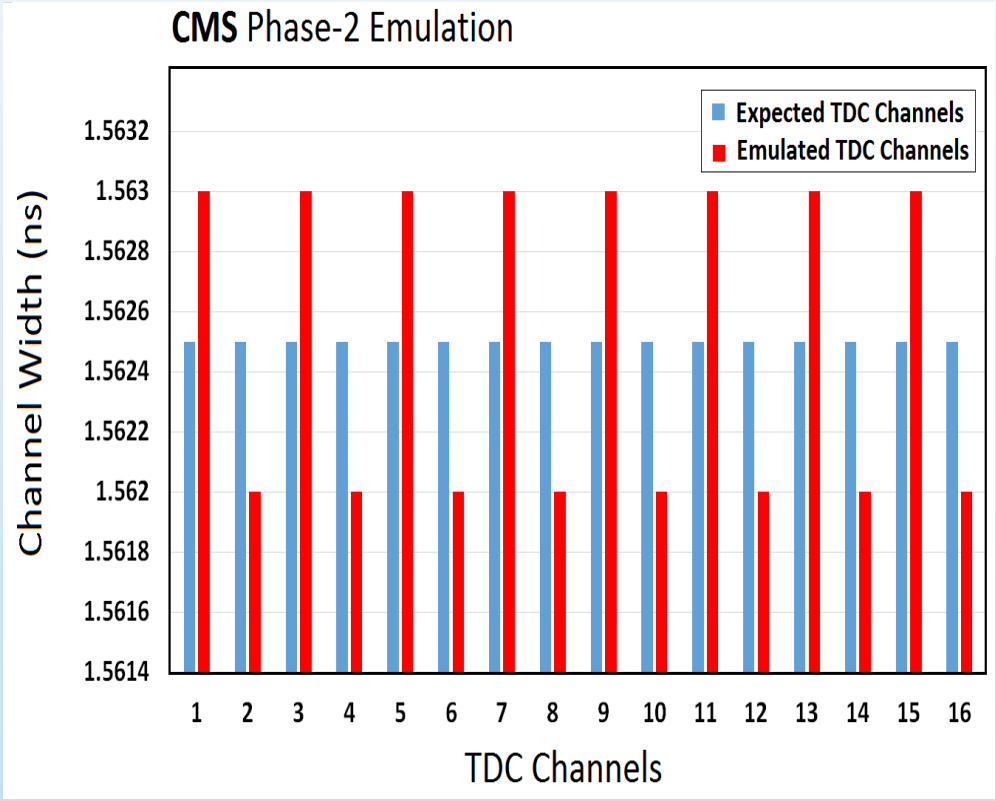
Time to Digital Converter Performance
TDC 1.56 ns @ 160MHz / 640 MSPS



TDC Calibration test setup



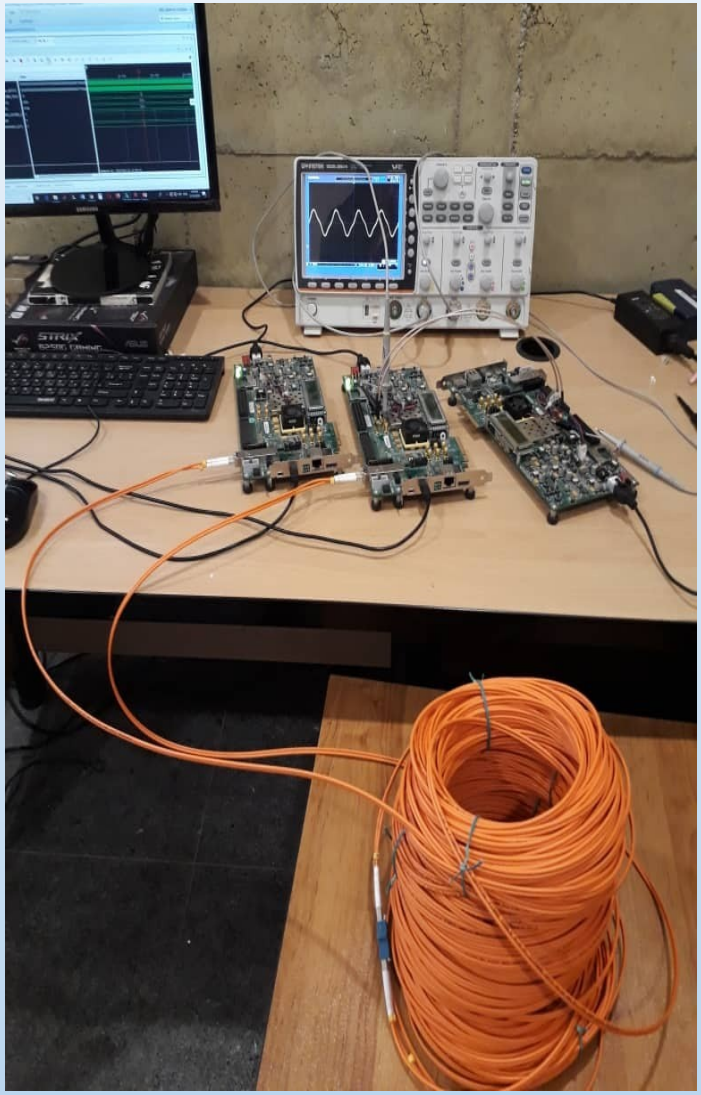
TDC Performance measurement

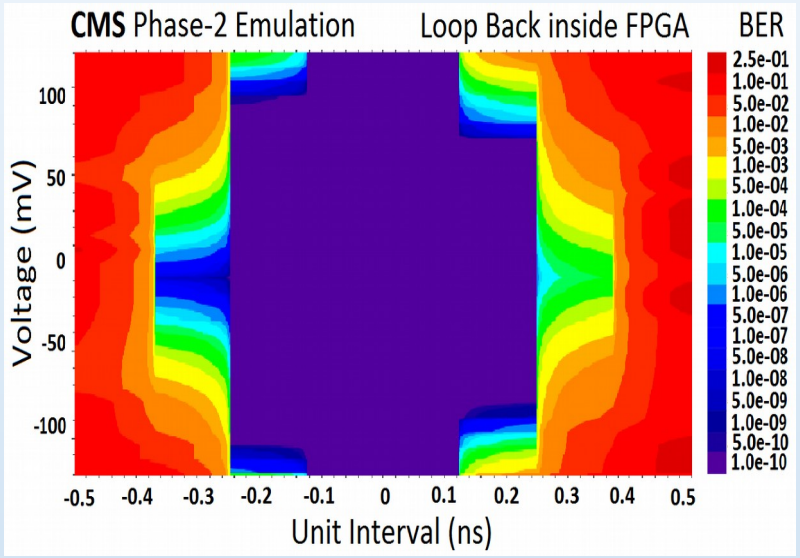


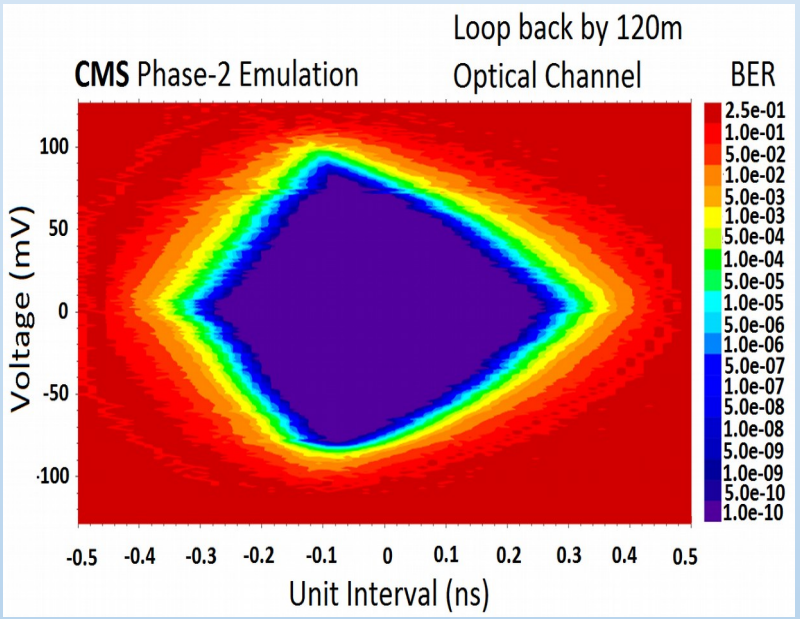
- ISERDES Based TDC
- FREQ. 160 MHz
- Sampling Rare 640 MSPS
- TDC Resolution 1.56 ns

- DNL < ± 0.006 LSB
- INL_{max} < 0.01 LSB

High Speed Data Transmission – Optical Li
Fixed Latency GTX @ 10.24 Gbps



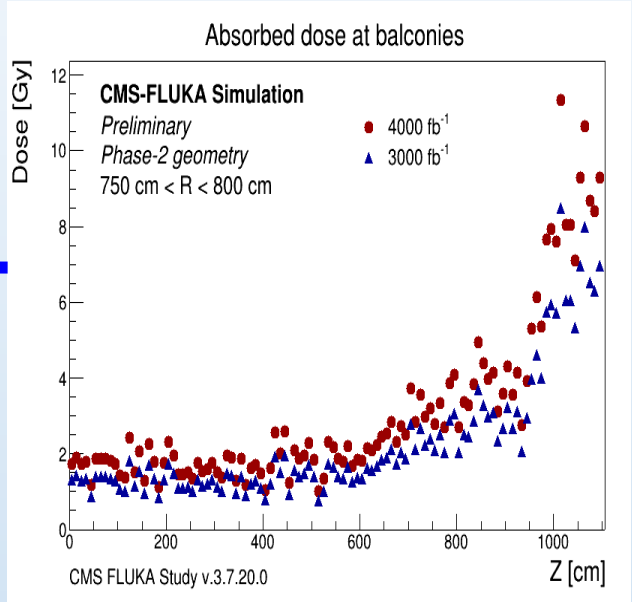




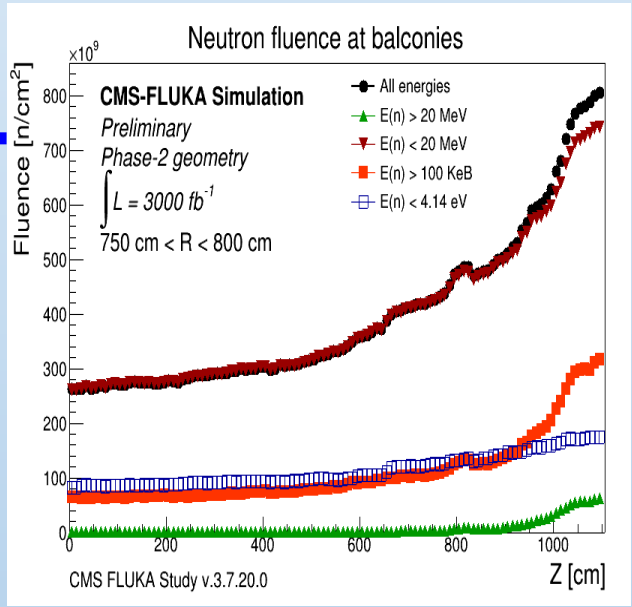
- (**Near-End**) Maximum achievable Opening eye for the Ideal Case (Loop back inside the FPGA1) is 55.56%
- (**Far-End**) Opening eye for the Real Case in which the data transmission will take by connecting two FPGAs through the 120 meters optical channel (OM2) is 50~55%.
- **Test Period is 48 hours and number**

Radiation Consideration

- **The Link system will be installed on the Balcony of CMS (750 cm <R < 800 cm), where the rates are even lower than what we have at the periphery of the detector.**
- **Total Irradiation Dose** is **0.001-10 Gy** @ **3000 fb^{-1}**
- The new Link board components has been chosen from (Commercial-off-the-shelf) COTS which are validated for radiation at the level of **300 Gy**
- The FPGA TID **KINTEX-7 (XC7K160T)** is **3400-4500 Gy**



- **Neutron Flux** at the **CMS Balcony** is **1x10^{4} cm^{-2}s^{-1}** @5 x 10^{34} cm^{-2}s^{-1}
- **Neutron Fluence for 10 HL-LHC years is 1x10^{12} cm^{-2}**
- The Single Event upset (SEU) rate on **configuration memory** is **1 SEU every 413 sec.** and **1 SEU every 1695 sec. at Block RAM**
- **Scrub Time of entire FPGA (SEU detection and Correction) : 13 ms**
- **TMR and Configuration Scrubbing will mitigate the SEUs**

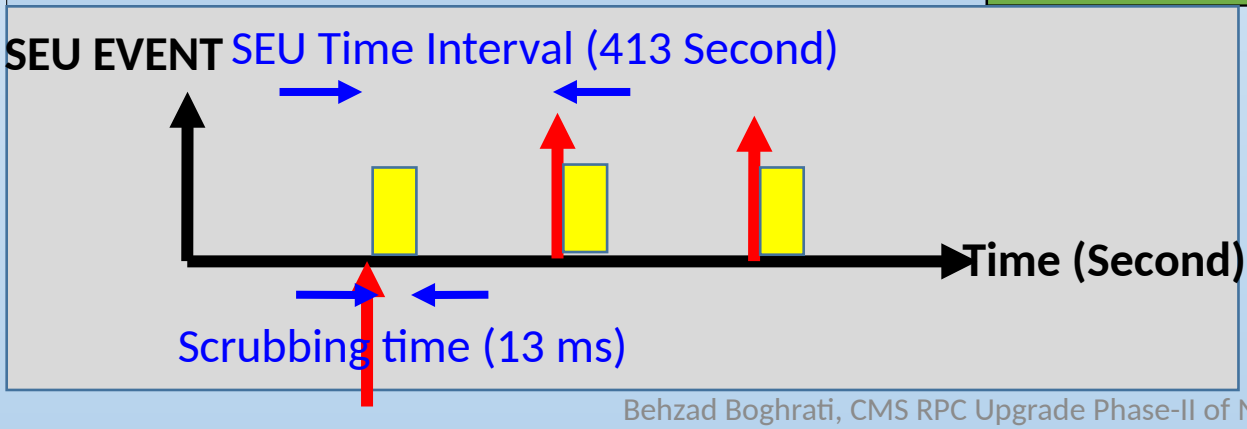


Radiation Consideration

Estimation of SEU on the KINTEX-7 XC7K160T Configuration and BRAM Memories

- *Number of Errors* = σ_{CRAM} × *Flux* × T_{irrd} × N_{CRAM}
- σ_{CRAM} = Cross section of the Single Event upset of each bit at the configuration Memory (cm^2 bit^{-1})
- **Flux** = Number of Neutron pre square centimeter per second
- T_{irrd} = Irradiation Time
- N_{CRAM} = number of bits at the Configuration Memory

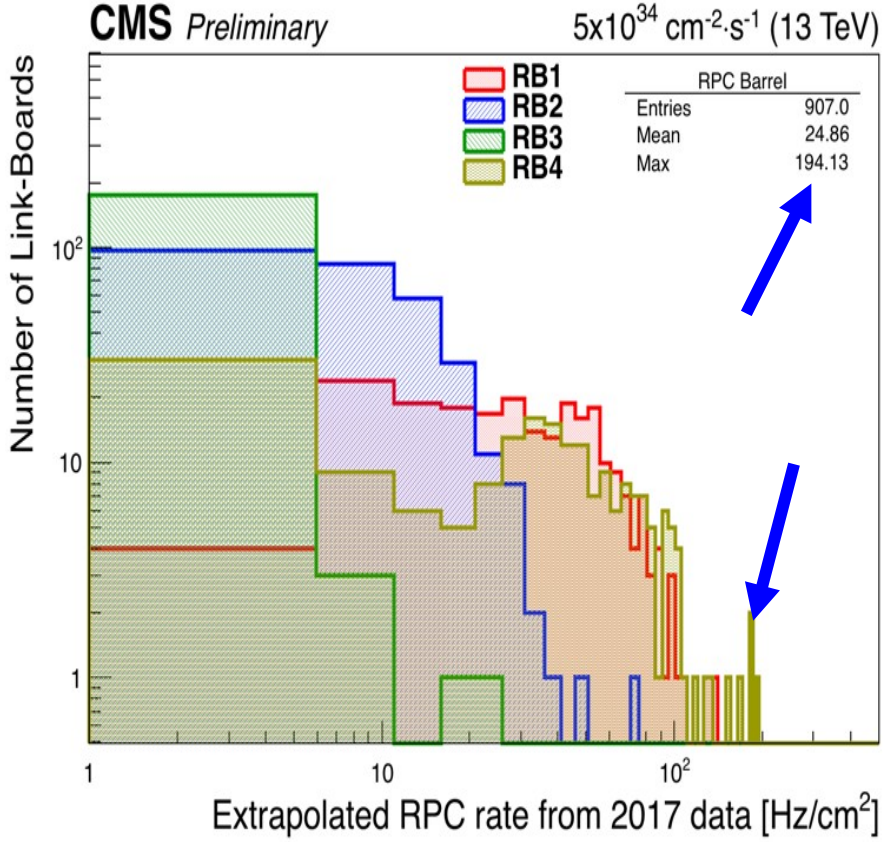
Integrated Errors due to SEU at the Configuration Memory of KINTEX-7 XC7K160T	Integrated Errors due to SEU at the BLOCK RAM Memory of KINTEX-7 XC7K160T
σ_{CRAM} = 4.52 x 10^{-15} cm^2 bit^{-1} Flux = 1 x 10^4 cm^{-2} s^{-1} Time of Exposure = 1 sec N_{CRAM} = 53,540,576 bits	σ_{BRAM} = 5.07 x 10^{-15} cm^2 bit^{-1} Flux = 1 x 10^4 cm^{-2} s^{-1} Time of Exposure = 1 sec N_{BRAM} = 11,700,000 bits
E_{CRAM} = 0.00242 at 1 second E_{CRAM} = 0.1452 at 1 minute E_{CRAM} = 8.712 at 1 hour	E_{BRAM} = 0.00059 at 1 second E_{BRAM} = 0.036 at 1 minute E_{BRAM} = 2.135 at 1 hour
1 SEU every 413 seconds	1 SEU every 1694 seconds



SEU Time Interval >> Scrubbing time

Hit Rate wrt Max expected Background Rate at HL-LHC

- Expected Max hit rate in Barrel/Endcap in HL-LHC , safety factor 3: 600 cm^{-2} s^{-1}
- Biggest Strip surface area : 120 X 3 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per bx : 600 x (120 x 3) x 96 x 25 X 10^{-9}= 0.52 hit /LB x bx
- One Master Link Board collects hits of two adjacent Slave Link boards
- Max Single hit in one MLB per bx : 0.52 x 3 = 1.56 hit /LB x bx
- Size of hit information Package : 15 bits (Yellow box)
- MLB Max. Payload: 15 bits x 1.56 hits x 40 MHz = 0.936 Gbps
- *We foresee to send 232 bits/BX (for physics, already removed EOD and checksums) between MLB and RPC backend.*
- Maximum limit of single hits in one MLB = (one frame -



Items	Header + FEC	Number of Events (1... 14)	No. Strip (1..96)	Sub-bx	LB No. (0 ... 8)	BCN	BC0	Partition	ID
Bit	24	4	7	4	4	12	1	3	2

New Slow Controller Functions

- **Downlink,** data direction from new Slow Controller to Control boards:
  - Number Links : 216 Downlinks (96 links Endcap CBs + 120 links Barrel CBs)
  - Link Protocol: LpGBT Protocol
  - Data Rate: 10.24/5.12/2.56 Gbps (All of this speeds are acceptable)
  - Fast trigger, Broadcast commands :
    - BC0, EC0, L1A, Hard Reset
  - TTC clocks (40.078 MHz)
  - Slow control Commands
    1. FEB Threshold setting (received from RPC online software)
    2. TTC fine skew adjustment (received from RPC online software)
    3. Open/Closed windows setting (received from RPC online software)
    4. FPGA configuration file (Remote Programming) (received from RPC online software)

- **Uplink,** data direction from Control boards to the new Slow Controller:
  - RPC strip hit Histogram
    - Counting Hits on every RPC strip
  - Timing Histograms
    - Counting Hits on all RPC strips in each Bunch Cross
  - Link System Status
    - Voltages, current, Temperature
    - Faults, SEU
    - Firmware Version Control

RE34/1: FEB v2

- Board Schematic and Layout is finished
  (Time Schedule is respected)
- Schematic has been transmitted to external experts
- Verification phase until end of May
- **Waiting for quotation**
  - **PCB manufacturing.**
  - **Components procurement**
  - **Board mounting.**

all rad hard components are delivered