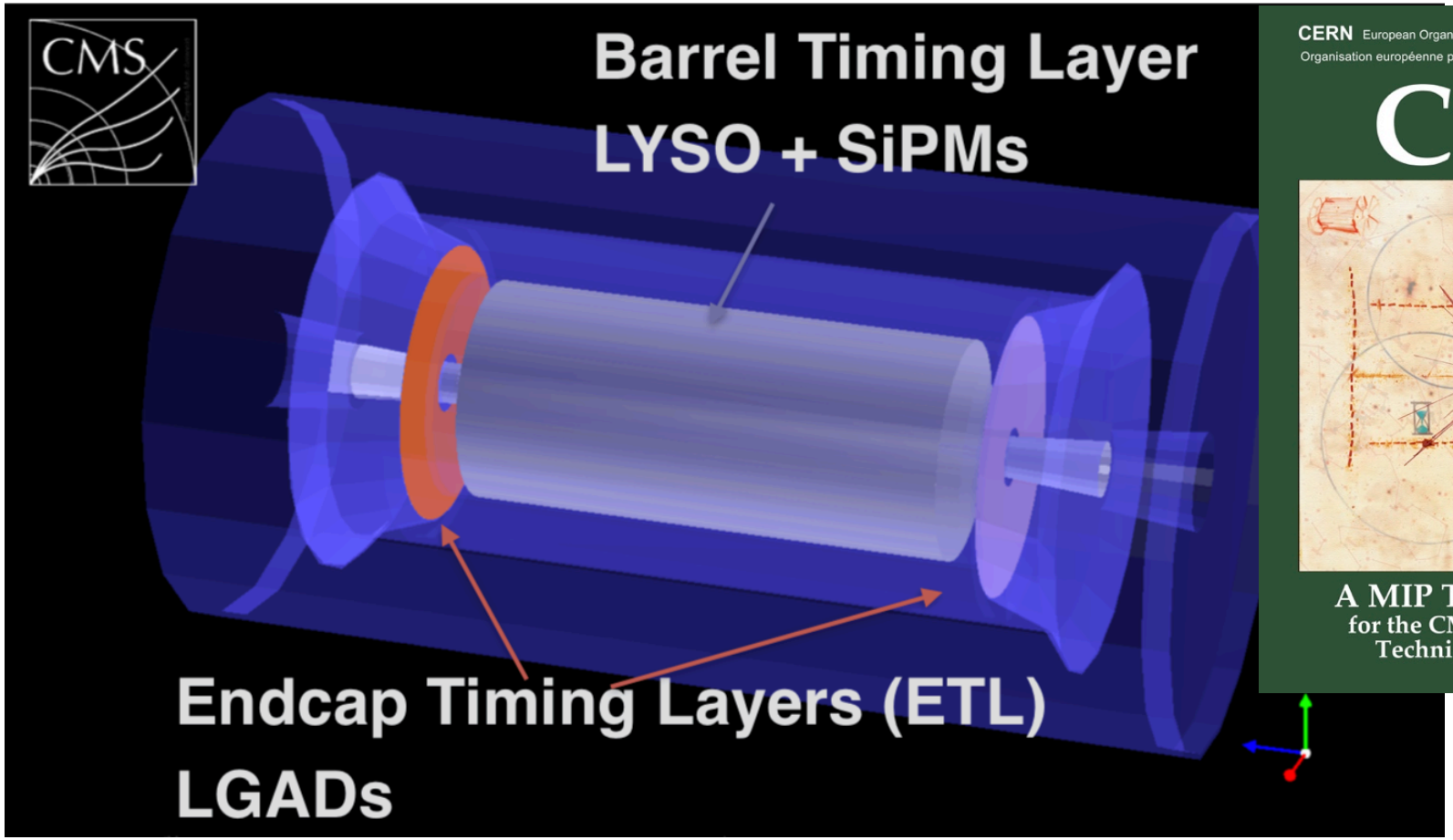
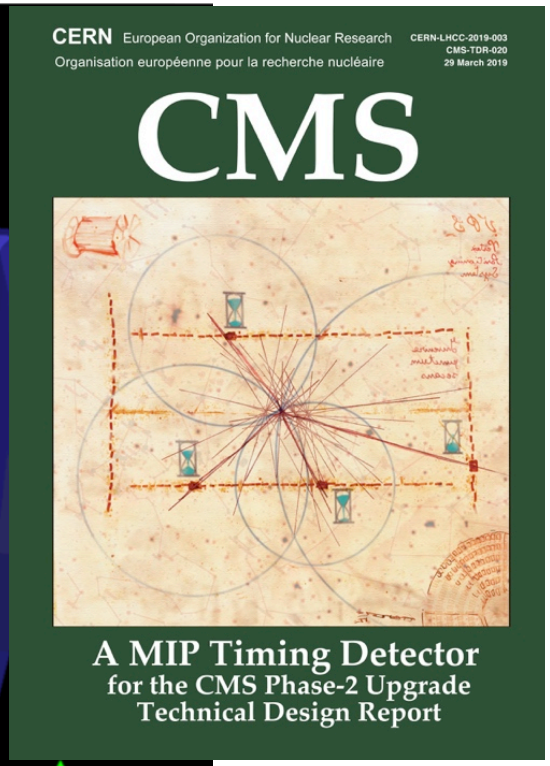
CMS Timing Detector (MTD) Electronics

Ted Liu, Fermilab

On behalf of the MTD collaboration





First generation precision timing detectors → challenging front-end electronics

- Thin layers between tracker and calorimeters (BTL single layer, ETL double)
- with ***~30-40 ps per track*** resolution at HL-LHC start, & < ***60 ps*** at 3000 fb^{-1}

BTL precision timing *challenges*

- **LYSO with dual-end SiPM readout**
  - Basic unit: 1x16 array of crystals (~ 3 x 3 x 57 mm^3)
  - $|\eta|<1.45$, surface ~38 m^2; 332k channels
  - Nominal fluence: *1.9x10^{14} n_{eq}/cm^2* (3000 fb^{-1})
  - *Single layer*
- **Huge MIP signal size**
  - Signal: 10k - 6k photoelectrons; + SiPM gain: 4 - 1.5 10^5
  - *Peaking time ~20 ns, LYSO decay time constant ~40 ns*
  - timing is given by the arrival of the first photoelectrons (20-100 p.e. depending on DCR) – *2 per mil of the signal matters*
- ***Dark count rate (DCR) and out-of-time pileup***

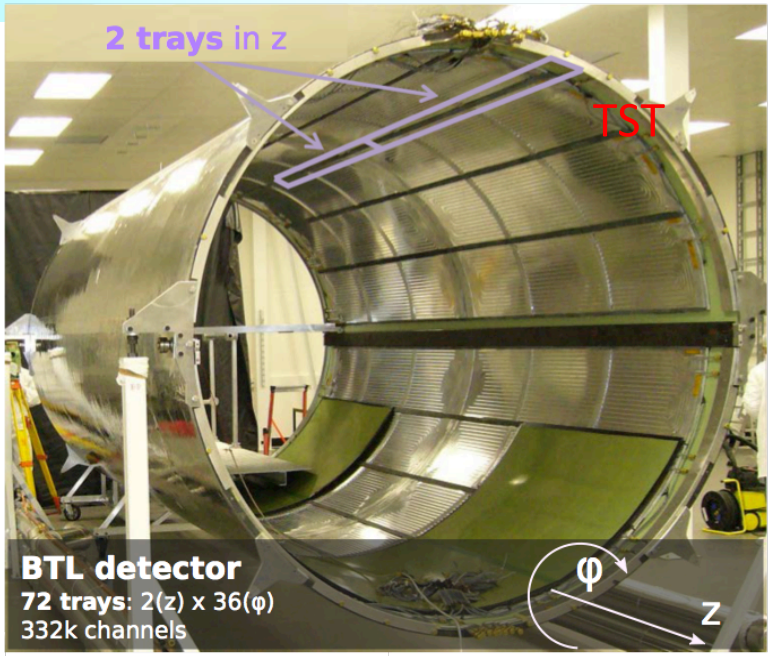
  noise is dominated by SiPM dark counts,

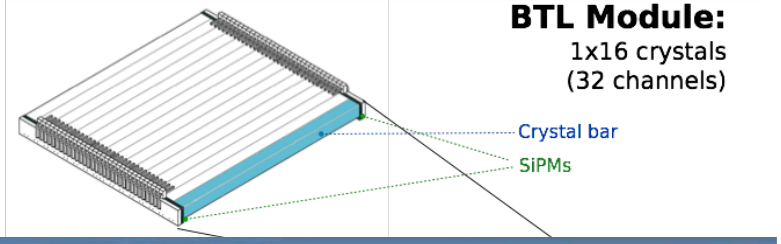
  out-of-time pileup → baseline fluctuations.

  Due to radiation along BTL lifetime, SiPM

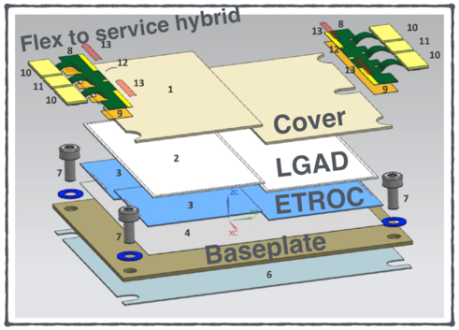
  DCR rate grows from 1 MHz to 55 GHz

The need for DCR cancellation at front-end

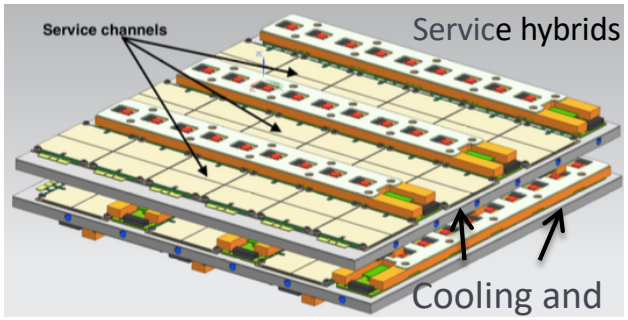


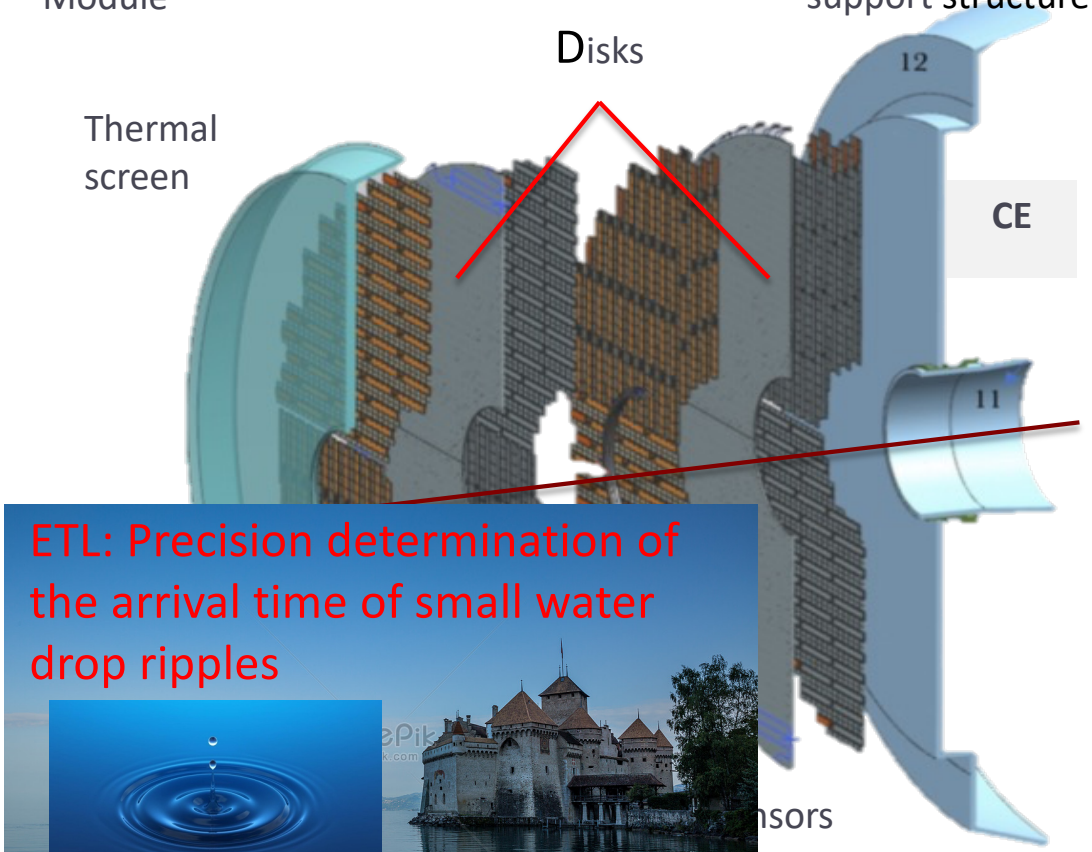


ETL precision timing *challenges*



Module



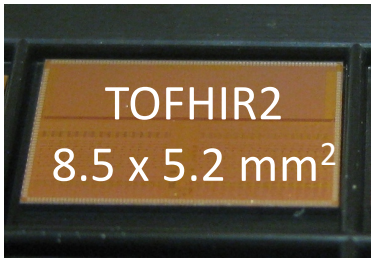


- Low Gain Avalanche Detectors (LGADs)
  - Basic unit: Module (4x6 cm^2)
    - 2x4 cm^2 LGAD bump-bonded to 2 ETROC ASICs mounted on two sides of cooling plates
  - Two layers/disks per endcap mounted on the HGC nose (~2 hits per track)
  - $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~8.5 M channels
  - Nominal fluence: ***1.6×10^{15} n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - Landau contribution: ~ 30-40ps
  - Front-end contribution kept < ~40ps
- ***Extract precision timing from small LGAD signal (~6fC) at end of operation***
  With low power: < 4mW/channel

BTL TOFHIR: Time Of Flight at HIgh Rate

Challenges:

- ***minimize impact of DCR noise and pileup on time resolution***
- cope with very high rate (2.5 MHz MIP + 5 MHz low E hits per channel)
- handle the dynamic range variation along detector lifetime
- 15mW/channel



Received on
5th May, 2020

- Timing measurements

Leading edge, electronics jitter < 20 ps

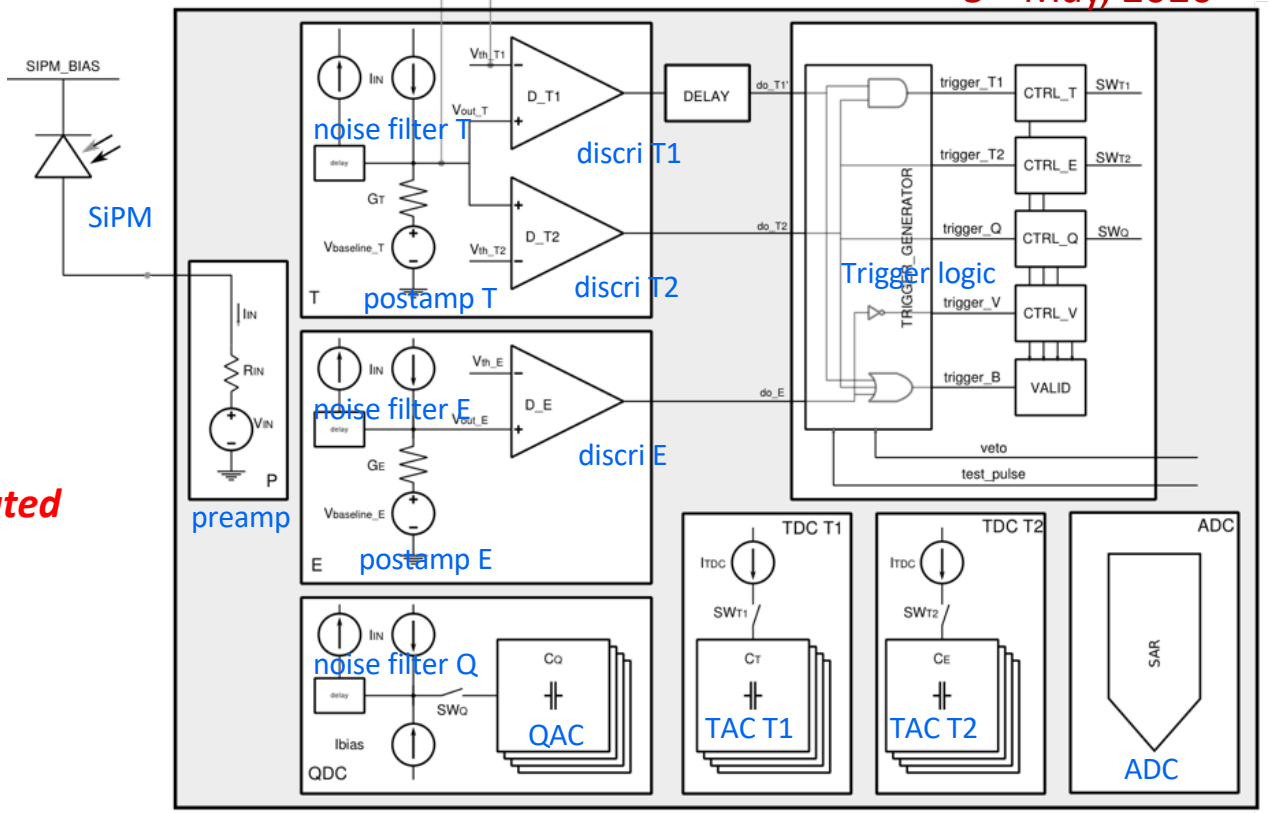
- Amplitude measurement

Charge integration and ToT/Slew Rate
Accuracy 2% for time walk correction

- ***DCR cancellation***

noise and baseline fluctuation are mitigated by a dedicated pulse filtering circuit.

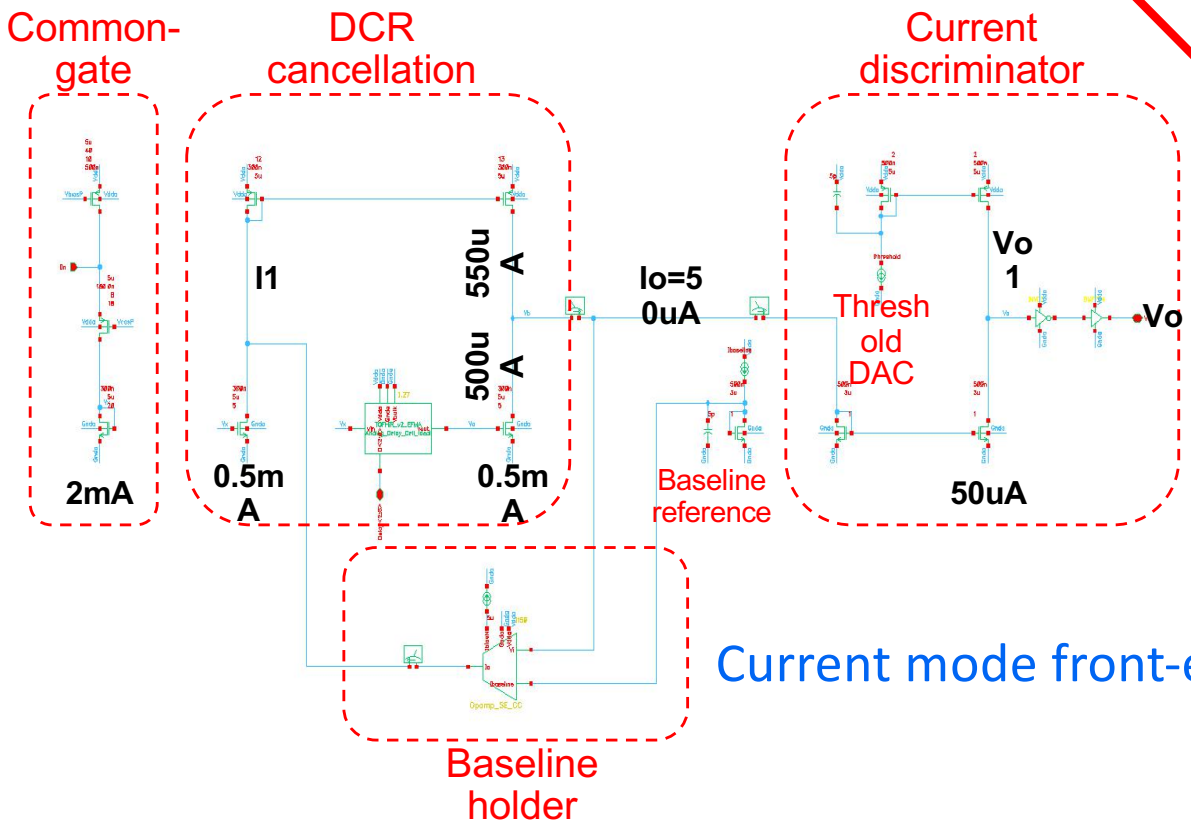
TOFHIR2 channel



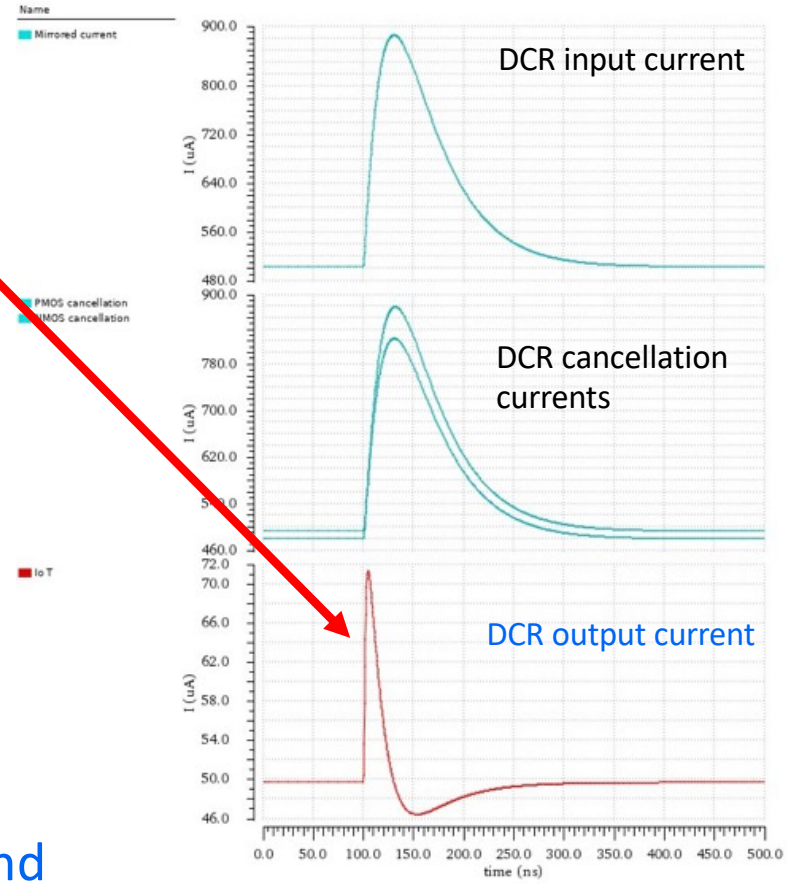
*) SAR ADC 40 MHz provided by Krakow group

TOFHIR2 DCR cancellation

- Inverted and delayed pulse added to the original pulse
- Delay line is approximated by a RC net, programmable 0.2-0.5ns
- Short output pulse (< 25 ns)
- *Noise and baseline fluctuations are mitigated*



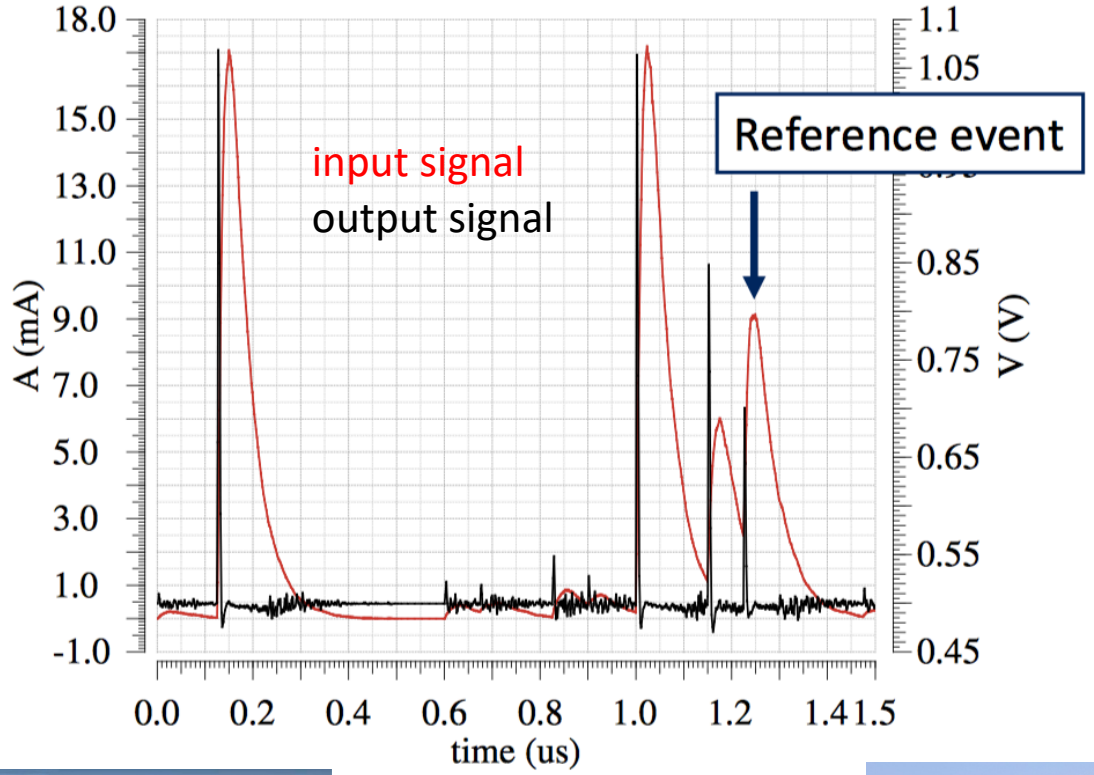
Current mode front-end

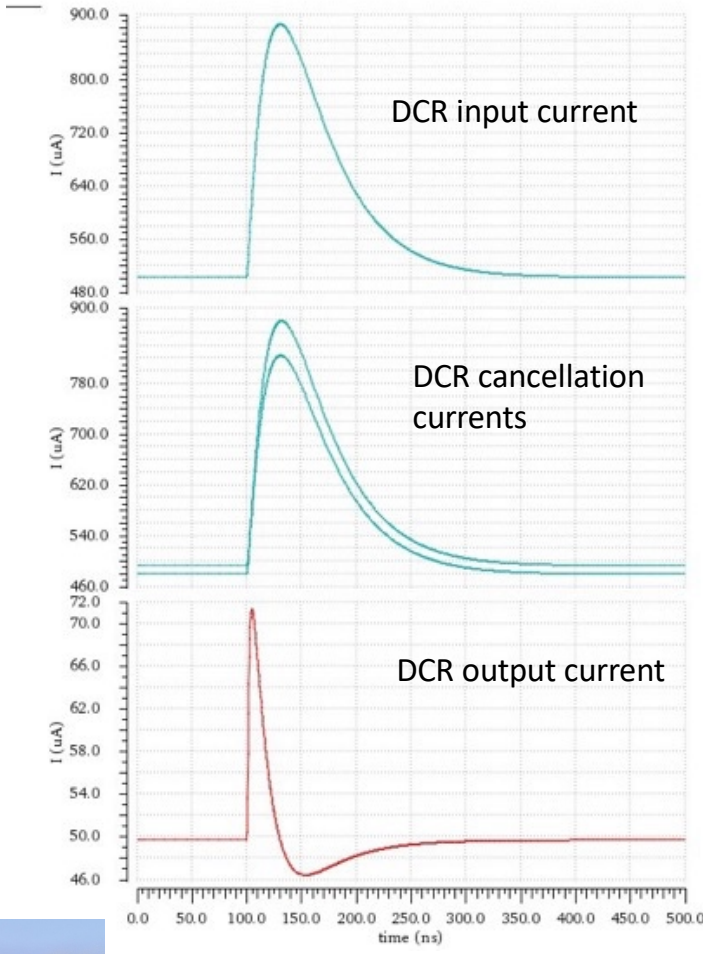


The effect of DCR cancellation

Noise and baseline fluctuations are mitigated

- at the highest DCR the time resolution is improved by a factor 3.5



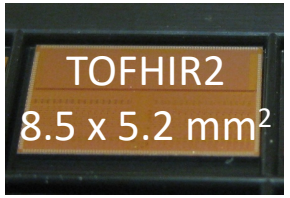


DCR cancellation →

Sharper waves, well separated in time…

TOFHIR versions

- TOFHIR1 (UMC 110 nm): Available, ***and enables system level testing***
- TOFHIR2 (TSMC 130 nm): Chips received in May 2020



TOFHIR2:

- New technology
- New frontend design
- DCR noise filter
- Radiation tolerance
- Faster ADC
- Higher rate capability
- L0 trigger capable
- Internal reference voltages
- Less sensitive to process variations

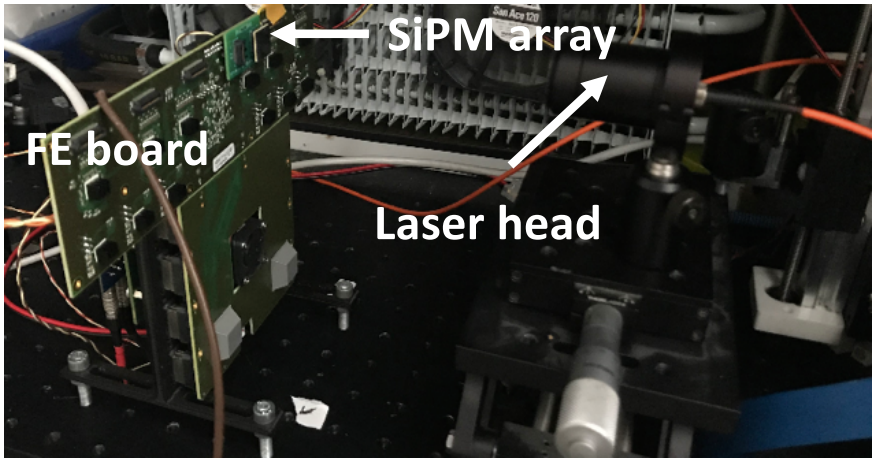
	TOFHIR1	TOFHIR2	
Number of channels	16	32	←
Technology	CMOS 110 nm	CMOS 130 nm	←
Voltage supply	1.2 V, 2.5 V	1.2 V	
Reference voltages	External	Internal	←
Radiation tolerance	No	Yes	←
DCR noise filter	No	Yes	←
Number of analog buffers	4	8	←
TDC bin (ps)	20	20	
10-bit SAR ADC (MHz) *)	10	40	←
Compatibility with lpGBT	Yes	Yes	
I/O links	LVDS	CLPS	
L1, L0 Trigger	Yes, No	Yes, Yes	
Maximum MIP rate/ch (MHz)	1	2.5	←
Max low E rate/ch (MHz)	3	5	←
Clock frequency (MHz)	160	160	

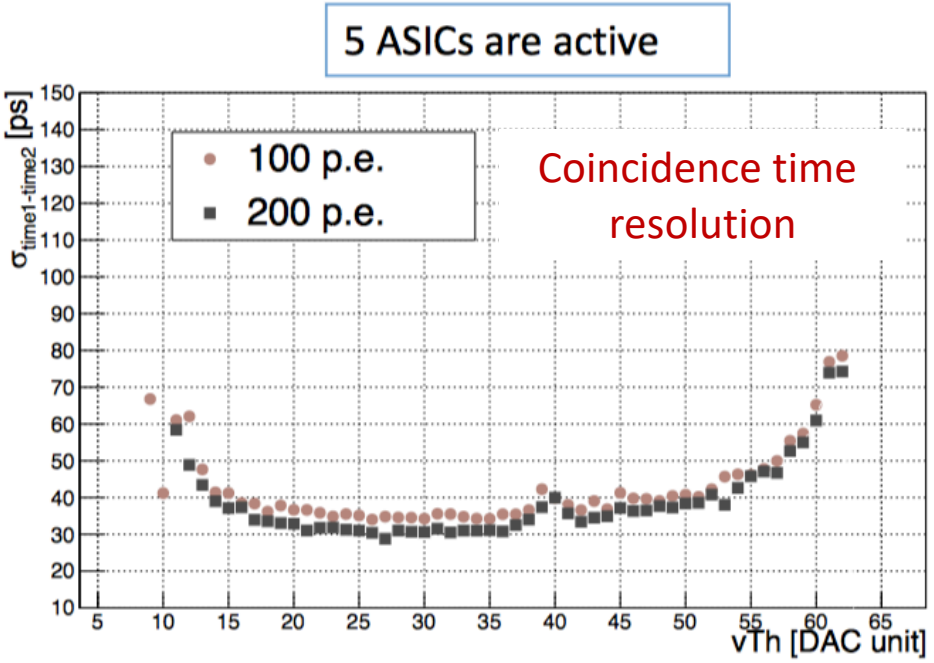
*) SAR ADC 40 MHz provided by Krakow group

Measurements with TOFHIR1

- FE board with 6 TOFHIR1 chips
- Picosecond laser
- SiPM array S13361-3050AE
- Measured coincidence time resolution between channels
- Single channel time resolution with laser pulse of 200 p.e. is 21 ps.
  - Same slew rate as 8000 pe LYSO
  - Adding the contribution of photo-statistics we expect a time resolution of 31 ps with LYSO

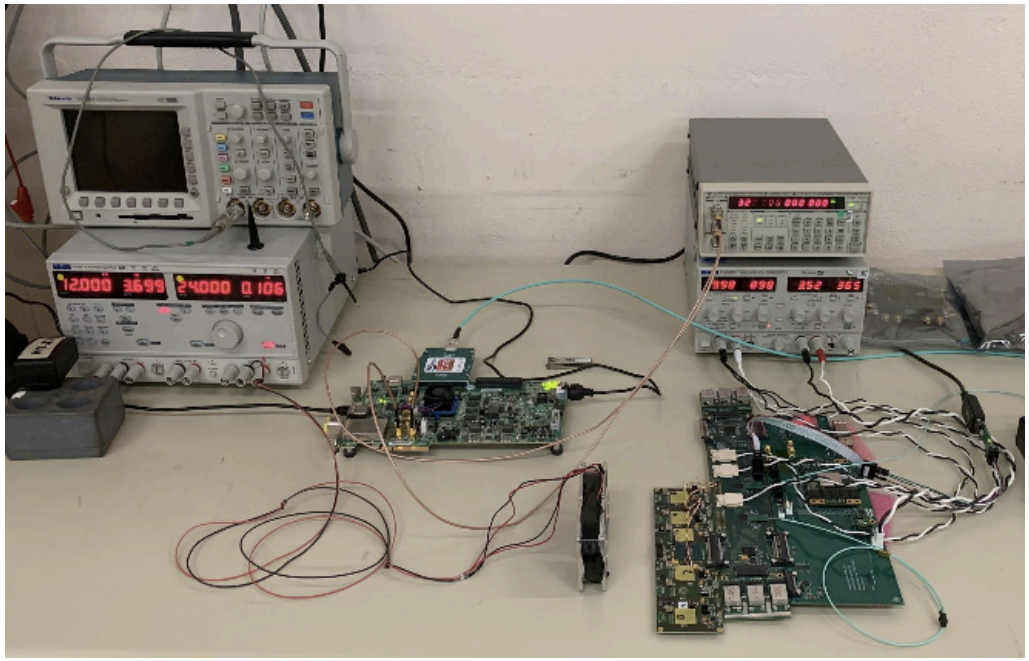
TOFHIR1 has already enabled system level testing

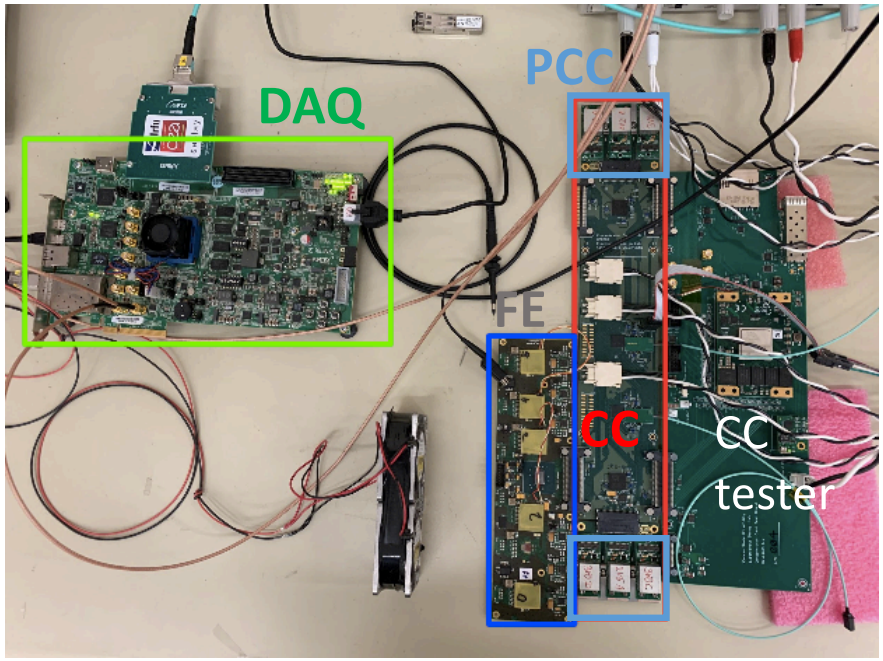




Readout Unit prototype 1

- The RUproto1 integrates Frontend board (FE), Concentrator Card (CC), and Power Converter Card (PCC)
- ***Integration of RUproto1 with backend DAQ*** is being carried-out at CERN
  - Configuration and data readout of test data via lpGBT/VTRX+ was achieved
  - Communication with GBT-SCAs and temp monitoring were achieved
  - Tests with sensors were postponed due to COVID-19



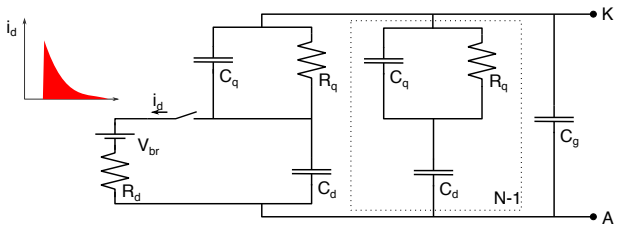


Expected time resolution TOFHIR2

Simulation conditions

	BoL	EoL
LYSO pulse	**9500 p.e.**	**6000 p.e.**
SiPM gain	3.8 10^5	1.5 10^5
SiPM jitter	100 ps	100 ps
SiPM cross-talk	14%	3%
TDC digitization	20 ps	20 ps

SiPM model



C_d	14.6 fF
C_q	1 fF
C_{grid}	36 pF
R_q	500 kΩ
R_d	1kΩ
N_{cells}	40,000

Time resolution at discriminator output

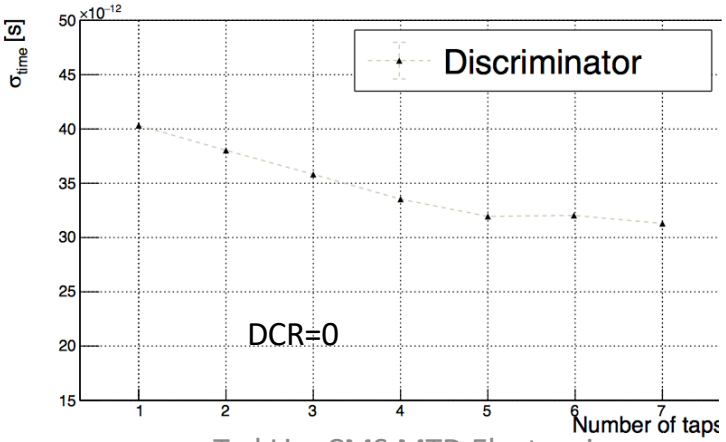
- LYSO photo-statistics included
- TDC digitization added
- Clock jitter 15 ps

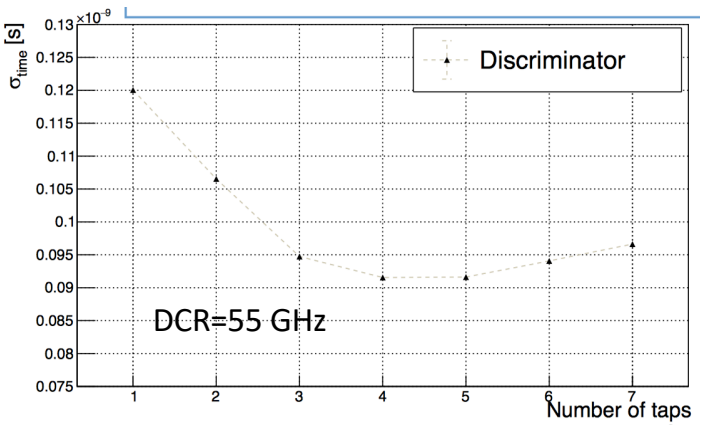
LYSO double readout

DCR (GHz)	0	30	40	60
σ_t (ps)	25	55	60	68

DCR at 3000 fb^{-1} for different scenarios of operating and annealing temperatures under study.

σ_t (ps) single-ended readout LYSO bar





ETROC: ETL ReadOut Chip

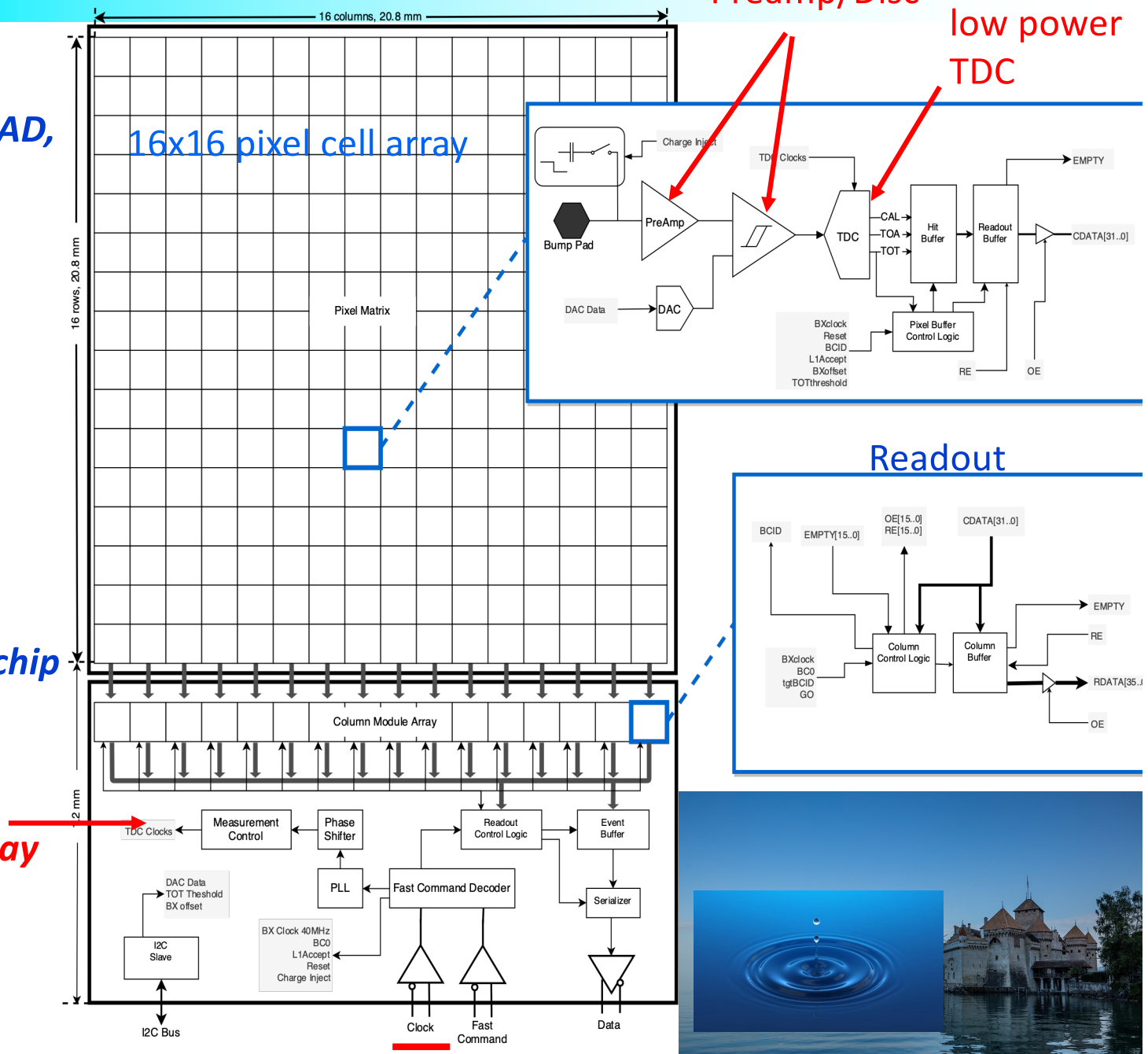
ETROC bump-bonded to LGAD,
To handle 16x16 pixels
Each 1.3 mm x 1.3 mm

Requirement:
ASIC contribution to
time resolution < ~40ps

Deal with small signal size
(~6fC, at end of operation)

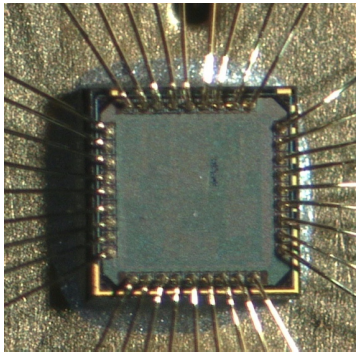
Power consumption < 1W/chip
L1 buffer latency: 12.5 us

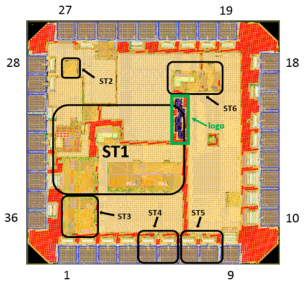
65nm
clock distribution all the way
into each pixel



From ETROC0 to ETROC1 to ETROC2

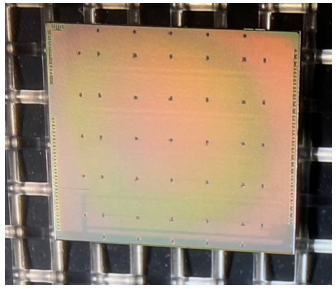
Design team: FNAL/SMU in collaboration with lpGBT team

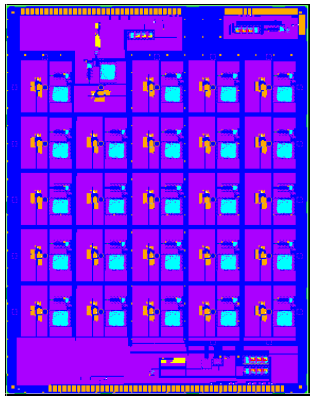




ETROC0

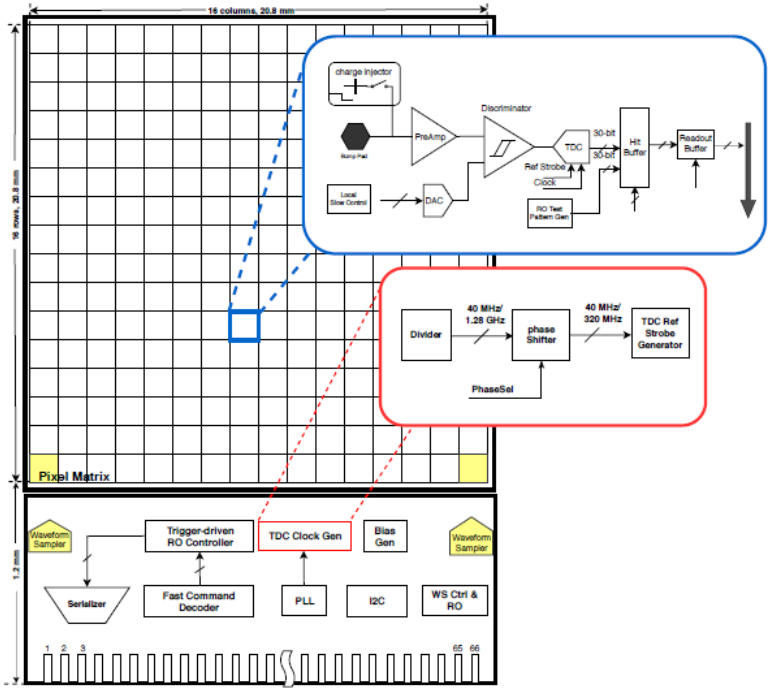
- ***Submitted in Dec. 2018***
- Analog Front-end
- Tests by far confirmed functionality
- First round beam test early 2020





ETROC1

- ***Submitted in Aug. 2019***
- 4 X 4 pixel array with full front-end including TDC
- Chips received middle Dec 2019
- TDC block works well
- Single pixel full chain testing on going (slowed down by COVID 19), and followed by 4x4 array testing



ETROC2

- ***Aim to submit in Q1 2021***
- Designed to be compatible with 16 X 16 pixel array with *full functionalities*

ETROC3

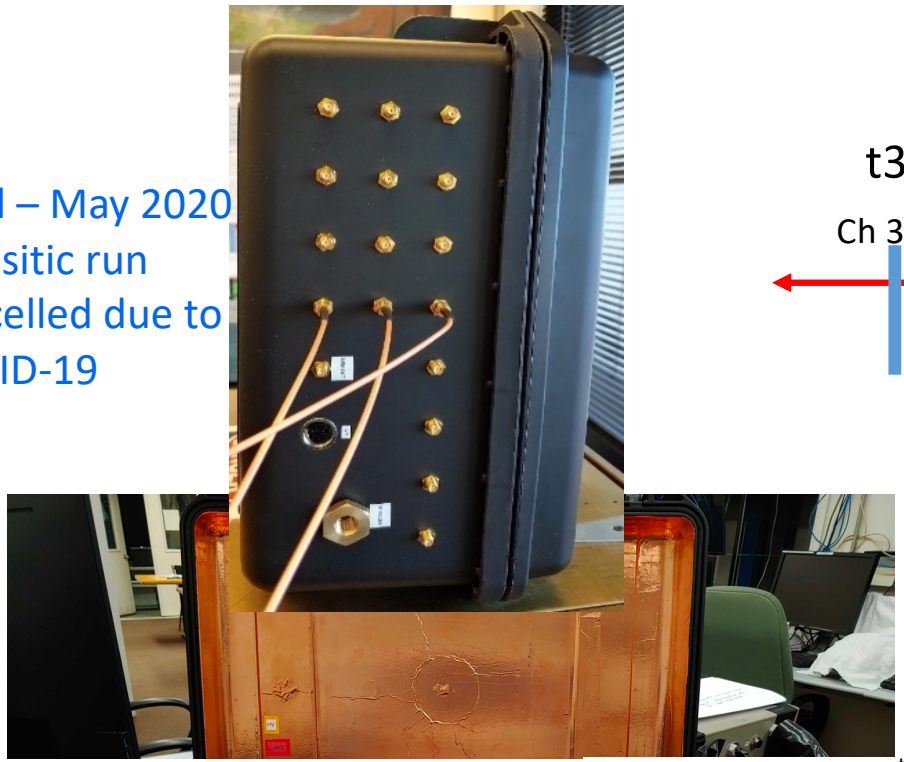
- Aim to submit in Q1 2022
- Pre-production version

A simple Beam Telescope (with 3 HPK-ETROC0 boards)

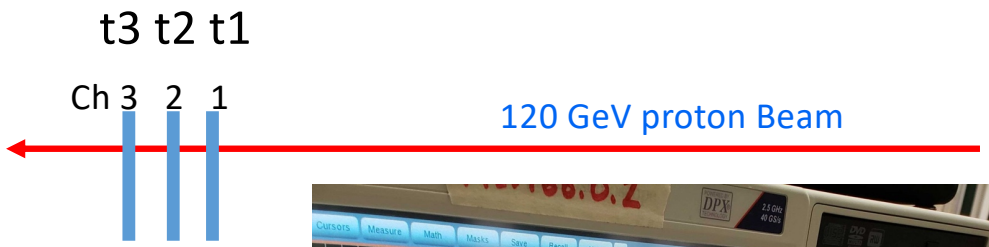
Jan-Feb 2020

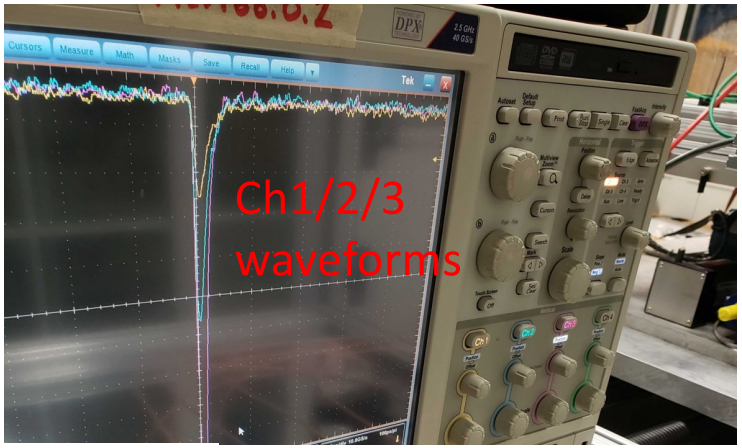
Simple "suitcase" setup in parasitic mode running at FNAL MTest

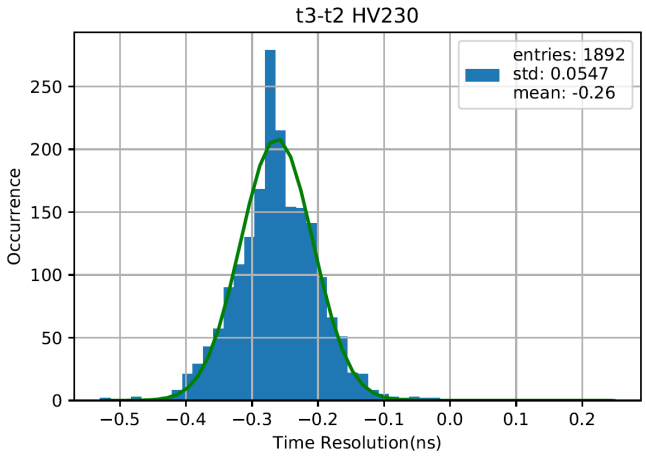
April – May 2020 parasitic run cancelled due to COVID-19

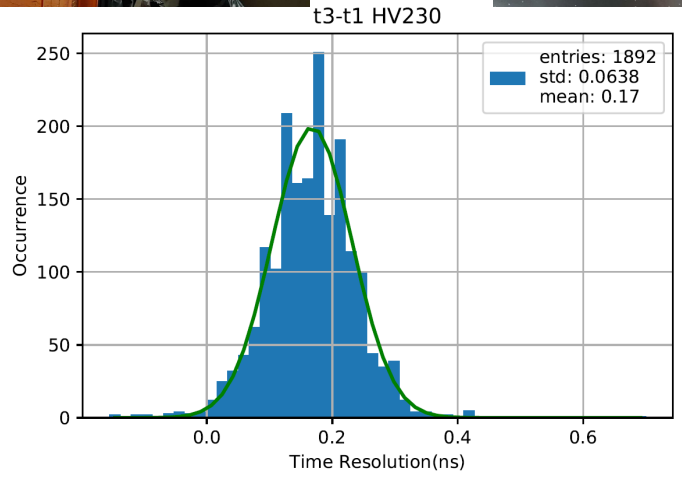


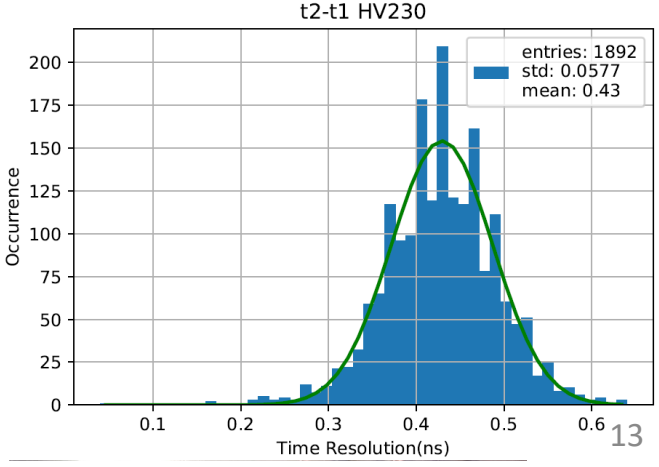
$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx 33\ (ps)$$

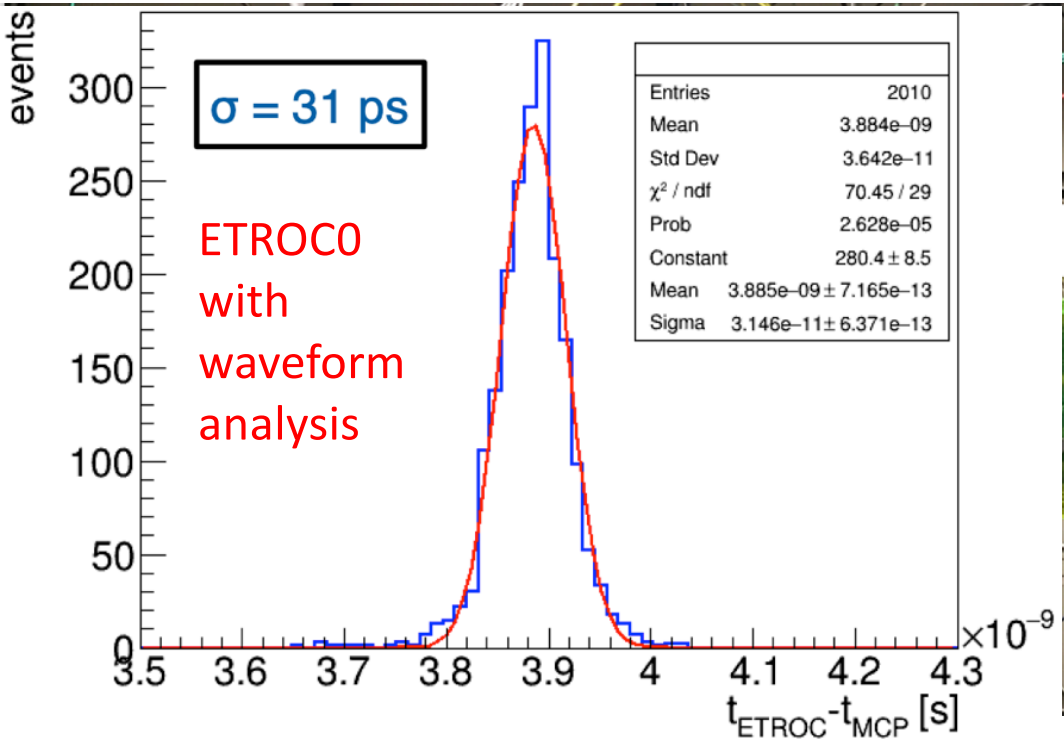


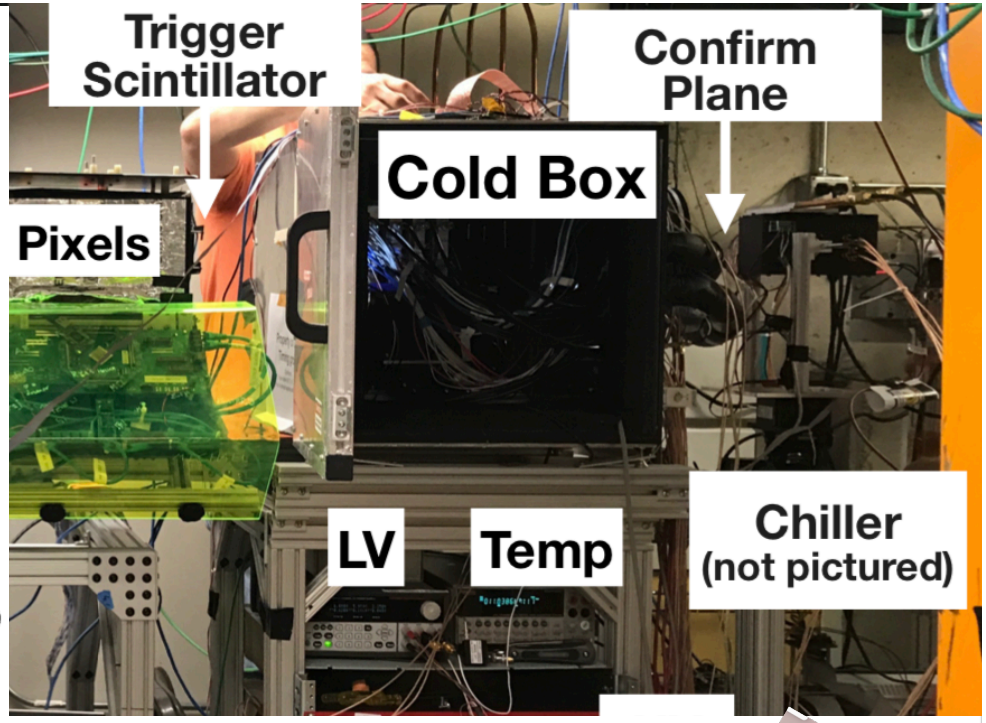


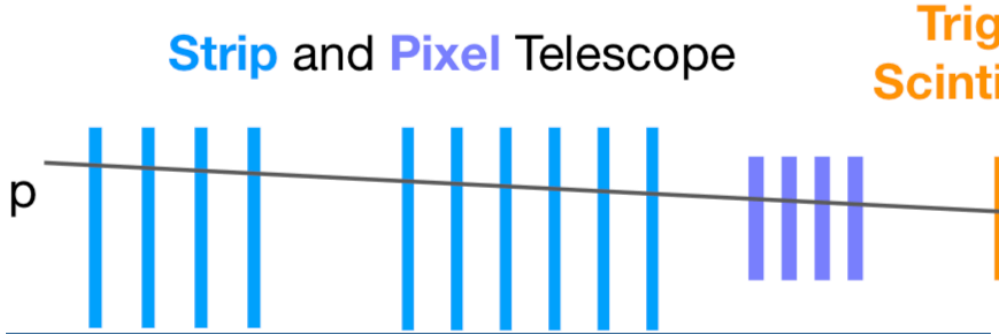


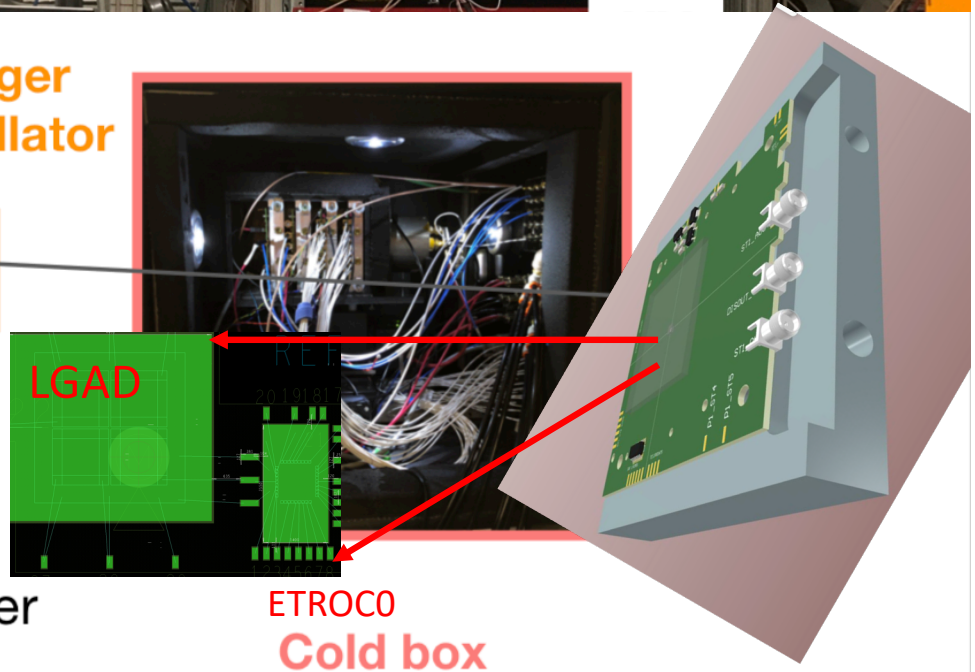












HPK-ETROC0 testing with ***full tracking***

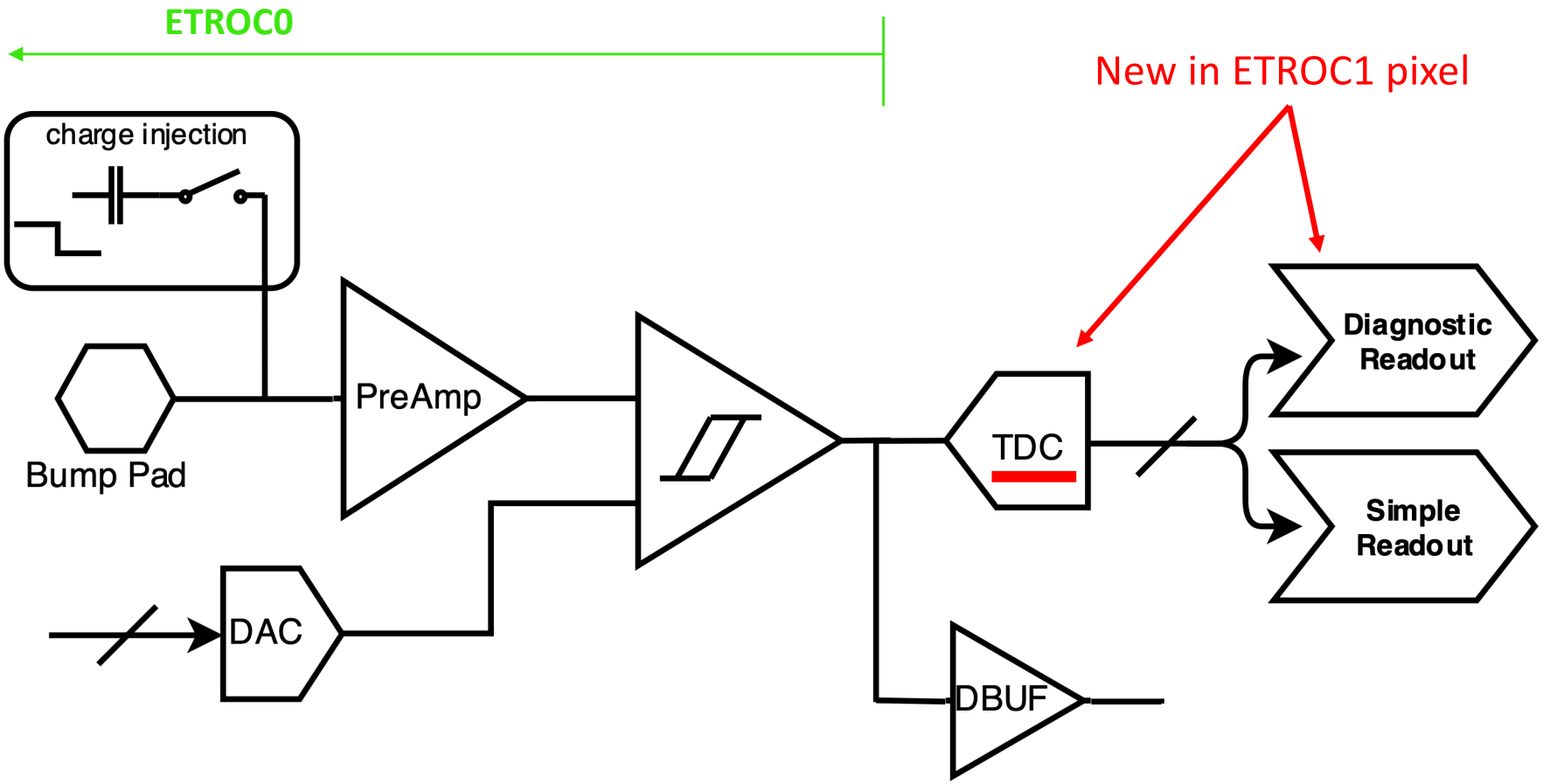
- MTD Beam Test Setup at FNAL MTest
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves waveforms
  - Study Δt(LGAD,MCP)

LGAD boards on cooling blocks

MCP (Photek) time reference

ETROC1 pixel: uses ETROC0 front-end

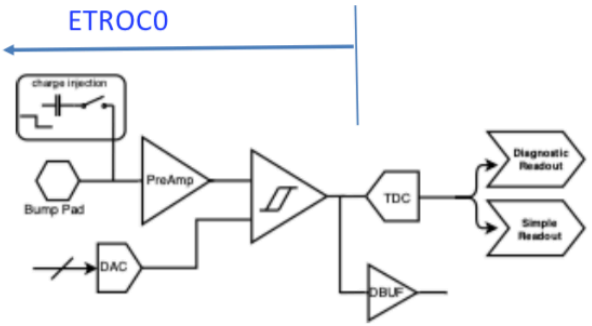
ETROC0 is used directly in ETROC1



The TDC is brand new design (low power)
~ one year development effort

ETROC1 TDC Design

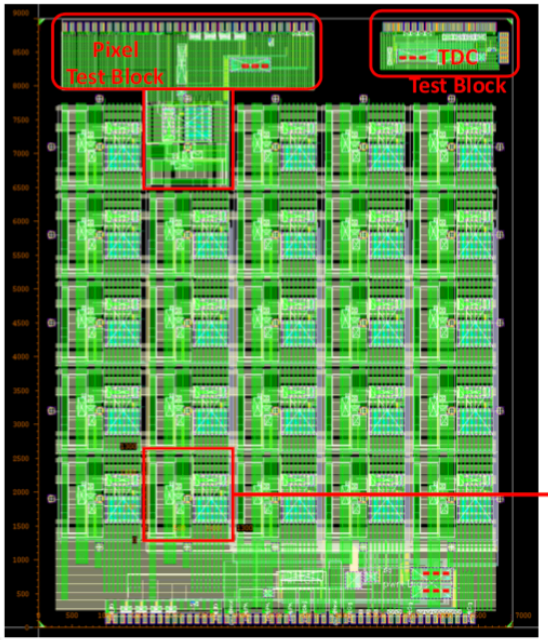
- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)



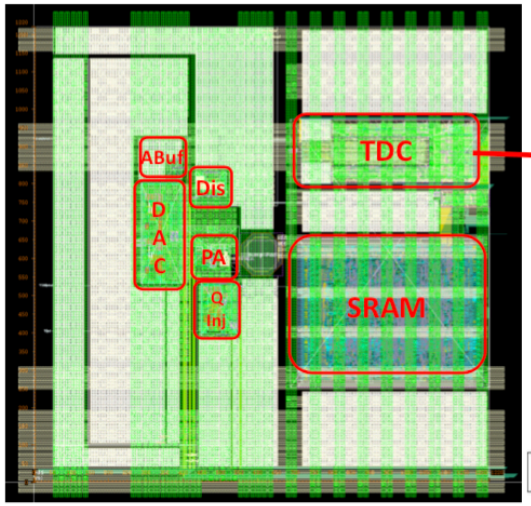
Extensive design verification has been done, mostly by EE students.

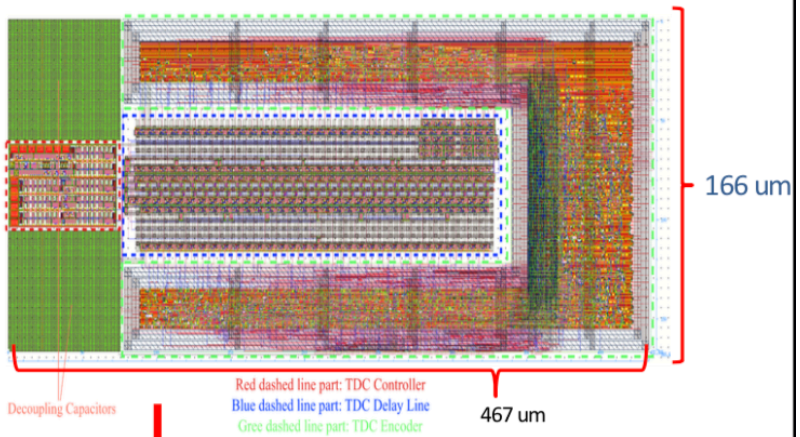
Low power TDC: <0.1mW

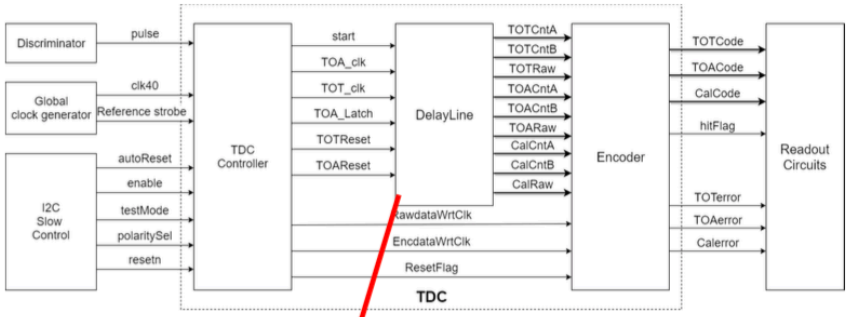
ETROC1 Top Layout



ETROC1 Single Pixel Layout





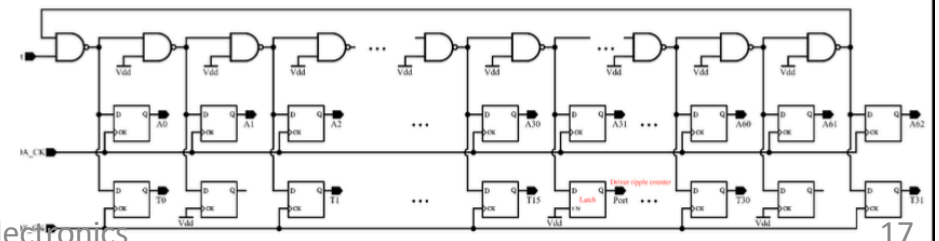


God-parent reviews in May and July 2019

ETROC1 submitted on time (Aug 28, 2019)

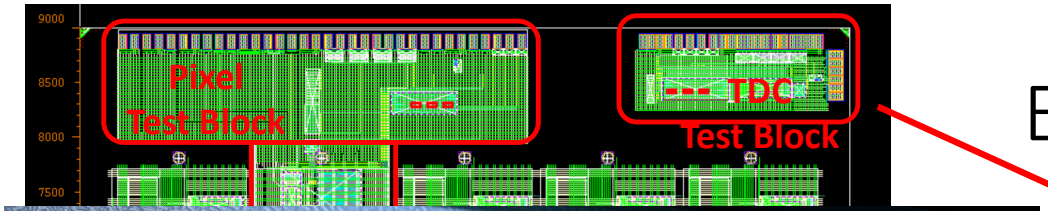
Chips arrived middle Dec 2019

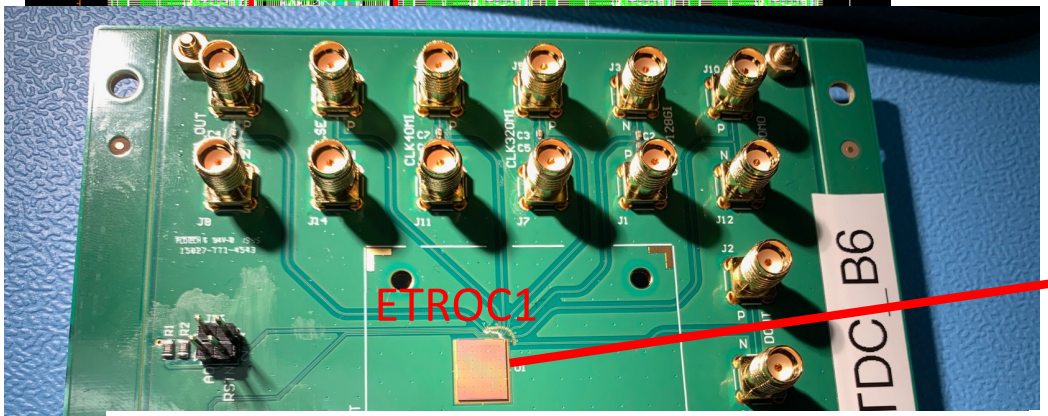
TDC core logic: gated ring oscillator

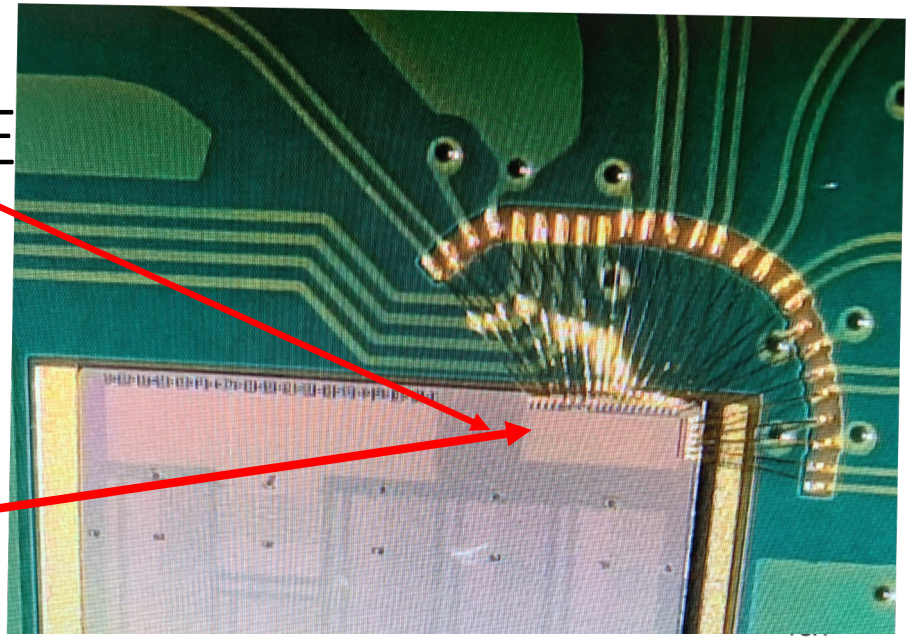


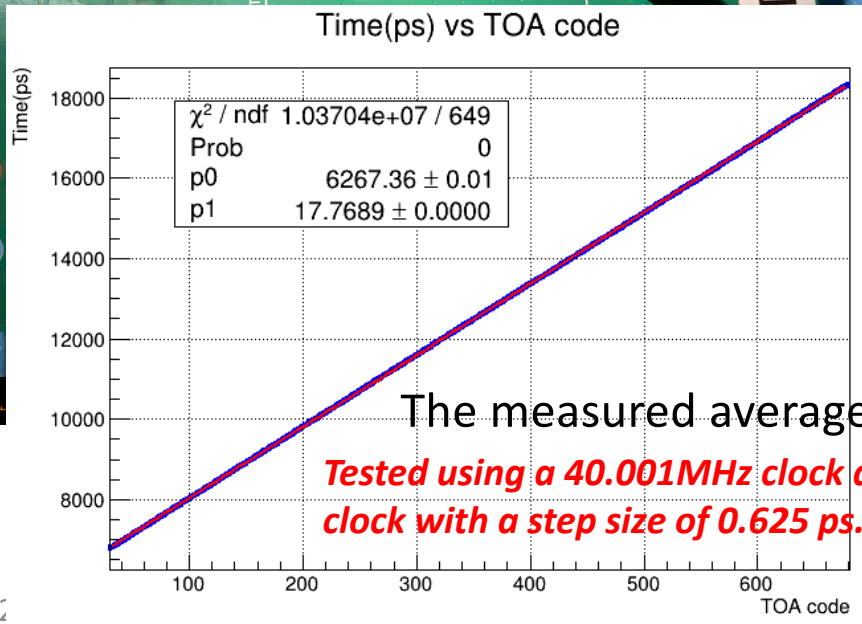
ETROC1 TDC resolution: ~ 6ps

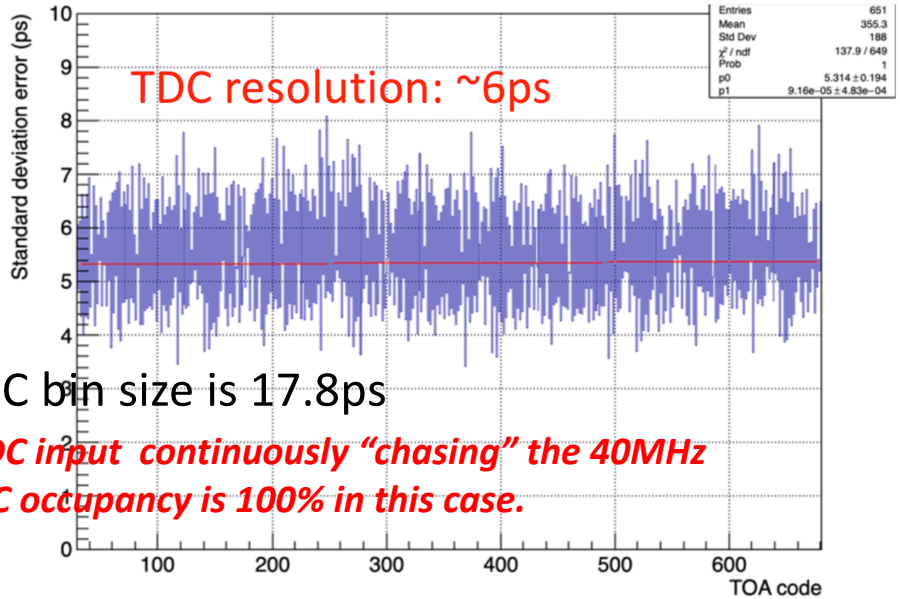
ETROC1 Top Layout











The measured average TDC bin size is 17.8ps

Tested using a 40.001MHz clock as TDC input continuously "chasing" the 40MHz clock with a step size of 0.625 ps. TDC occupancy is 100% in this case.

ETROC2&3: already on going

- ETROC specification has been developed (TDR)
  - Most critical components implemented in ETROC0&1
  - PLL is based on newly improved version from lpGBT
    - ***Mini-ASIC submitted last week***
- Full-chip clock distribution design advanced
  - The textbook H-tree clock distribution
- Waveform sampling spec and design developed
  - Single channel ADC prototype received last year, ***works well***
  - The core 2.56 GS/s waveform sampler submission in Feb 2020
    - ***Mini-ASIC received two weeks ago***
- Much of the supporting circuitries will be based on existing design blocks in 65nm from CERN (lpGBT)

Overall expected ETROC performance

Time resolution

LGAD+ preamp/discriminator + TDC bin	35 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	41 ps
Per track (2 hits) total time resolution	29 ps

To be verified with ETROC1 soon

With safety margin:
design specification is
~ 35ps per track (~50ps per hit),
< ~ 60ps per track at end of life

Power consumption

Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

All confirmed

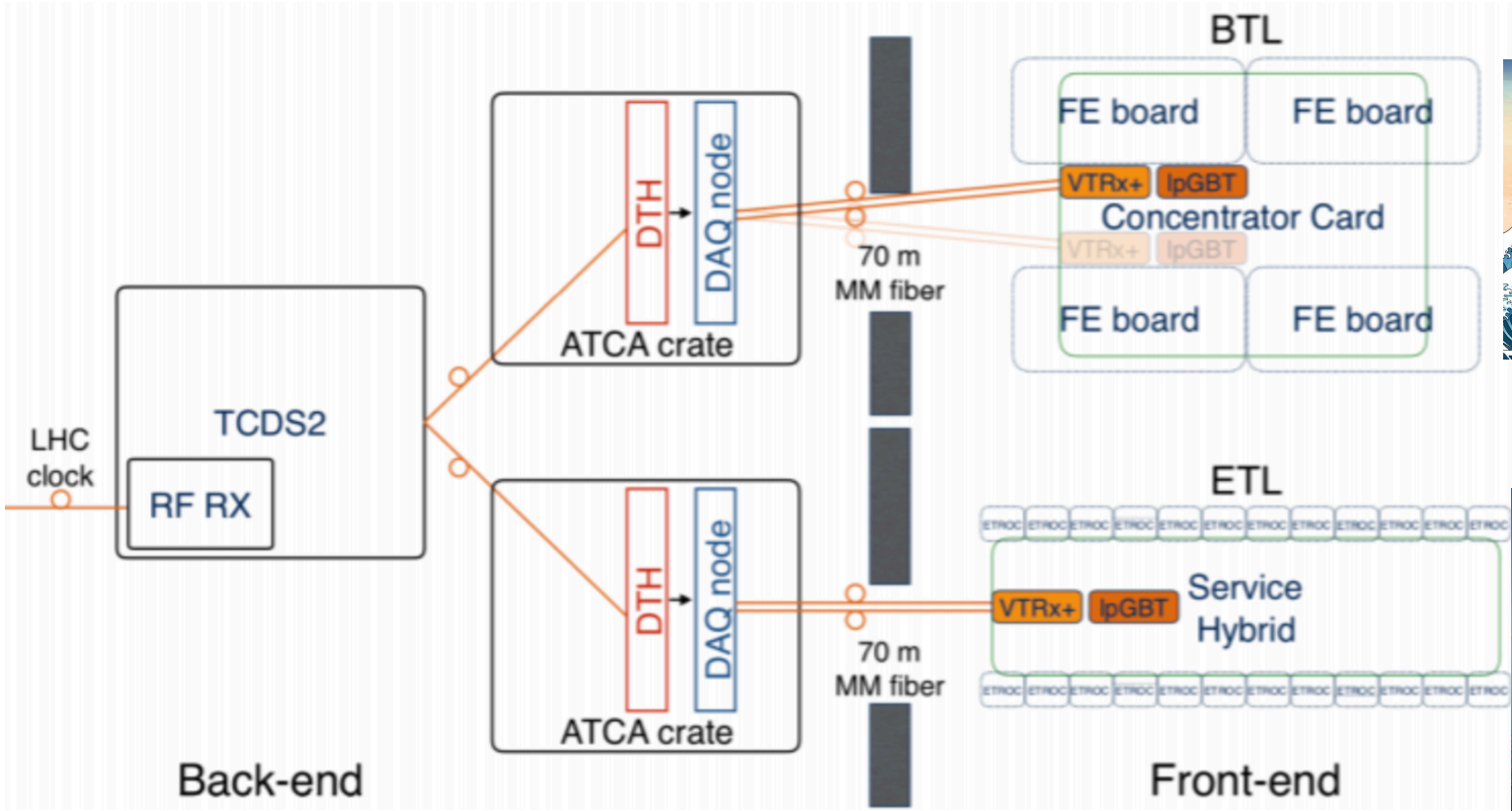
achieved 0.1mW

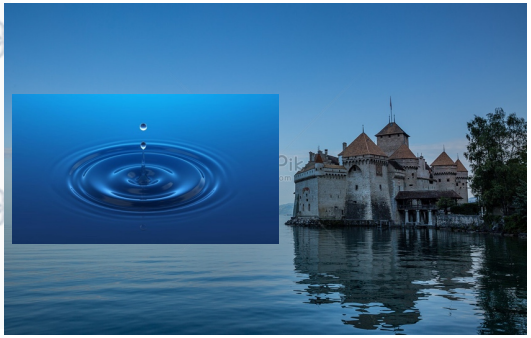
With safety margin:
design specification is
~ 1W per chip

Summary of ETL ETROC Status

- ETROC0
  - Charge injection — done (see backup)
  - Cosmic — done
  - Laser testing — done (see backup)
  - TID test to 100Mrads — done (see backup)
  - Beam testing — first round successful (early 2020)
- ETROC1 (chips received in Dec 2019)
  - TDC initial testing results — results good, power within spec
  - Single pixel full chain test — started, delayed (COVID-19)
  - Full ETROC1 testing — delayed (COVID-19)
  - ETROC1 and 5x5 LGAD bump-bonding — delayed (COVID-19)
- ETROC2: ***design in progress***
  - Aim for submission in Q1-Q2 2021

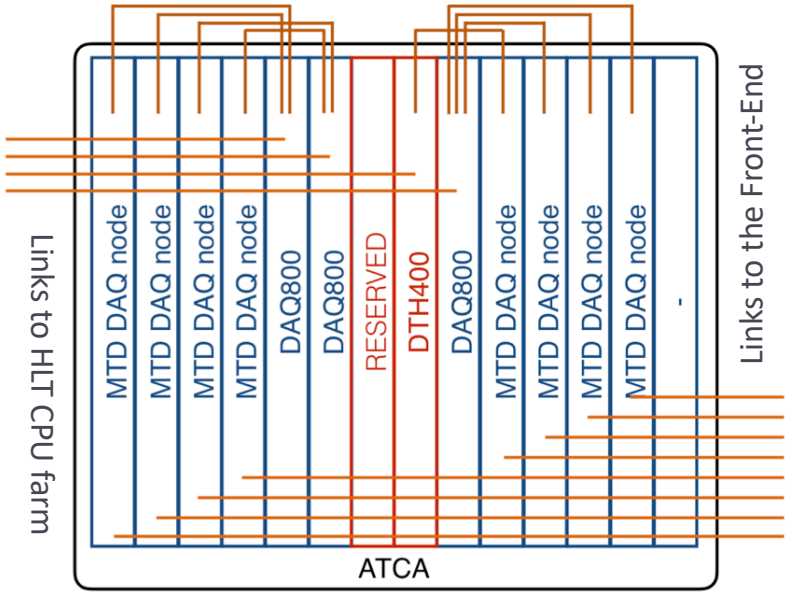
MTD electronics system



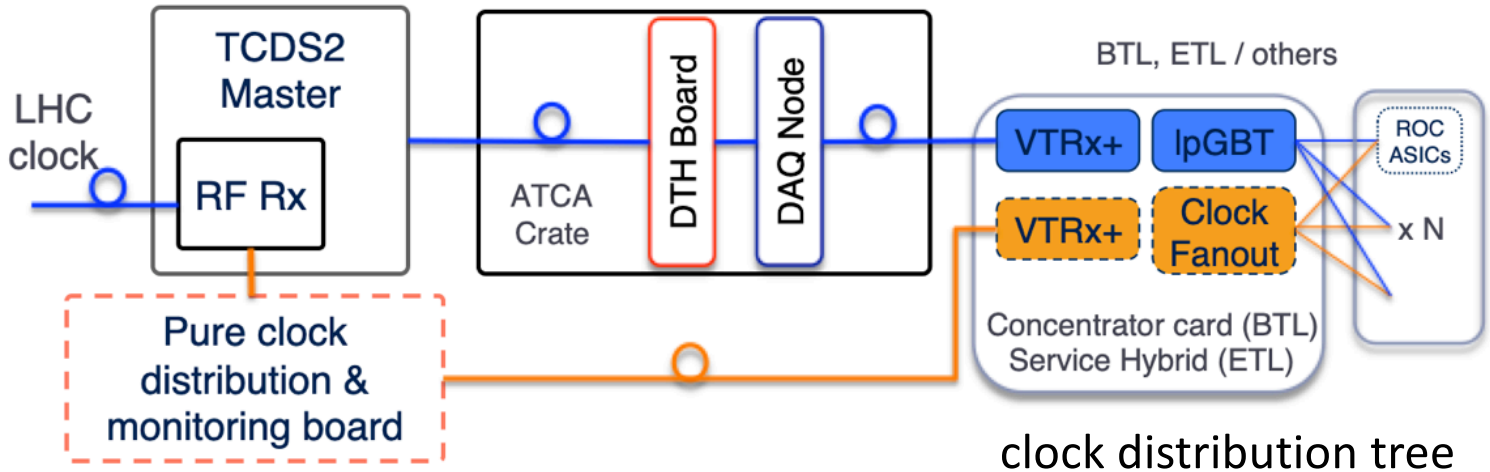


MTD DAQ and Clock distribution overview

- **DAQ: <0.4 Tb/s data rate at 750 kHz L1A**
  - Number of bi-directional links and data rate
    - BTL: 864 (2x redundant); 5.5 Gb/s / link
    - ETL: 1600 links; <1.5 Gb/s / link
  - Three ATCA crates with 8 (BTL) and 6+6 (ETL) MTD DAQ nodes (e.g. Serenity KUP15)
    - Being re-visited and optimized now
- Clock: <15 ps jitter (channel-to-channel)
  - **Baseline**: Encoded within lpGBT links
  - **Risk mitigation**: "Pure clock path"



Schematic of an MTD DAQ ATCA crate layout

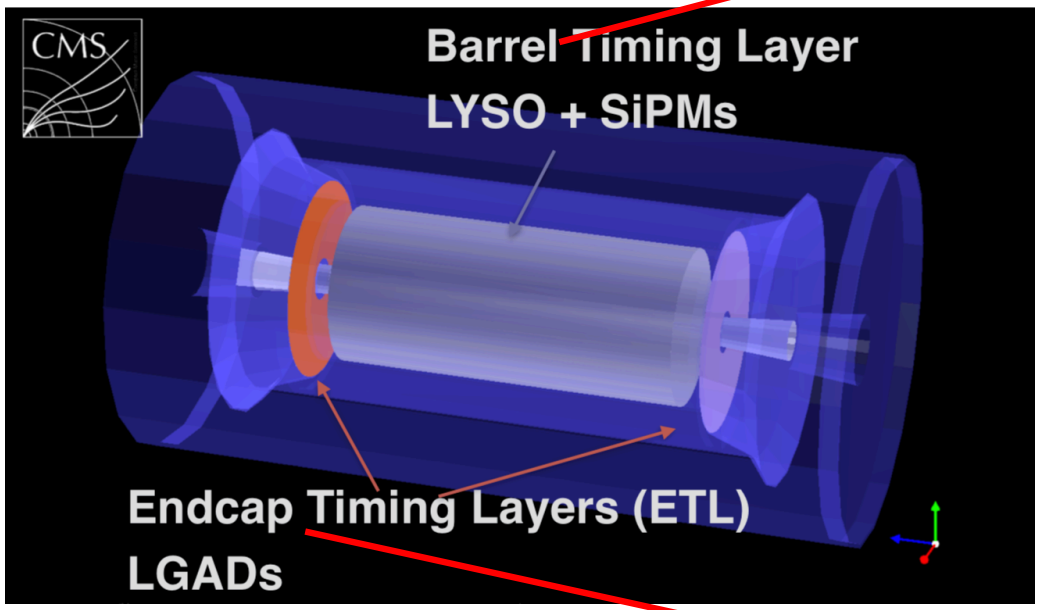


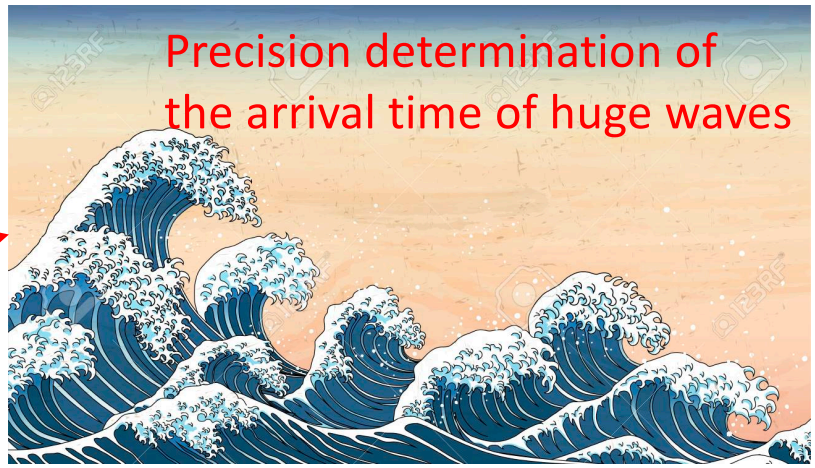
clock distribution tree

Summary

CMS MTD BTL and ETL are among the first generation precision timing detectors:

challenging front-end electronics design, tons of progress have been made over recent years
Exciting time ahead of us …





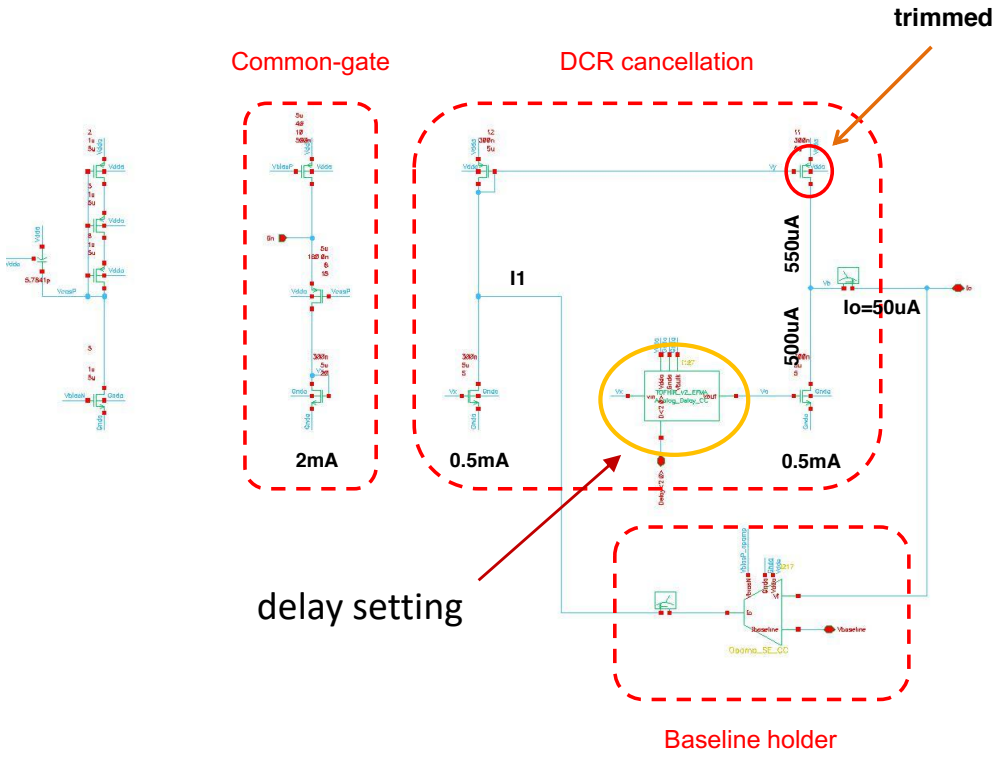
- Thin layers between tracker and calorimeters (BTL single layer, ETL double)
- with ***30-40 ps per track*** resolution at HL-LHC start, & <***60 ps*** at 3000 fb^{-1}

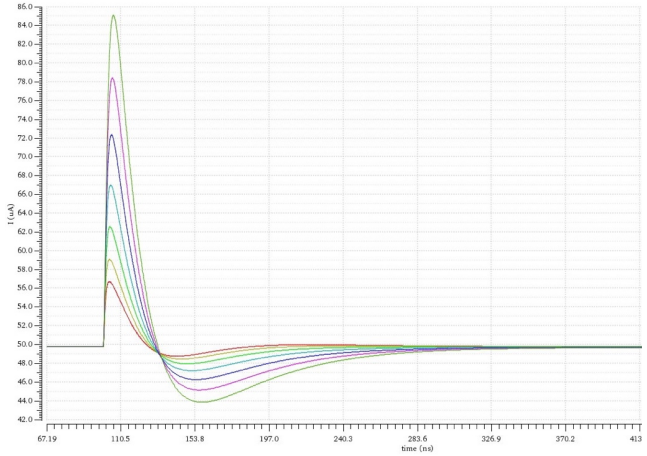
Backup slides

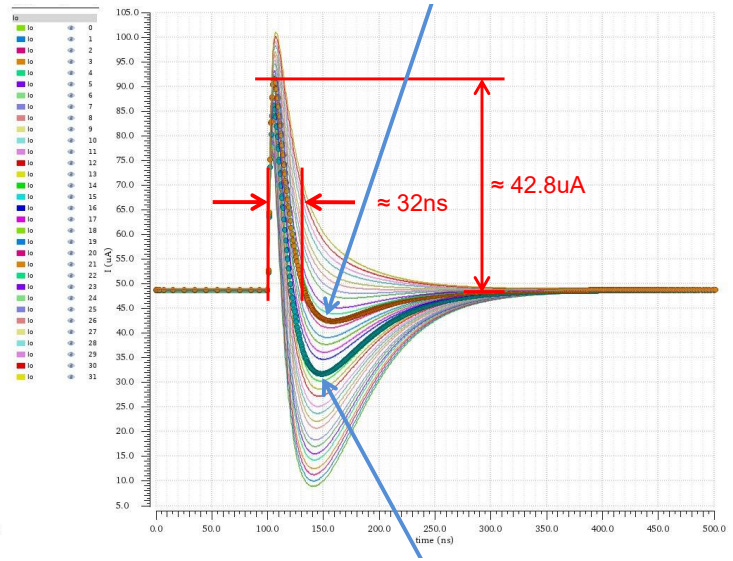
TOFHIR: Trimming the pulse shape

Trimming of the pulse shape to cope with PVT variations

- DCR cancelation delay (200-500 ps)
- PMOS transistor in current summation

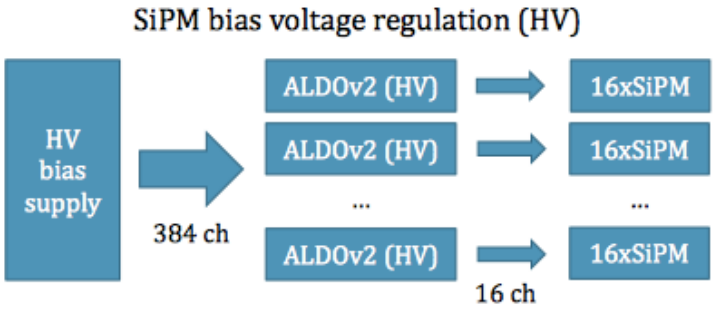


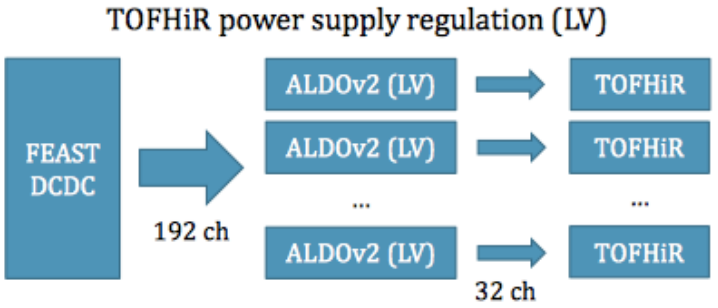




BTL ALDO2 ASIC

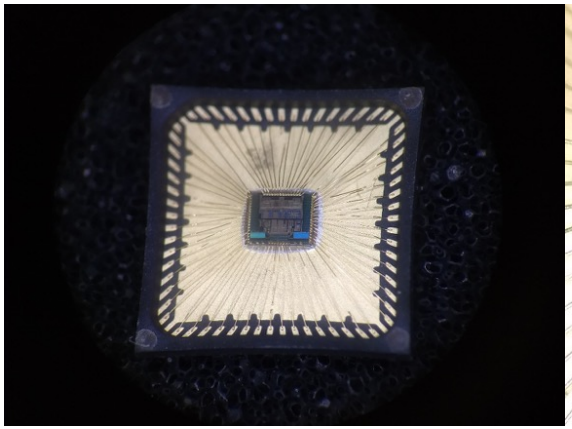
- SiPM bias voltage regulation
  - Finer segmentation and adjustable regulation
    - 16 channels for each independent bias line
  - Dark current measurement
- TOFHiR power supply regulation
  - Filter noise on power supply
  - Improve thermal and load stability
  - Finer segmentation
    - 1 TOFHiR for each ALDO

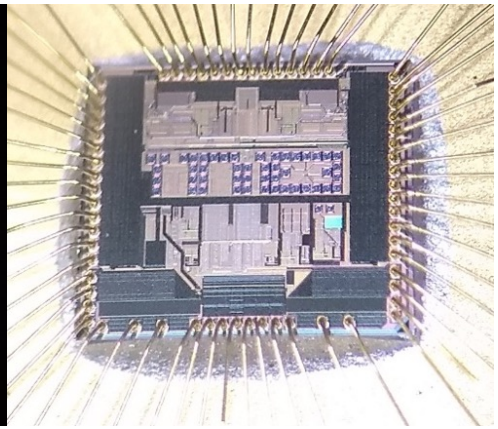




- Performance matches the simulation
- Radiation tests to be done

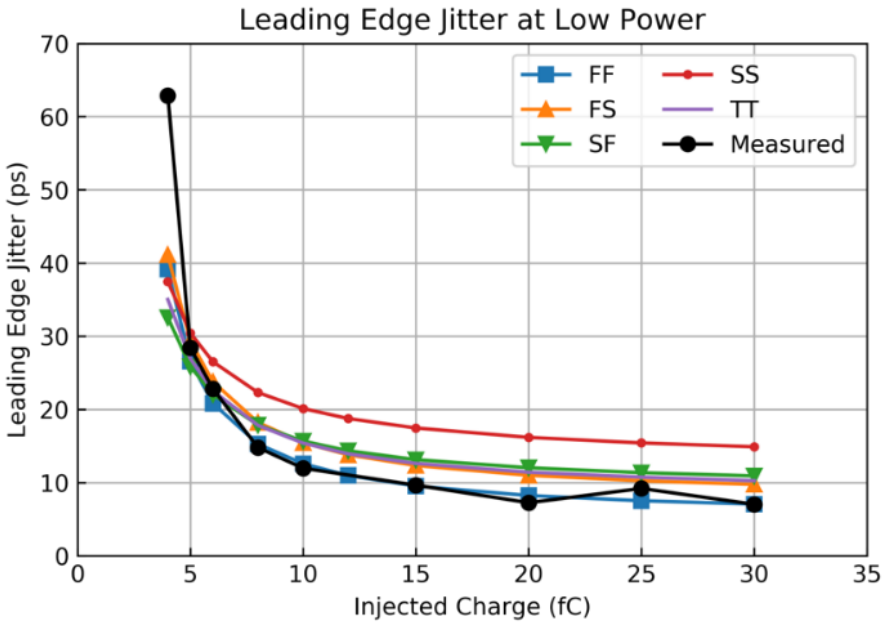
Details see ACES poster by Paolo Carniti.



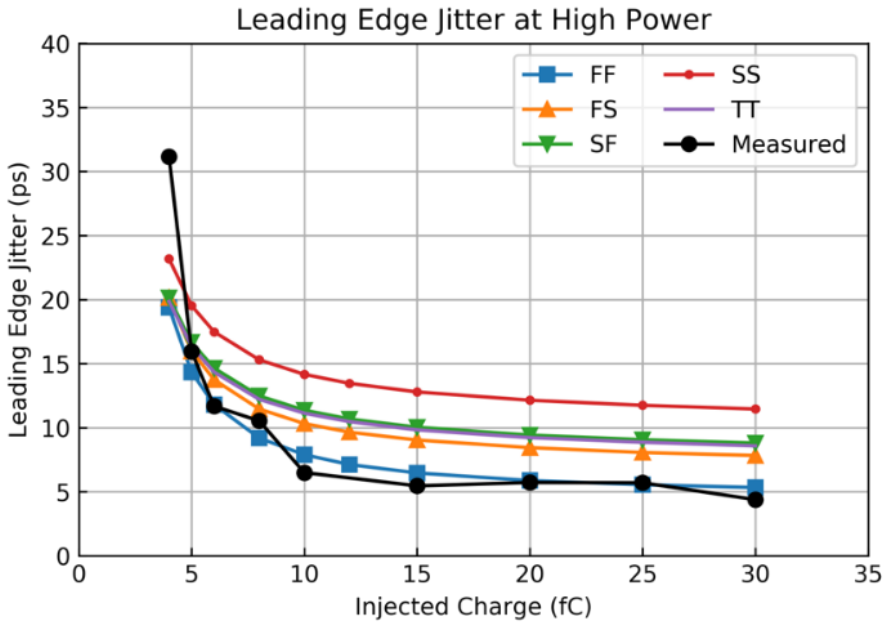


ETROC0 jitter: measured vs simulation

ETROC0 post-layout simulation vs testing results using 25ps risetime external pulse injection



(a)



(b)

ETROC0: Preamp + discriminator

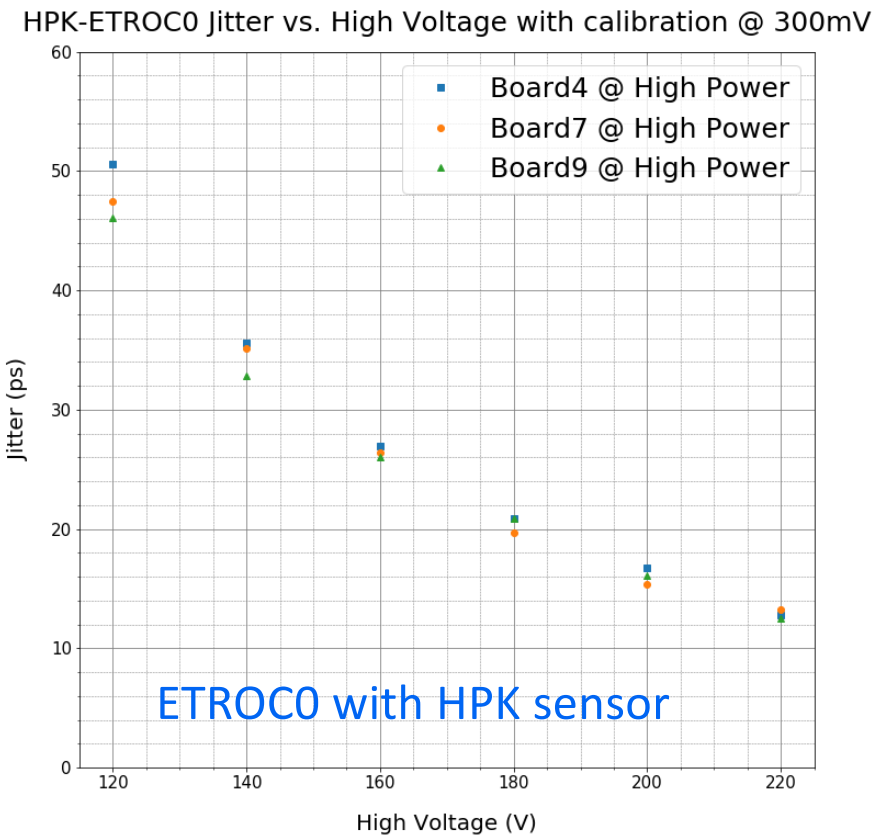
Summary of the charge injection testing:

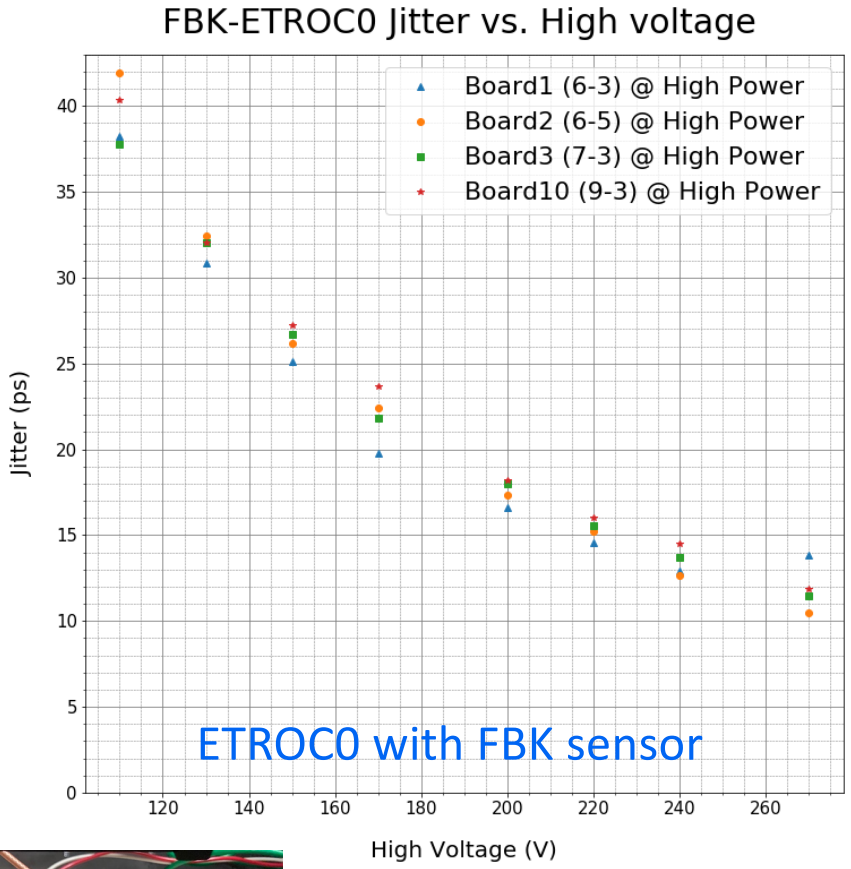
Discriminator leading edge jitter measurements agree with chip post-layout simulation

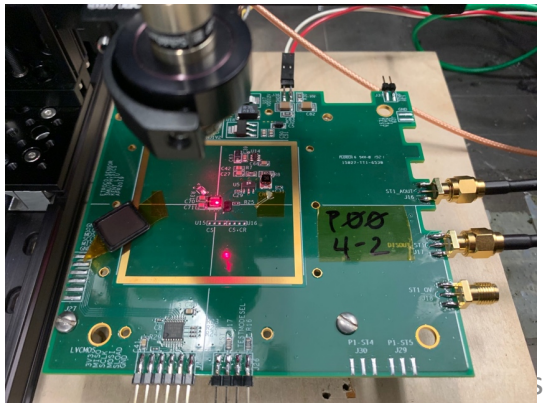
Power consumption for preamp and discriminator all match with simulation

Testing ETROC0 boards with laser before beam

HPK-ETROC0 and FBK-ETROC0 boards prepared in Jan 2020





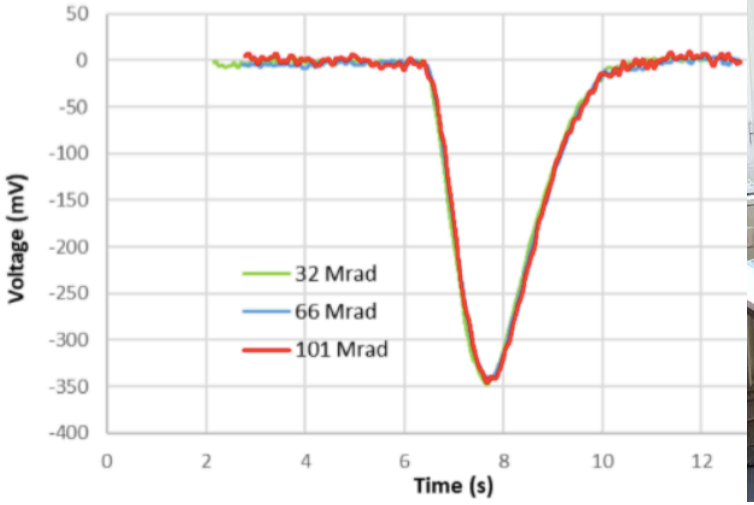


ETROC0 TID testing at CERN: Dec 2019

ETROC0 has been tested with TID up to 100Mrad: no issue found.

CERN x-ray irradiation facility: AsteriX,
Tube voltage: 40 kV. Tube current: up to 50 mA. Calibrated dose rate up to 8.09 Mrad/hr
https://espace.cern.ch/project-xrayese/_layouts/15/start.aspx#/AsteriX/Forms/AllItems.aspx

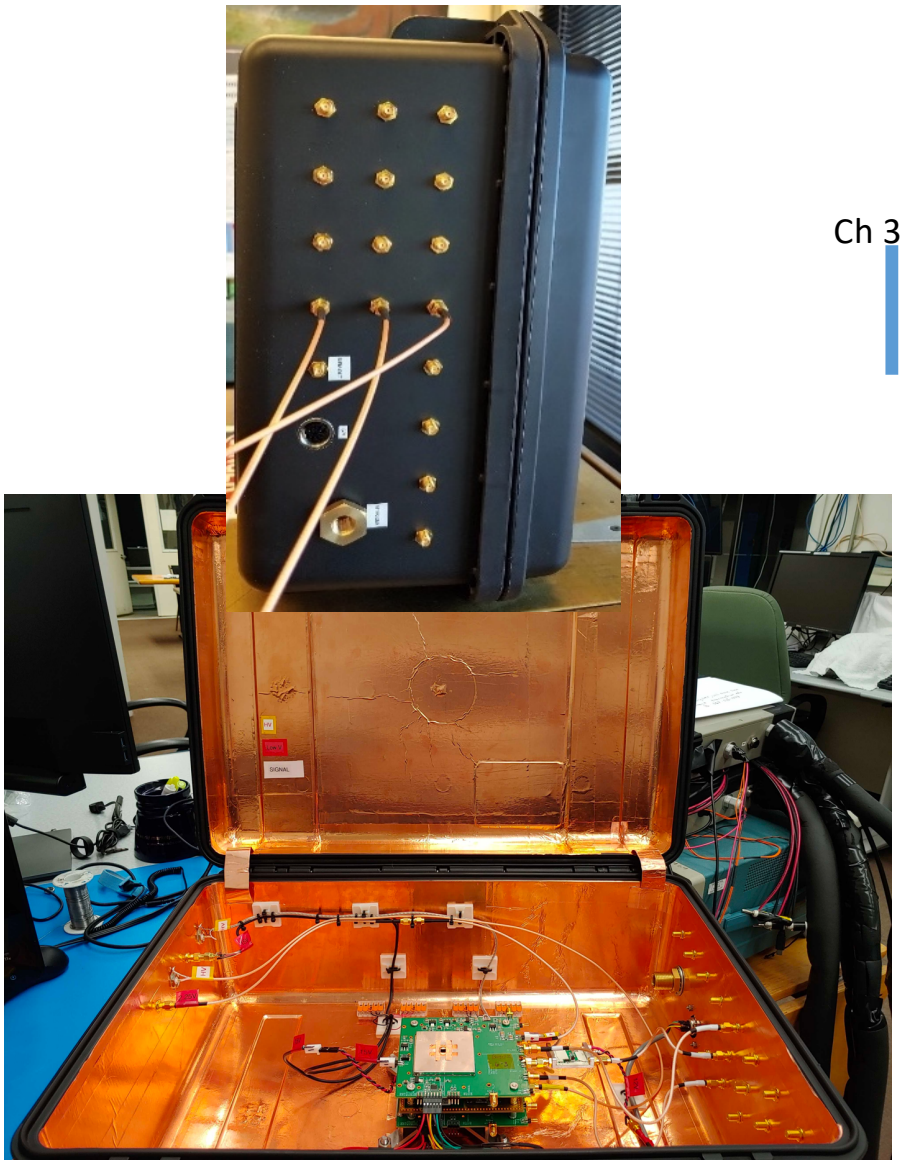
Preamp output
Pulses at different doses

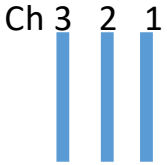


A simple ETROC0 Beam Telescope (3 boards)

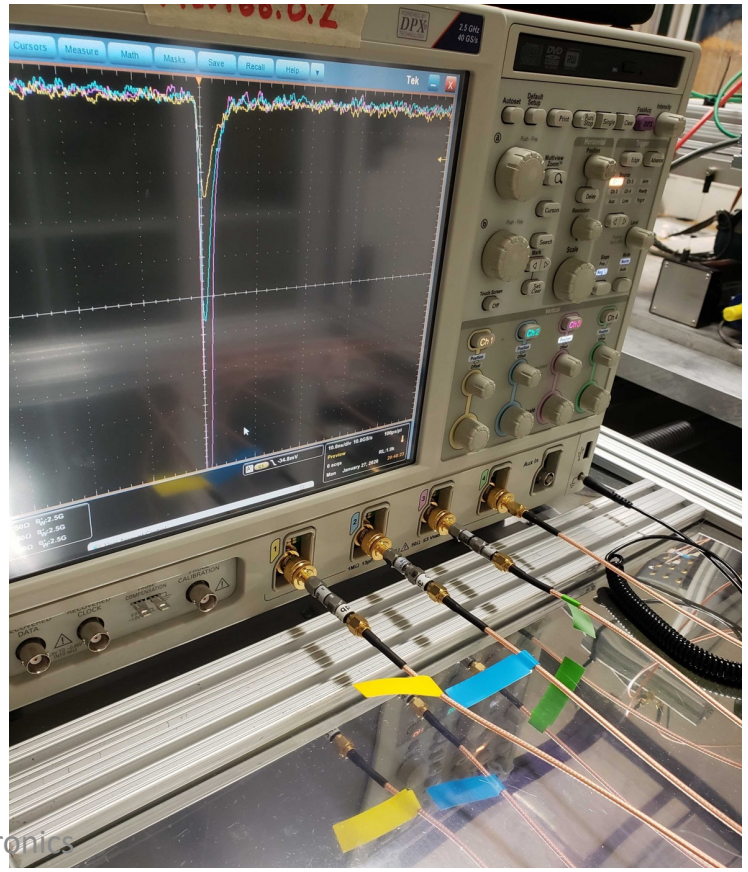
Jan-Feb 2020

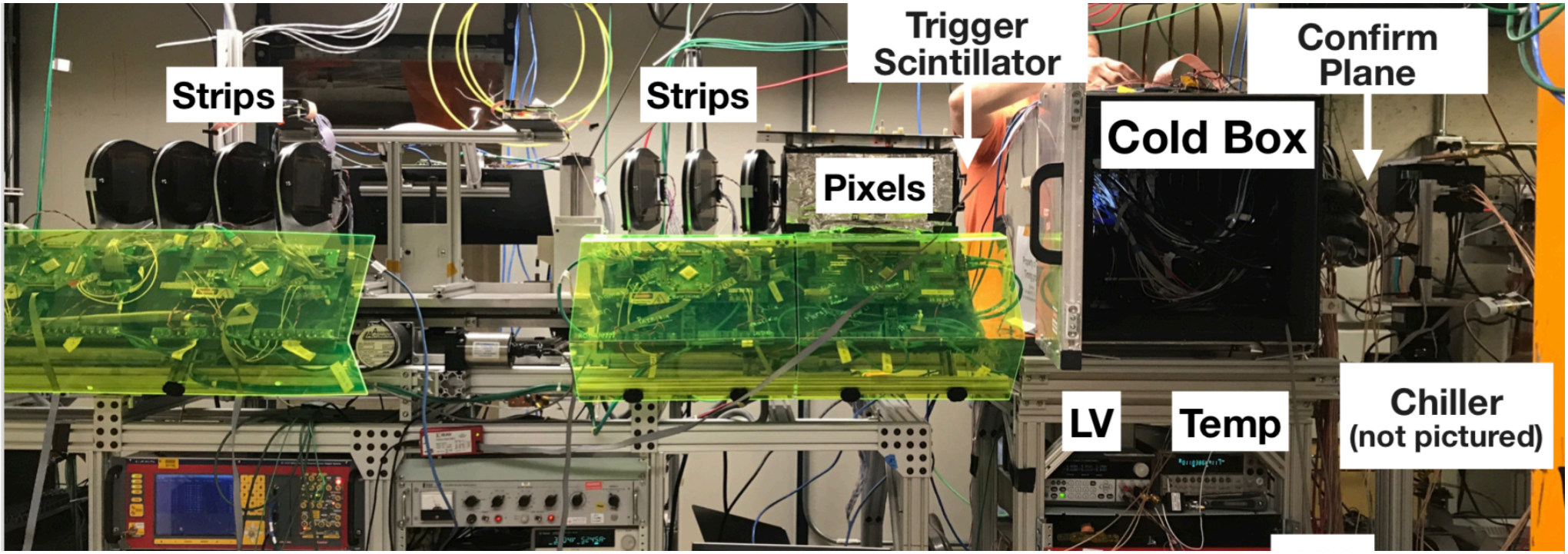
Simple "suitcase" setup in parasitic mode running at FNAL MTest



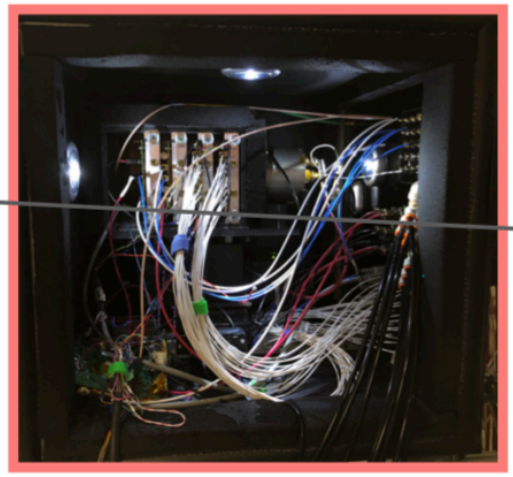


120 GeV proton Beam





Strip and Pixel Telescope



HPK-ETROC0 testing with ***full tracking***

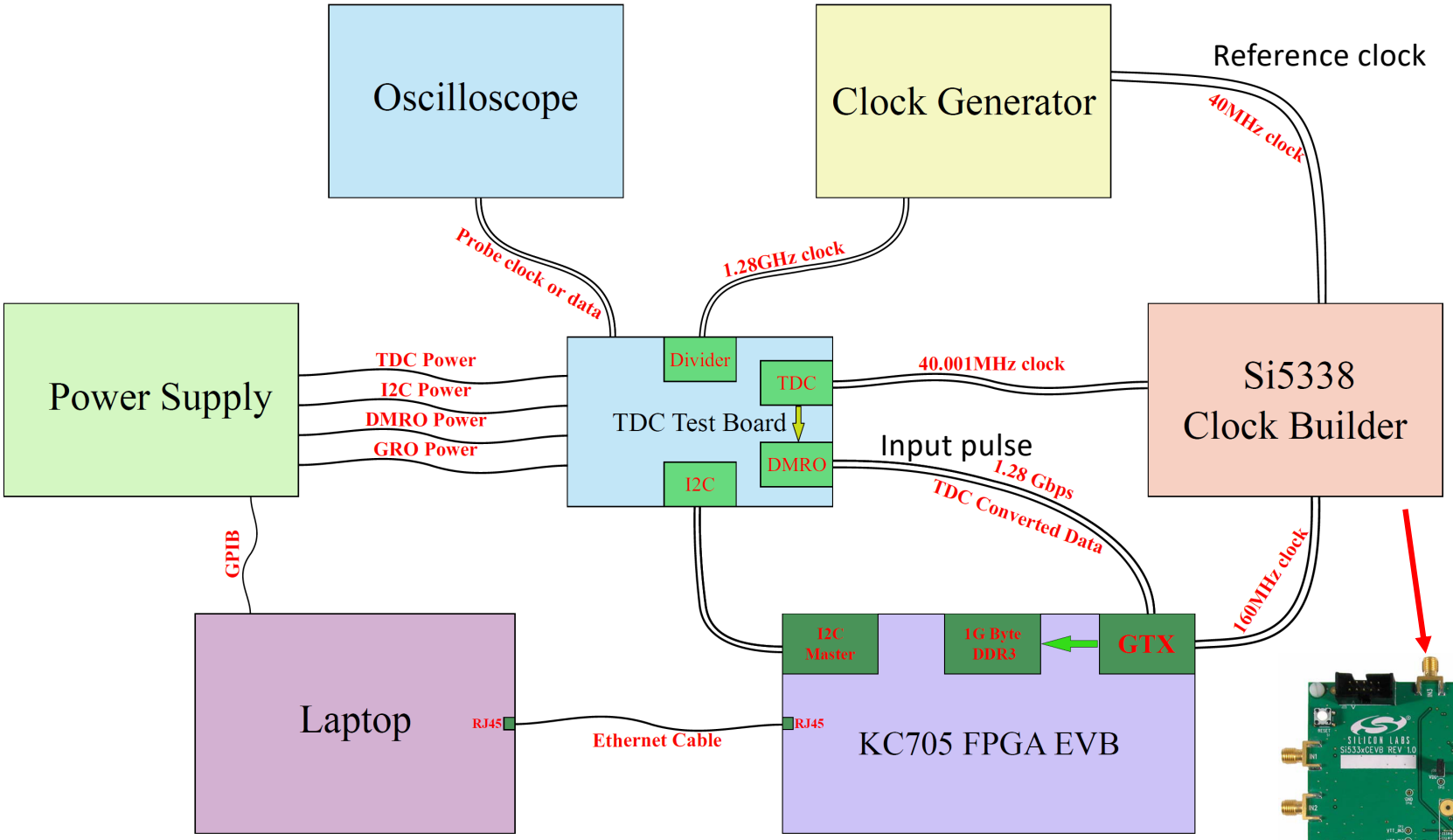
- MTD Beam Test Setup at FNAL MTest
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves waveforms
  - Study Δt(LGAD,MCP)

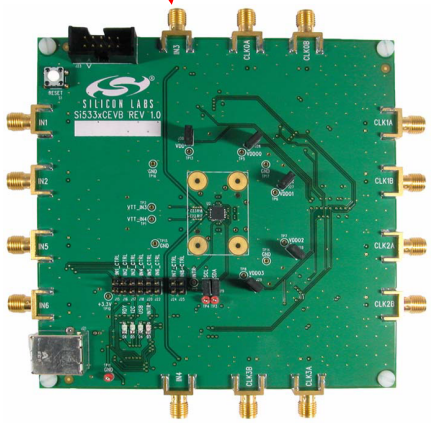
Cold box

LGAD boards on cooling blocks

MCP (Photek) time reference

ETROC1 TDC performance study setup





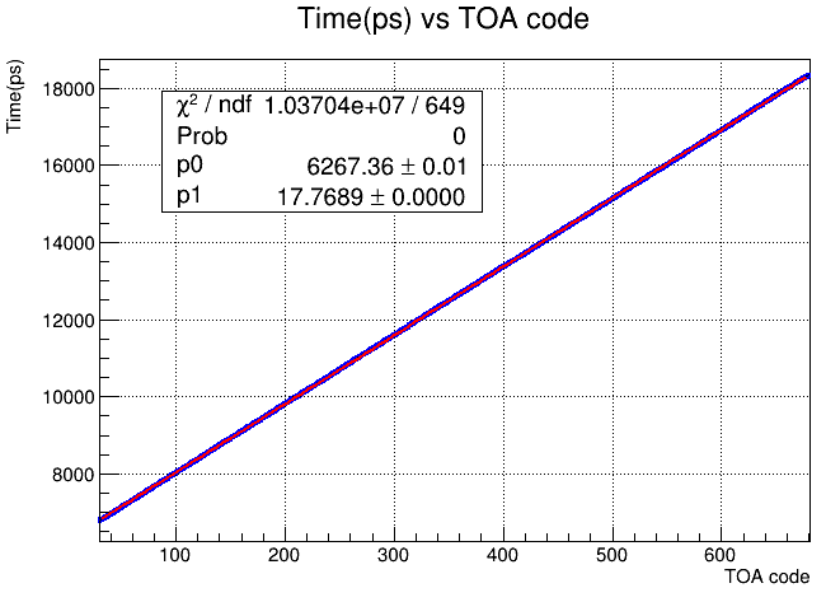
- The TDC input pulse and reference clock signals are all synchronous
- Use 40.001 MHz synchronous clock as TDC input,

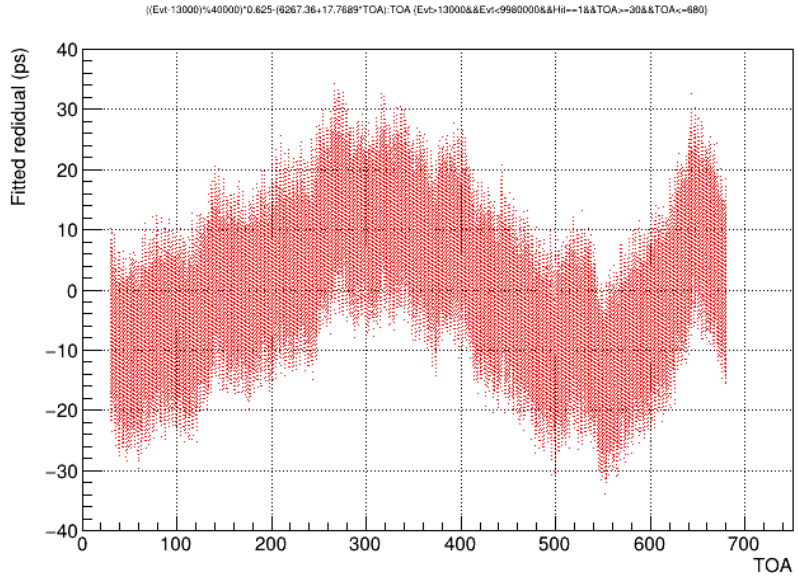
it is continuously "chasing" the 40MHz clock with a step size of 0.625 ps

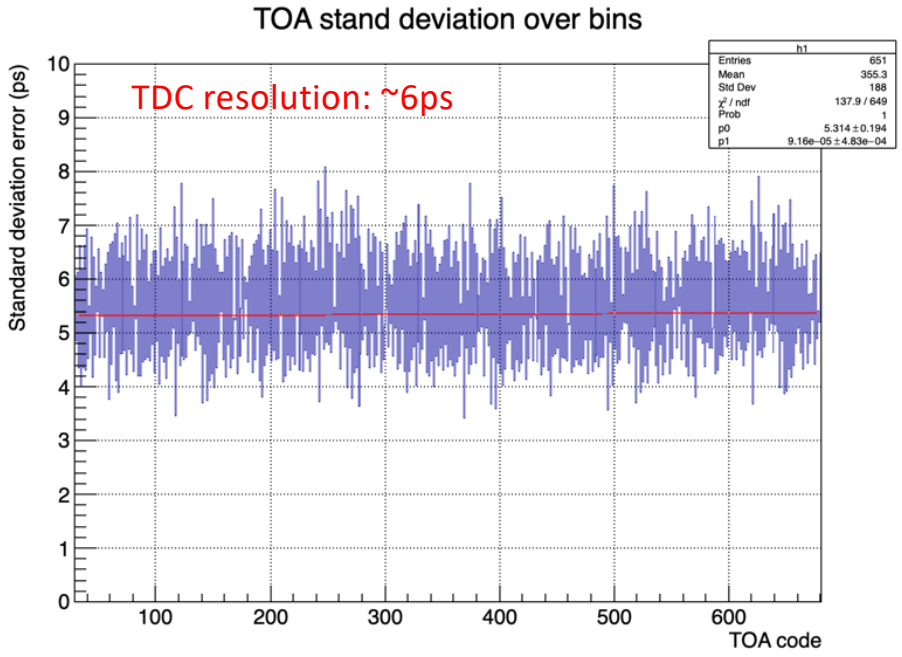
- When f_0 = 40 MHz and Δf = 1 kHz. The phase step size is 0.625 ps

The TDC resolution estimate

Tested with 100% TDC occupancy.
for real operation: up to few % occupancy.
The testing at lower occupancy was interrupted by COVID-19.



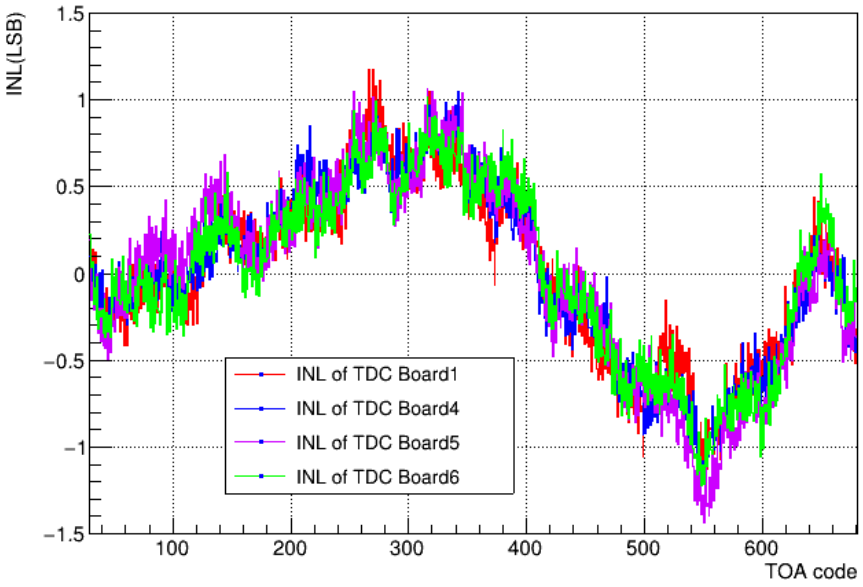


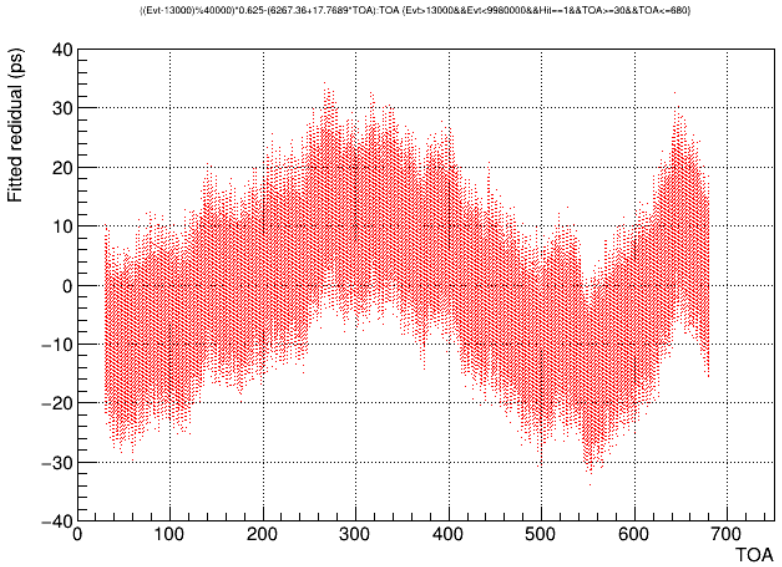


The measured average TDC bin size is 17.8ps

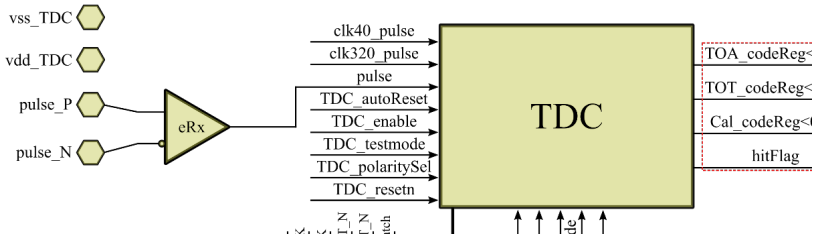
TDC INL measured from four boards

Measurements from four boards





TDC Power consumption measurement



eRx status	TDC status	Current(mA)	Power components
on	on	3.170	$TDC_{sta}+TDC_{occu}+eRx_{on}$
on	off	1.132	$TDC_{sta}+eRx_{on}$
off	on	0.068	$TDC_{sta}+eRx_{off}$
off	-	0.007	eRx_{off} (Estimate from simulation)

- The measured power of TDC block includes eRx and TDC core.
  - Both TDC and eRx can be turned on/off by I2C interface.
- We assume TDC power comprises of **standby power (**when no incoming hit), and **occupancy power**
- The measured TDC **occupancy power** is **2.446 mW** = 1.2x(3.170-1.132);
- The current of eRx is estimated to be 7uA when it is off, the **standby power** of TDC is 73 uW = 1.2*(68-7) uW
- When occupancy is 100%, the TDC power is 2.519 = 2.446+0.073 mW
- ***When occupancy is 1%, the TDC power is 73+2446*1% = 97 uW***