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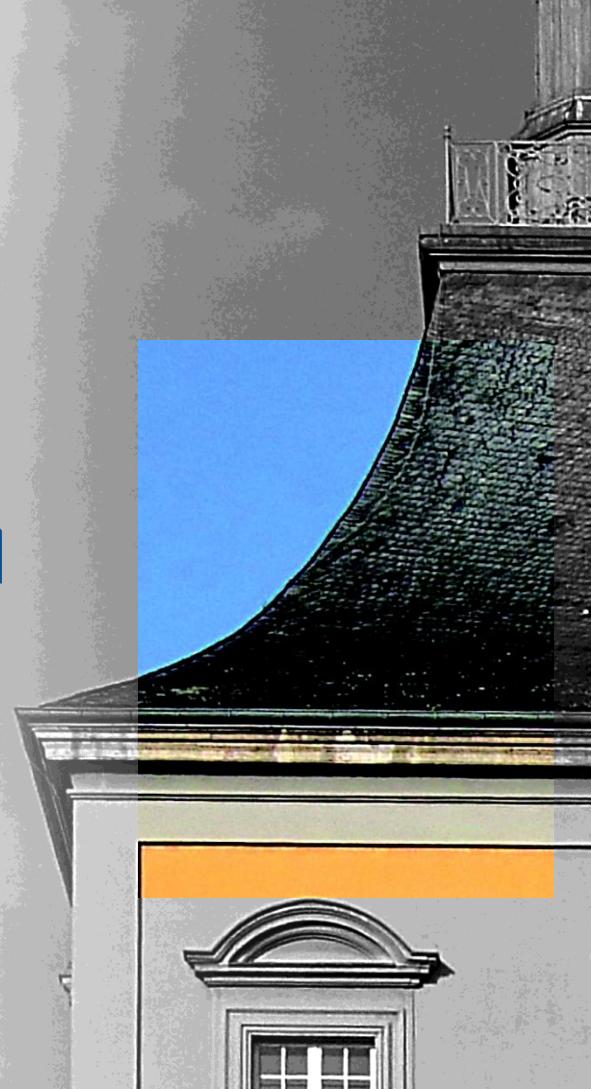
ACES 2020

SERIAL POWERING SYSTEM IMPLEMENTATION AND TEST RESULTS



Matthias Hamer

Special Thanks to Stella Orfanelli for providing material from CMS!

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OUTLINE

- Motivation for Serial Powering
- Overview for ATLAS and CMS
- System Level Test Results so far
  - example test from FE-I4 demonstrator
  - current RD53A test setups
- Optimisation of System Parameters:
  - Current Headroom
  - Slopes and Offsets
- Relevant Improvements in RD53B

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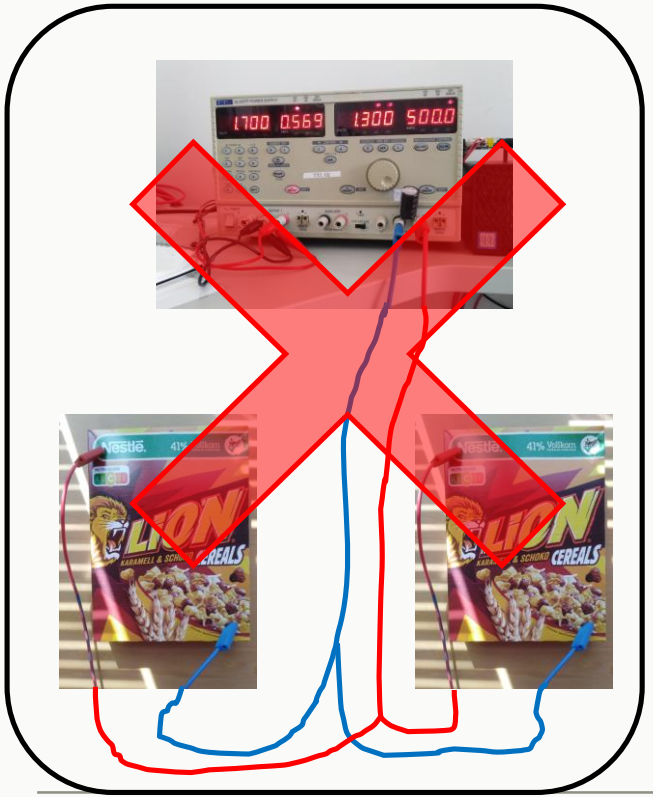
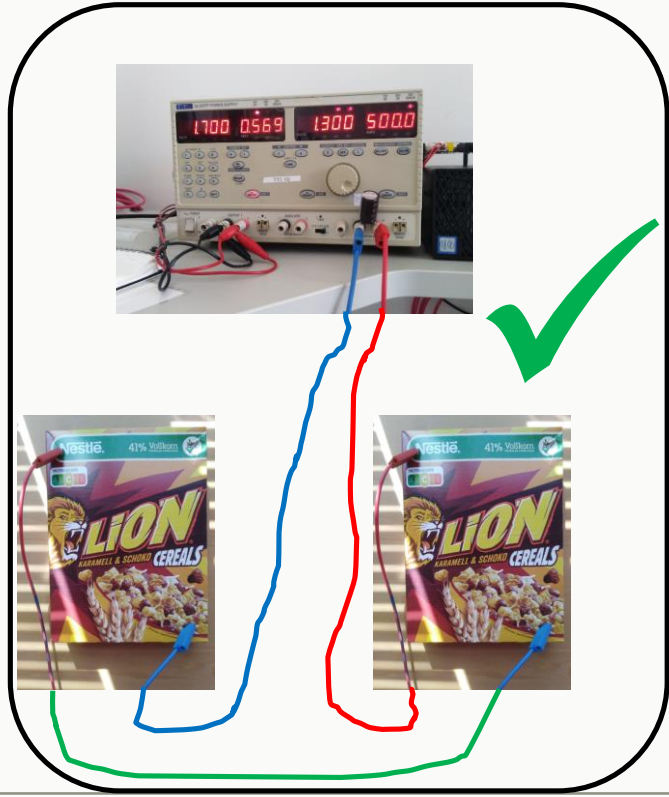
- Relevant Improvements in RD53B

the talk will be a bit ATLAS heavy
my apologies for that!

MOTIVATION FOR ~~CEREAL~~ Serial POWERING

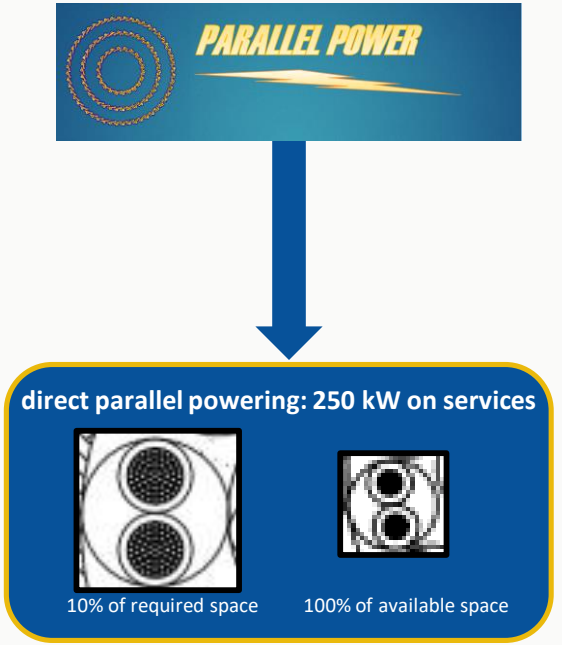




MOTIVATION FOR SERIAL POWERING

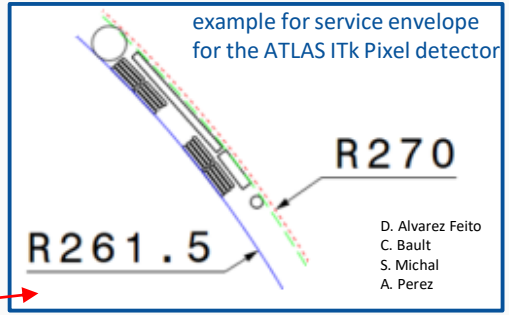
- upgraded pixel detector for ATLAS and CMS
  - will have significantly more modules than their predecessors
  - will have significantly more pixels per area than their predecessors
  - will feature a similar services volume as their predecessors

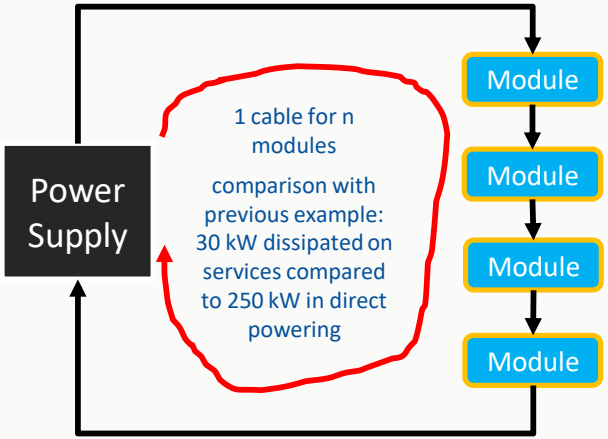
- currently used parallel powering scheme is not feasible
  - example ATLAS: assuming a current consumption of 1.25 A per readout chip and AWG 14 cables to power all the chips from the service caverns to the modules:
    - > 250 kW dissipated on services
    - compared to ~70 kW delivered power



MOTIVATION FOR SERIAL POWERING

- two alternatives for direct parallel powering
  - parallel powering with DC-DC conversion close to the module
    - significantly lower ohmic losses on major part of services
    - POL DC-DC converters close to modules with shielded air coils
    - space constraints effective rule this out
  - serial powering of pixel modules
    - Shunt-LDO regulators on modules/chips
    - ‘recycle’ current from one module to another
    - details of implementation not always straight forward

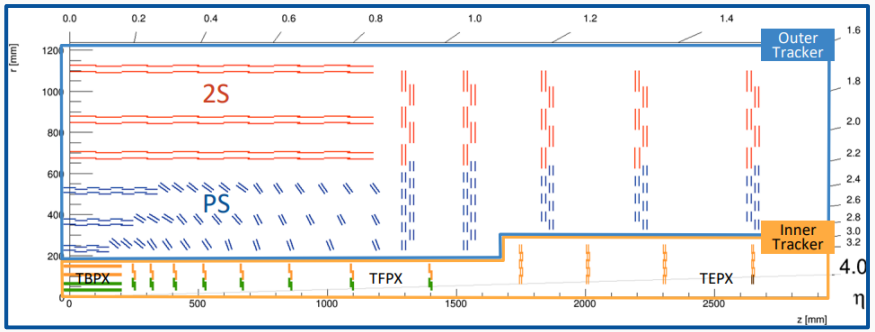


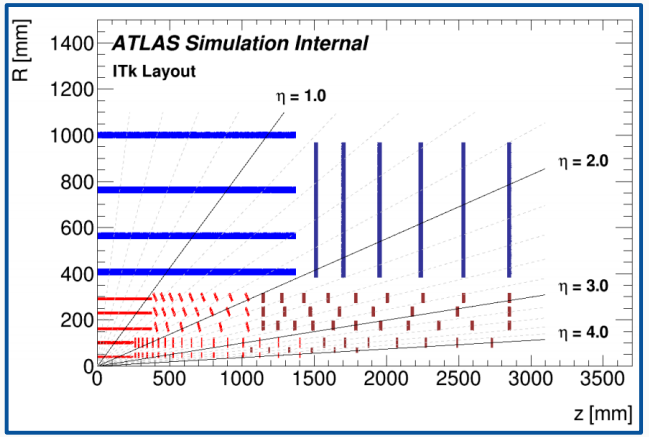


Overview for ATLAS and CMS

SERIAL POWERING CHAINS IN ATLAS AND CMS

CMS Phase 2 Tracker Layout

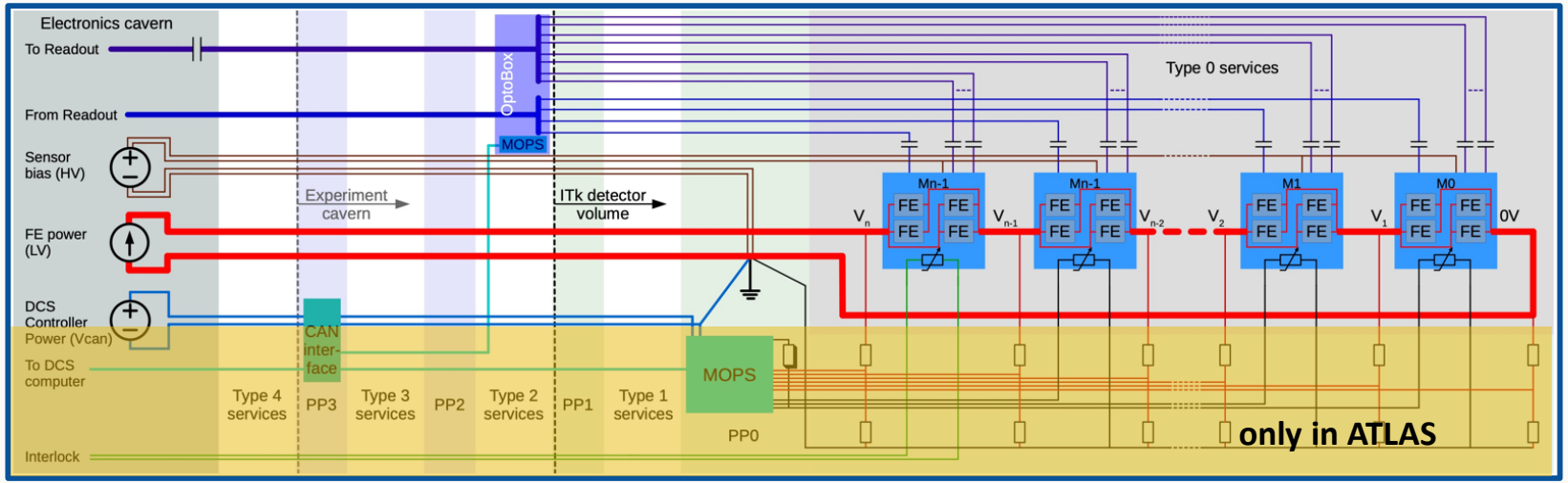




- serial powering to be deployed in Inner Tracker
- 3900 pixel modules with 2 Gigapixels (124 M in Phase-1)
- 500 serial powering chains with up to 12 modules per chain
- 13,256 readout chips
- 4 layers with about 5 m^2 of active silicon

- serial powering to be deployed in the pixel detector
- 8372 pixel modules with 5 Gigapixels (100 M in Phase-1)
- 900 serial powering chains with up to 14 modules per chain
- 33,092 readout chips
- 5 layers with about 13 m2 of active silicon

SERIAL POWERING IN A NUTSHELL

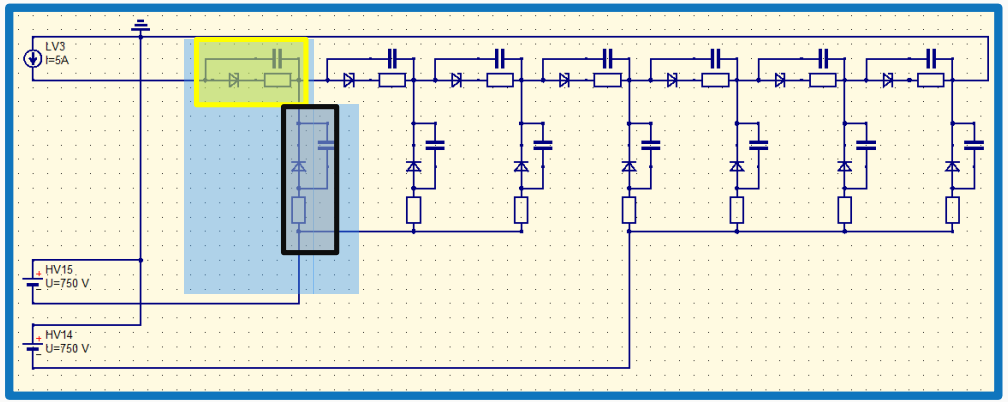


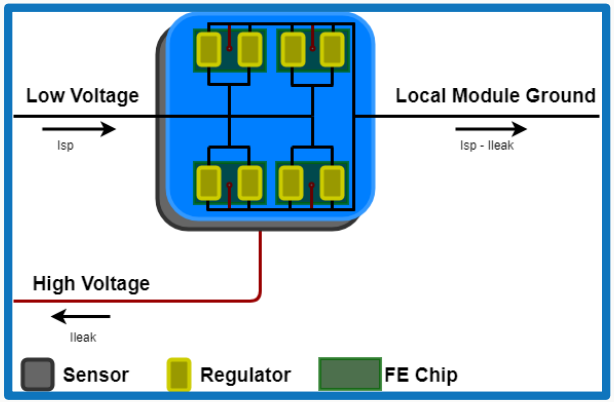
- example schematic from ATLAS including Monitoring of Pixel System Chip
  - 2 HV lines per Serial Powering Chain in most of the detector – sharing a common 'return' line with the LV
  - both HV and LV lines share a common reference with the MoPS at a starpoint on the local supports
  - no active components in both LV and HV lines between modules and power supplies
  - AC coupled data transmission lines to the optosystem

Test Results so Far

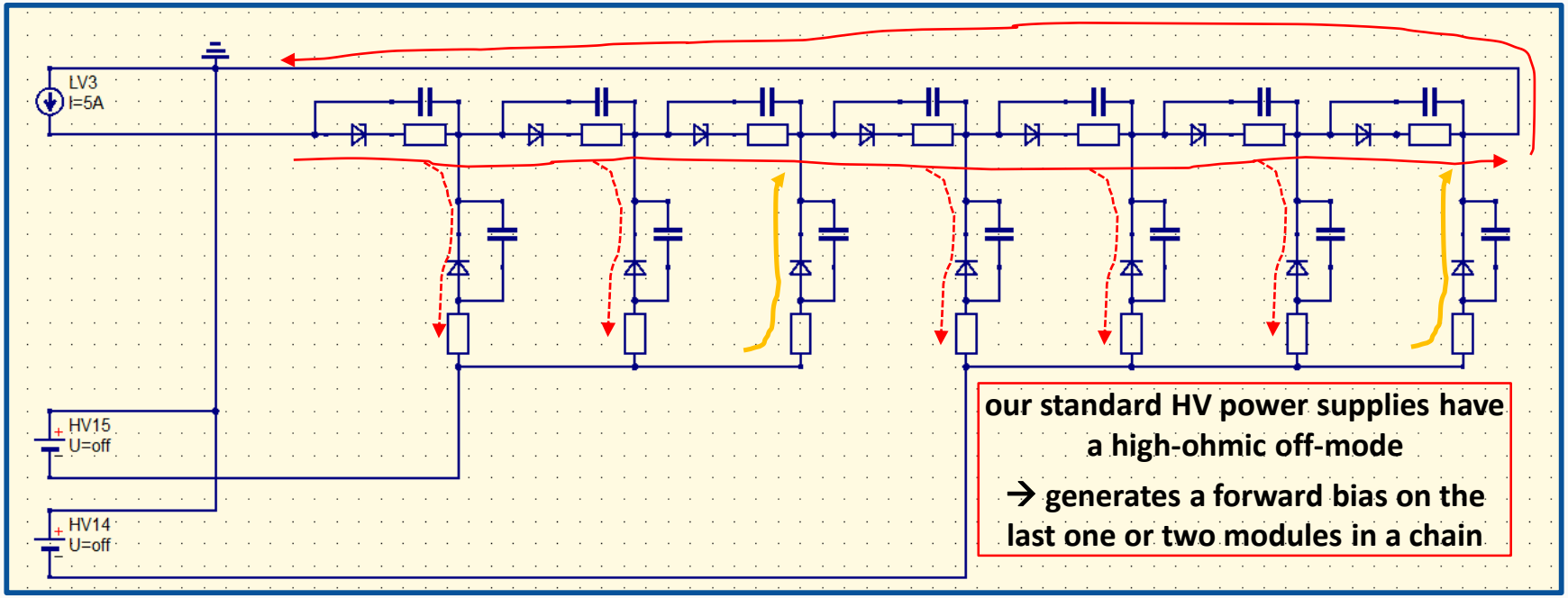
SYSTEM LEVEL CONSIDERATIONS - HIGH VOLTAGE DISTRIBUTION AND GROUNDING

- consequences of distributing the HV in parallel to sensors that are bonded to serially powered readout chips
  - in both systems, the High Voltage is negative with respect to the local module ground
  - expecting regularly during operations that LV will be switched on, but HV will be switched off
  - this generates an effective bias voltage on some of the sensors in a chain, and a leakage current that is returned through the HV power supply or through other sensors





SYSTEM LEVEL CONSIDERATIONS - HIGH VOLTAGE DISTRIBUTION AND GROUNDING



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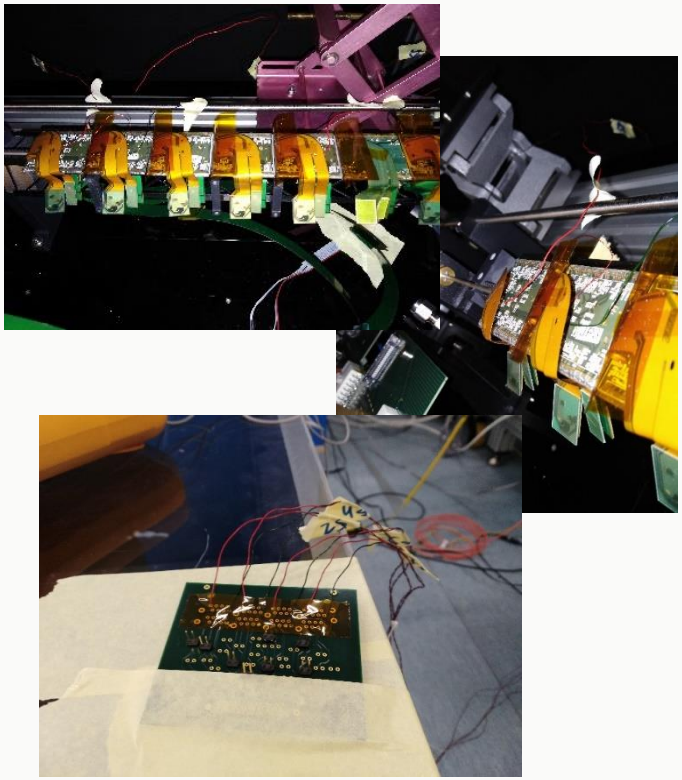
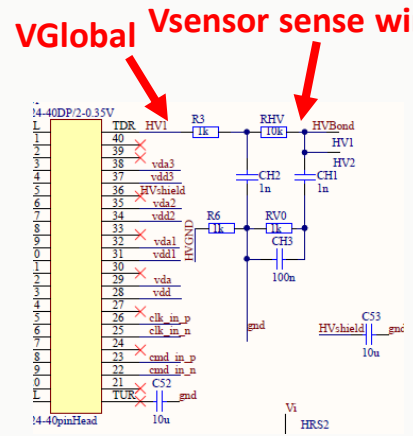
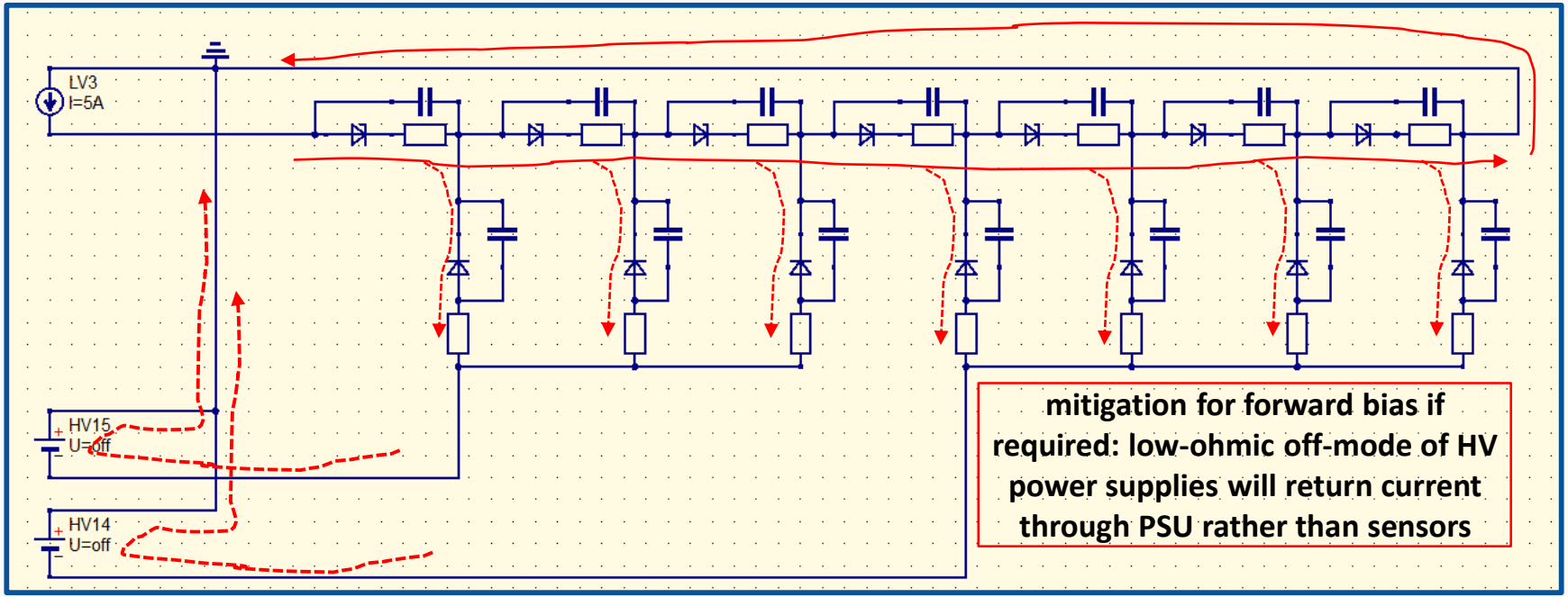




- measurements with ATLAS OB FE-I4 demonstrator
- one serial powering chain with 7 modules, one HV line
- BM4 and BM5 were disconnected from common HV line due to broken sensor
- measurements repeated and consistent with 2 HV lines per chain
- 95+% of LV induced leakage current are returned through the last module in the chain
- unclear if this presents a risk after irradidation (several mA expected)

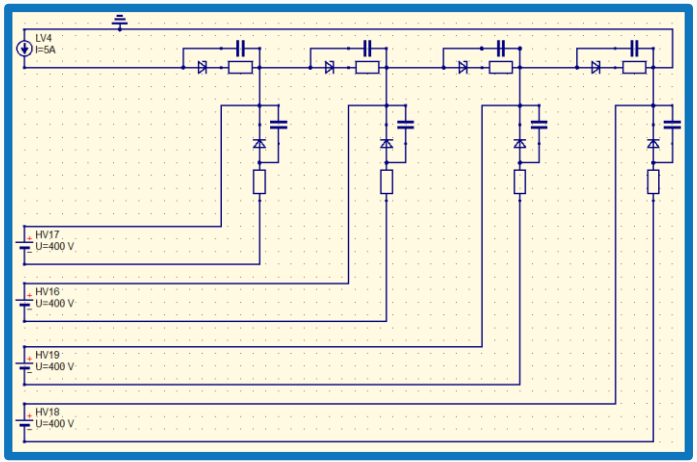
Module	Voltage Drop [V]	R_HV [Ohms]	Vglobal [V]	Vsensor [V]	Drop over R_HV [V]	ISensor [uA]
BM1	2.12	11000	0.701	0.368	0.333	30.27
BM2	1.78	10000	0.701	0.724	-0.023	-2.30
BM3	1.95	11000	0.701	0.92	-0.219	-19.90
BM4	1.99	11000	0.701			
BM5	2	11000	0.701			
BM6	2	11000	0.701	0.742	-0.041	-3.72
BM7	2.01	11000	0.701	0.754	-0.053	-4.81

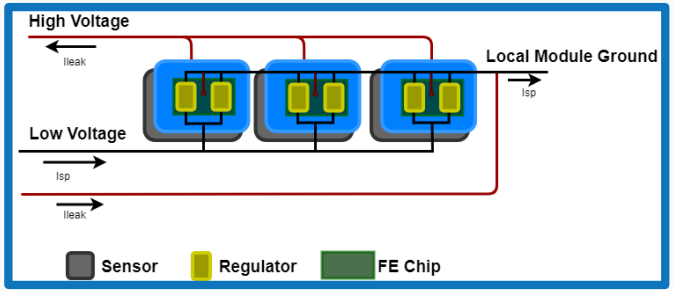
SYSTEM LEVEL CONSIDERATIONS - HIGH VOLTAGE DISTRIBUTION AND GROUNDING



SYSTEM LEVEL CONSIDERATIONS - HIGH VOLTAGE DISTRIBUTION AND GROUNDING

- what remains is an effective bias on almost all modules even with the HV switched off
  - this bias is mostly small compared to the depletion voltage of planar sensors
  - it can be sizeable even in short serial powering chains for 3D sensors
  - ATLAS will build the innermost layer with such sensors different HV distribution scheme chosen

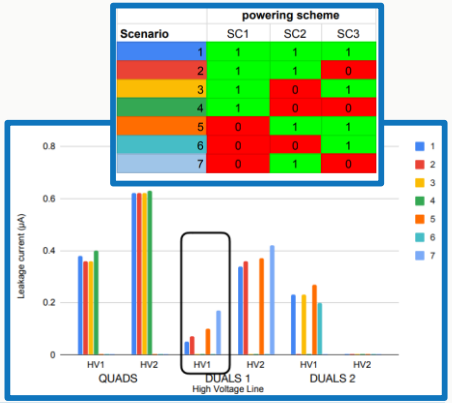


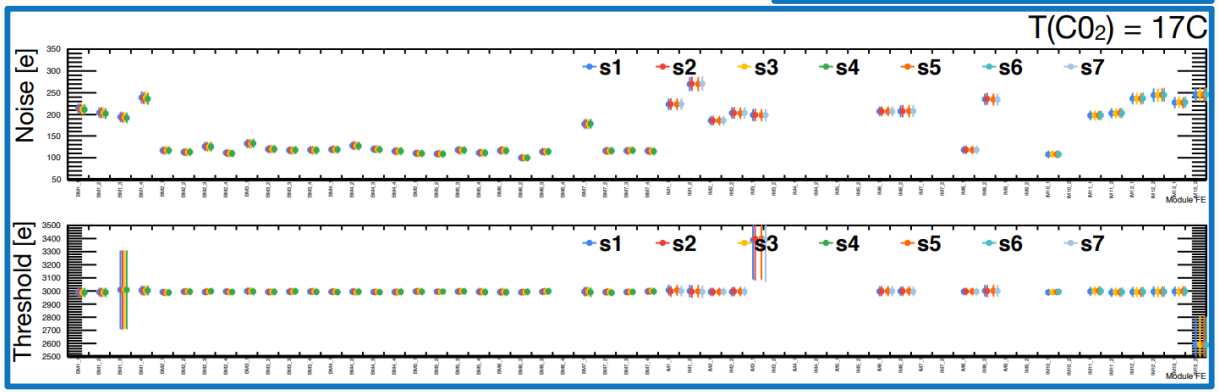


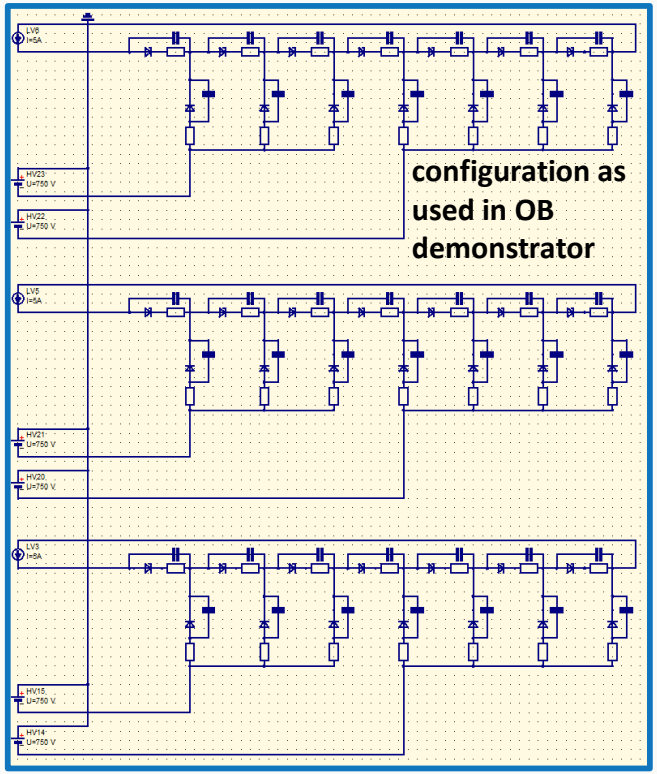
  - short chains in L0 (3 to 5 modules per chain) allow to use one HV channel per triplet
  - referencing through local module ground still to be tested

SYSTEM LEVEL CONSIDERATIONS - HIGH VOLTAGE DISTRIBUTION AND GROUNDING

- common referencing of multiple serial powering chains
  - economize usage of ATLAS MoPS chip – direct connection on PP0
  - all other serial powering chains will be electrically connected trough their low impedance tie to the ITk reference in ATLAS
  - seems to be okay for operation, although needs to be tested in combination with HV distribution scheme







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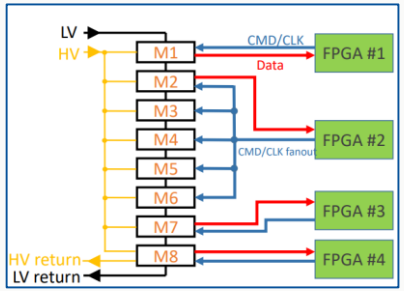
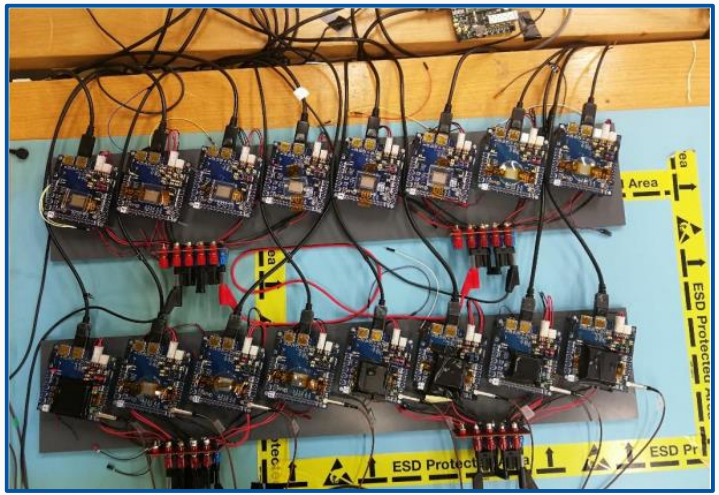
FURTHER ONGOING AND PLANNED TESTS

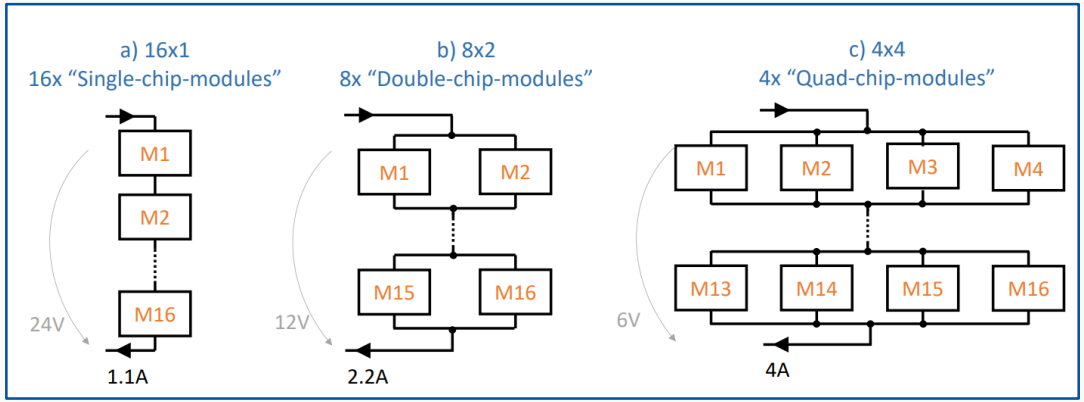
- full system level tests available only with FE-I4 prototypes so far
  - tests have revealed relevant information for SLDO and system design
- next stage of testing in ATLAS uses RD53A chips
  - SLDO regulators in RD53A have some of the same short comings as the FE-I4 SLDOs
  - CMS has tested RD53A chips in combination with RD53B-like SLDO test chips

FURTHER ONGOING AND PLANNED TESTS

- ATLAS and CMS test setup with RD53A SCC and different readout systems
  - combined 8 bare chips and 8 single chip assemblies with various sensors
  - flexible setup for testing different combinations of the 16 SCCs







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FURTHER ONGOING AND PLANNED TESTS

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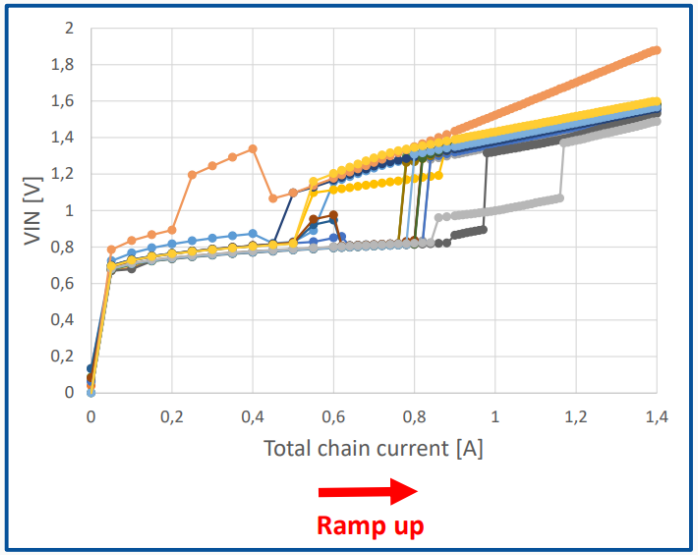
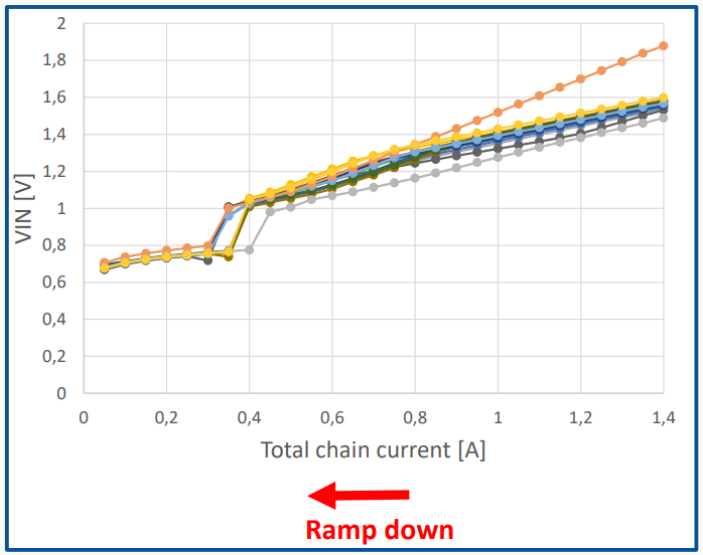
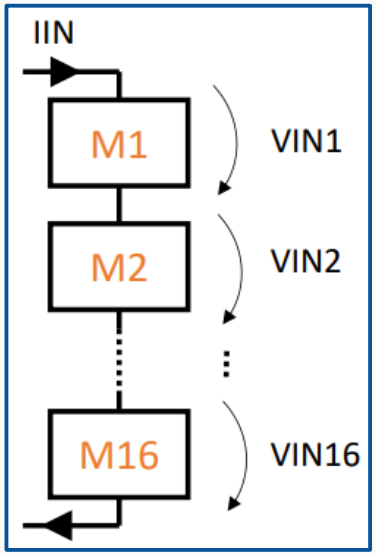
- test results confirmed previous observations
  - SLDO startup issues in RD53A – should be much better with new pre-regulator scheme in RD53B







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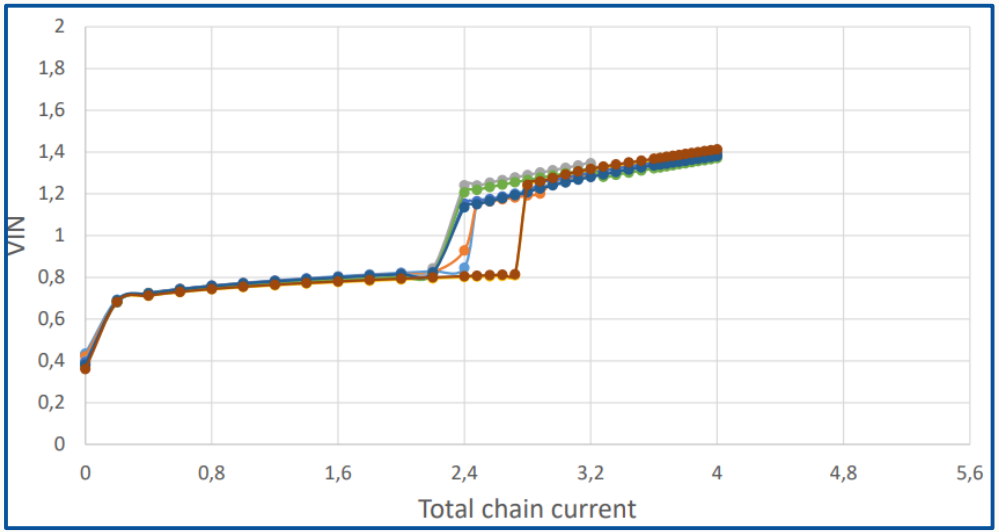
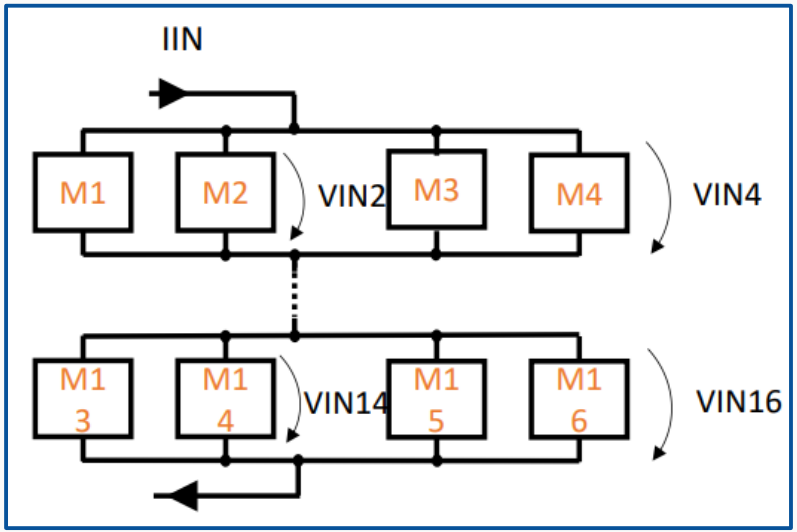
  - parallel powered SLDOs show more homogeneous startup behaviour – 'kickstart' effect





FURTHER ONGOING AND PLANNED TESTS

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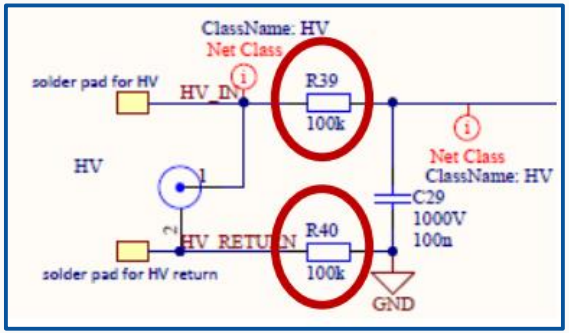
- test results confirmed previous observations
  - SLDO startup issues in RD53A – should be much better with new pre-regulator scheme in RD53B
  - parallel powered SLDOs show more homogeneous startup behaviour – 'kickstart' effect
  - currents through sensors depend on PSU off-modes in the standard HV distribution schemes

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-9.5	-3	0
2	201	-8.1	-49	0
3	196	-6.6	-44	0
4	198	-5.2	-58	0
5	282	-3.7	-1.6	0
6	313	-2.25	-1.7	0
7	284	-0.76	-2	0
8	308	0.73	162	0.6

High-ohmic off mode

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-9.8	-2.7	0
2	201	-8.4	-49	0
3	196	-7	-42	0
4	198	-5.6	-59	0
5	282	-4.15	-1.4	0
6	313	-2.72	-1.5	0
7	284	-1.304	-1.9	0
8	308	0.04	-1.2	158.7

Low-ohmic off mode



PSU behaviours emulated through open or shorted connection

FURTHER ONGOING AND PLANNED TESTS

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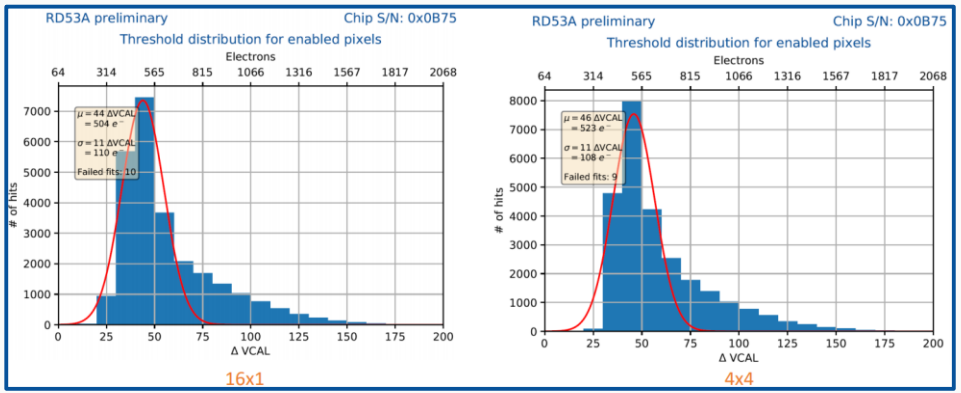
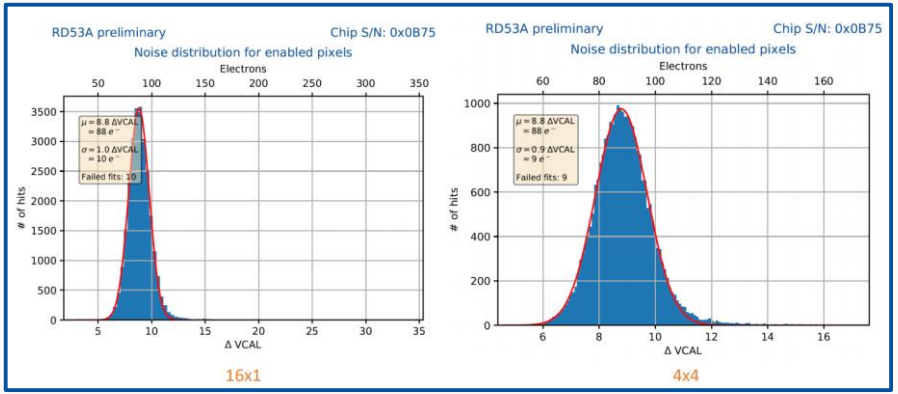
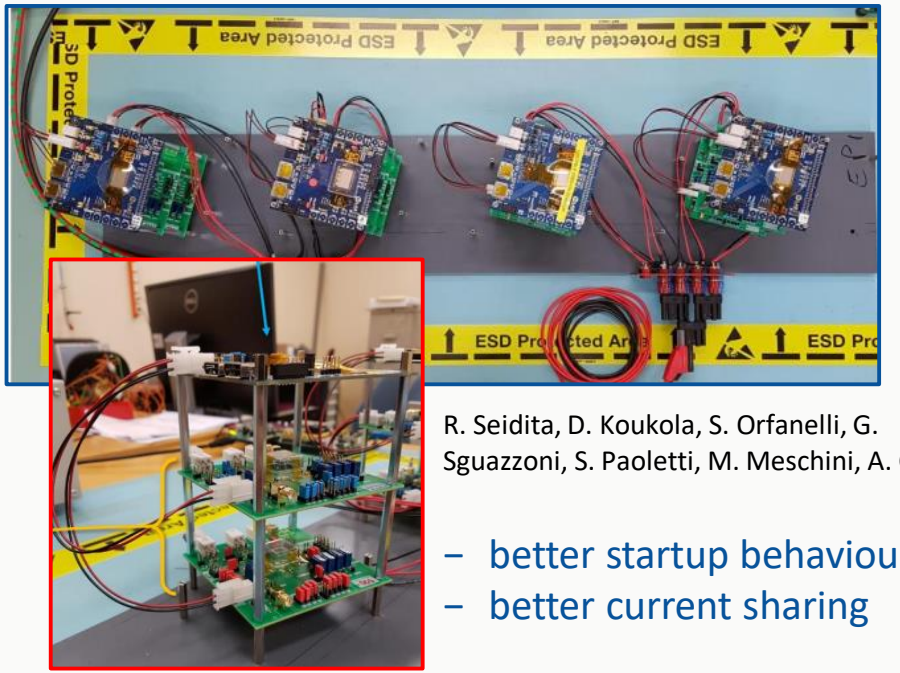
  - SLDO startup issues in RD53A – should be much better with new pre-regulator scheme in RD53B
  - parallel powered SLDOs show more homogeneous startup behaviour – ‘kickstart’ effect
  - currents through sensors depend on PSU off-modes in the standard HV distribution schemes
  - no significant difference in chip performance between different configurations





FURTHER ONGOING AND PLANNED TESTS

- CMS tested RD53A SCC chain with RD53B-like SLDOs



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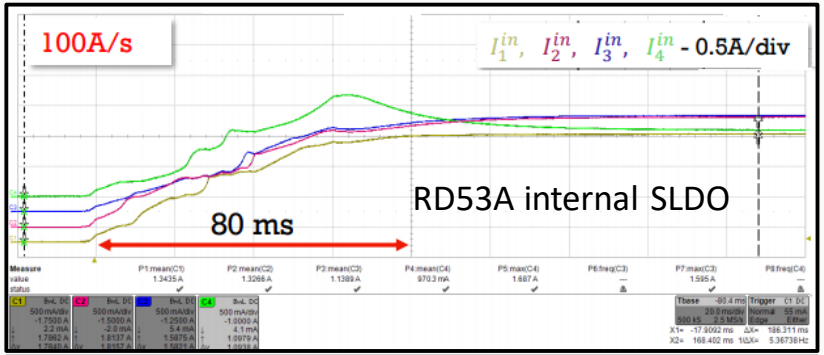
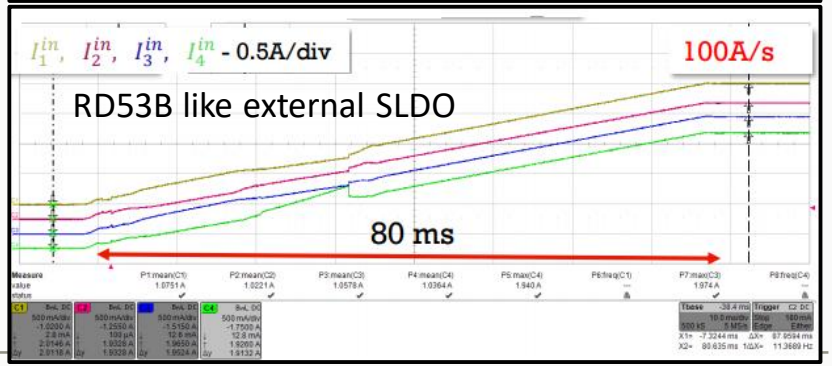
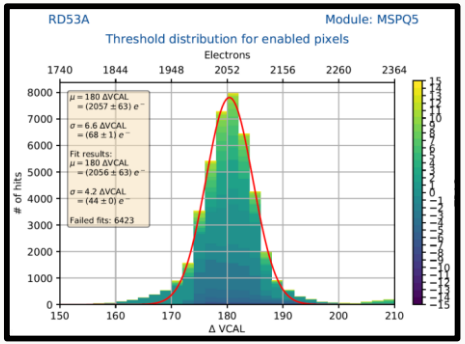
- better startup behaviour
- better current sharing

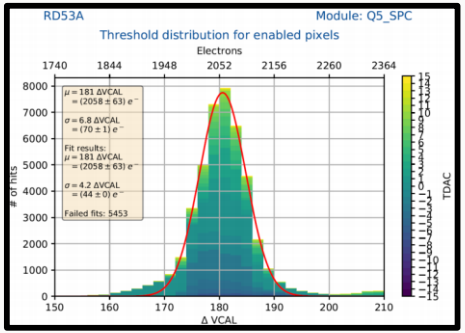


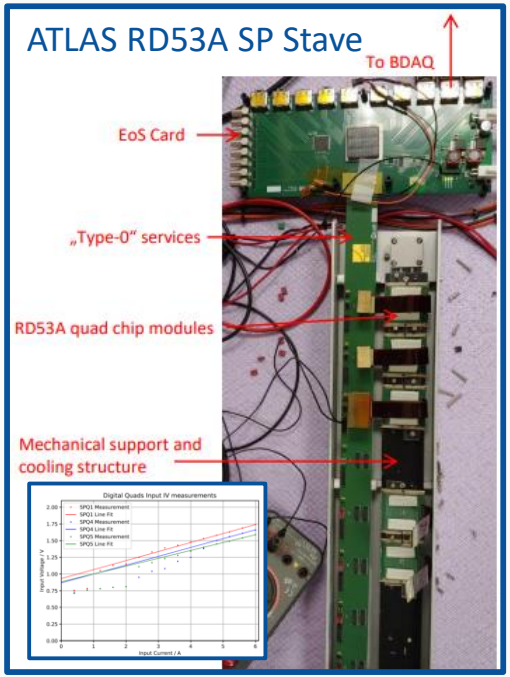


FURTHER ONGOING AND PLANNED TESTS

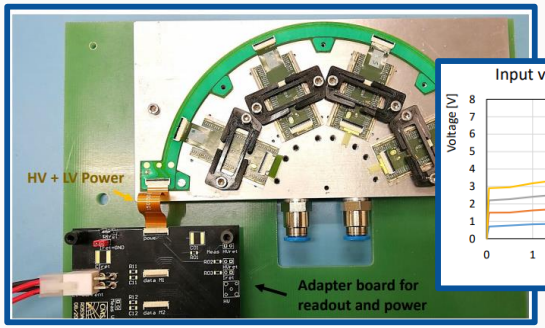
- ATLAS and CMS building larger setups with RD53A modules

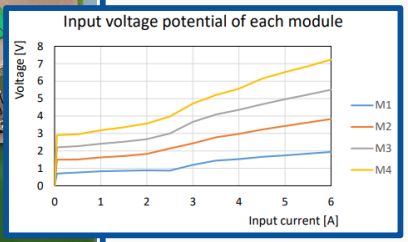


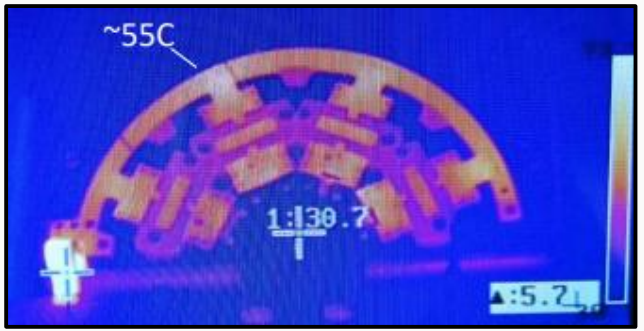




CMS RD53A Setups







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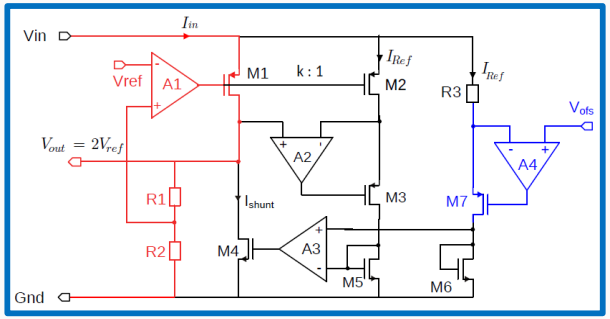
F. Hinterkeuser, M. Daas, M. Frohne, F. Huegging, H. Krueger, D-L. Pohl, M. Standke, M. Vogt, MH

System Parameter Optimisation

SYSTEM PARAMETER OPTIMISATION

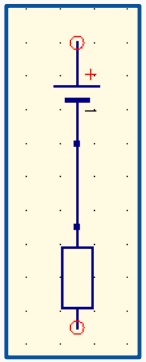
- SLDO – simplified schematic for system parameter analysis



as long as the

SLDO is operational

$$\begin{aligned} V_{\text{in}} &= V_{\text{ofs}} + R_{\text{eff}} \cdot I_{\text{in}} \\ &= R_{\text{ofs}} \cdot I_{\text{ofs}} + \frac{R_3}{k+2} \cdot I_{\text{in}} \end{aligned}$$

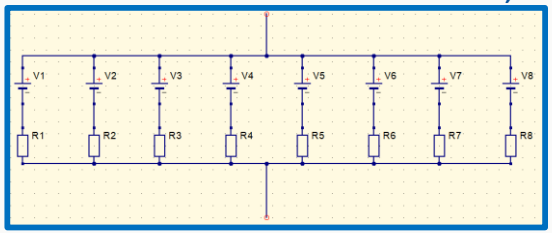


SLDO I-V characteristics in operation range determined in good approximation by 2 paramters:

→ Vofs, generated by reference current through external SMD resistor

→ Rext, SMD resistor on module flex

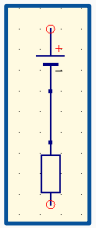
- ATLAS and CMS will be using multi-chip modules → parallel operation of several Z-diodes/V-sources and resistors – from the outside, the module looks just like one SLDO



“

$$\begin{aligned} U_1 &= U_2 = U_3 = \ldots = U_8 \\ &= V_i + R_i \cdot I_i \\ I_{\text{in}} &= \sum_i I_i \end{aligned}$$

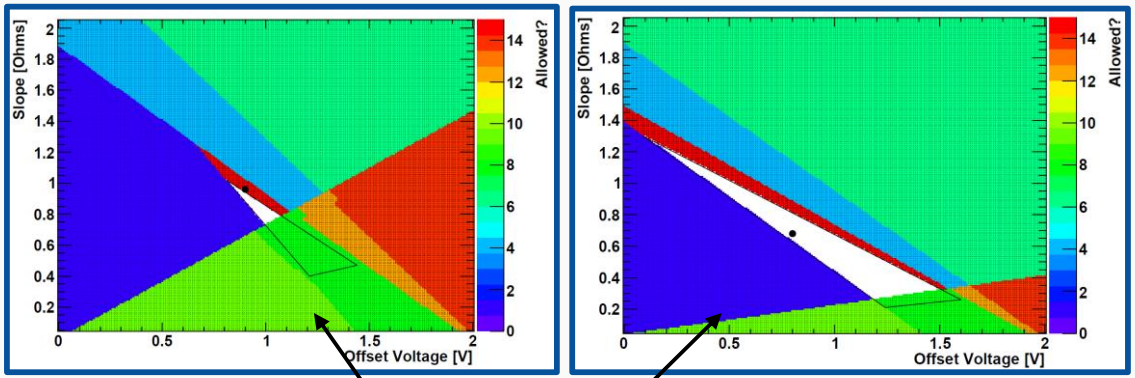
“



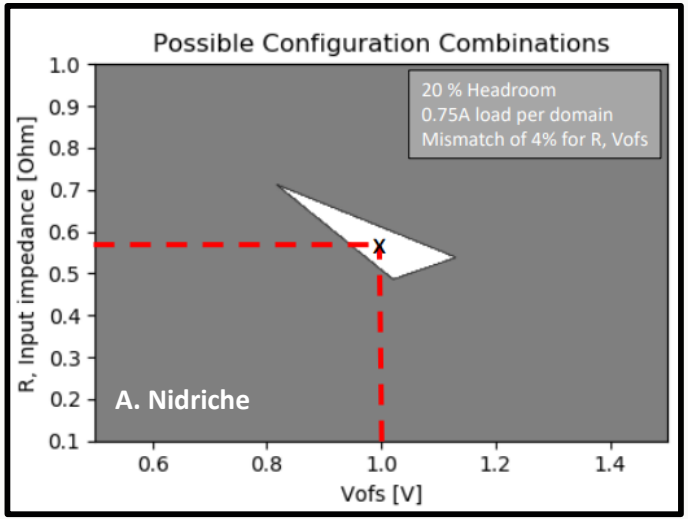
$$U_{\text{Module}} = \frac{I + \sum \frac{V_i}{R_i}}{\sum \frac{1}{R_i}}$$

SYSTEM PARAMETER OPTIMISATION

- offset voltage and slope resistance can be chosen by the value of external SMD resistors
  - which values to choose? several constraints:
    - Vin > 1.4 V
    - Vin < 2.0 V
    - local current headroom > ε
  - studies done in ATLAS and CMS



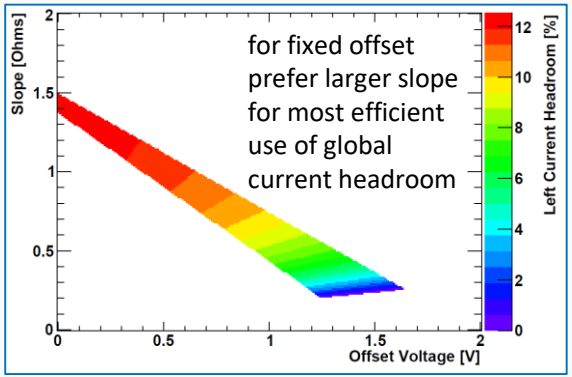
ATLAS quad chip module and triplet with 10% headroom and 1% mismatch, detailed model for current consumption in analog and digital parts

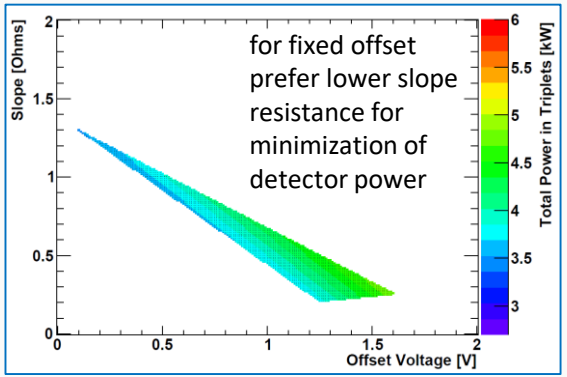


CMS quad chip module with 20% headroom and 4% mismatch

SYSTEM PARAMETER OPTIMISATION

- offset voltage and slope resistance can be chosen by the value of external SMD resistors
  - which values to choose?
  - conflicting requirements

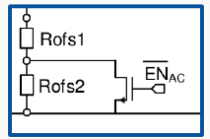




Layer	Section	Subsection	Ideal Slope Ratio Digital/Analog
L0	flat		1.16
L1	flat		1.12
L2	flat	long chain	1.06
L2	flat	short chain	1.06
L3	flat	long chain	1.00
L3	flat	short chain	1.00
L4	flat	long chain	0.96
L4	flat	short chain	0.96
L0	barrel rings		1.16
L1	barrel rings		1.14
L2	barrel rings	long chain	1.06
L2	barrel rings	short chain	1.06
L3	barrel rings	long chain	1.00
L3	barrel rings	short chain	1.00
L4	barrel rings	long chain	0.96
L4	barrel rings	short chain	0.96
L0	rings		1.12
L1	rings		1.14
L2	rings		1.17
L3	rings		1.07
L4	rings		0.96

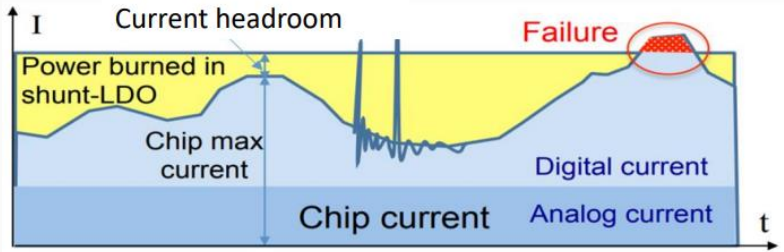
$$s_2 = (1 + s_{\text{global}})(1 - x)\left(1 + \frac{V_1 - V_2}{R(1-x)I_{\text{Module}}}\right) - 1$$

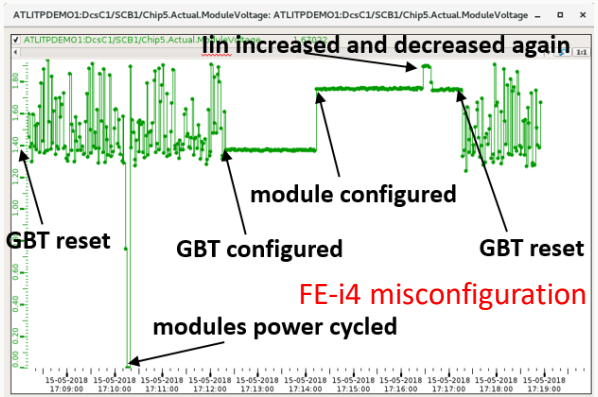
- different values for each layer in the detector?
- low power mode not so low power?

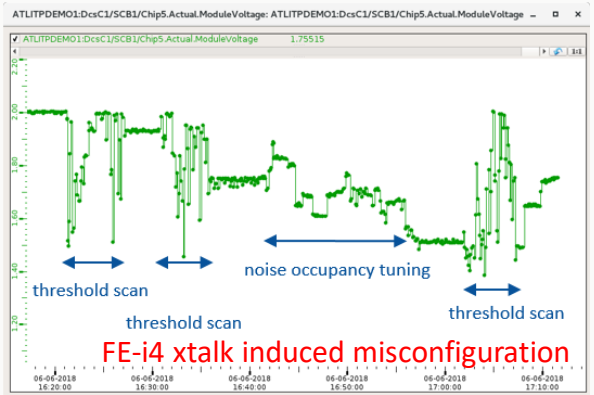


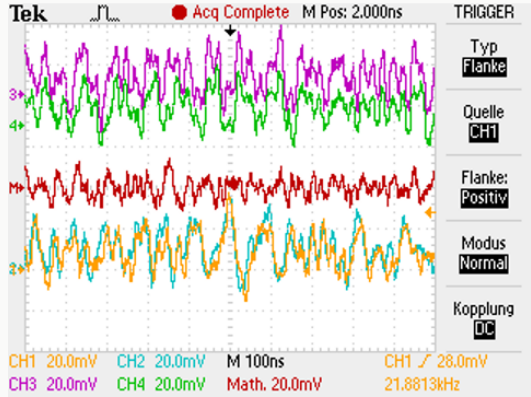
SYSTEM PARAMETER OPTIMISATION

- each FE chip will require a certain current to operate properly, this is the required current $I_{required}$
- $I_{required}$ is not constant but a function of time
- we supply a constant current for the SP chain
- if the required current is larger than the supplied current the chip won't work properly any more









SYSTEM PARAMETER OPTIMISATION

- we can only supply the total input current – the fraction that each chip gets depends on many parameters

$$I_j = \frac{I}{\sum_i \frac{R_j}{R_i}} + \frac{\sum_i \frac{V_i}{R_i}}{\sum_i \frac{R_j}{R_i}} - \frac{V_j}{R_j}$$

'true' parameters are k_i, $I_{ofs,i}$, $R_{ext,i}$, $R_{ofs,i}$

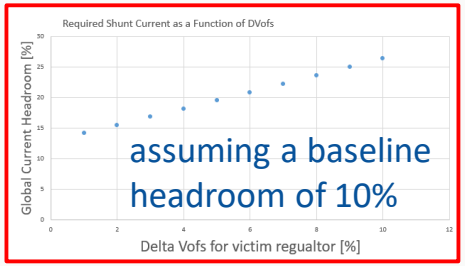
these parameters may vary

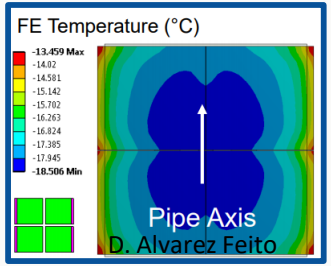
k_i, $I_{ofs,i}$: process variation, T dependence, not configurable

$R_{ext,i}$, $R_{ofs,i}$: SMD tolerances, flex PCB design and manufacturing

- we won't have perfectly balanced chips and we will not build perfectly balanced modules
  - the overall SP current headroom must handle these variations on top of the spikes in digital current consumption
  - small variations can have a significant impact on the system here

→ 10% smaller offset voltage for single regulator leads to a ~30% increase in the power dissipation in the services



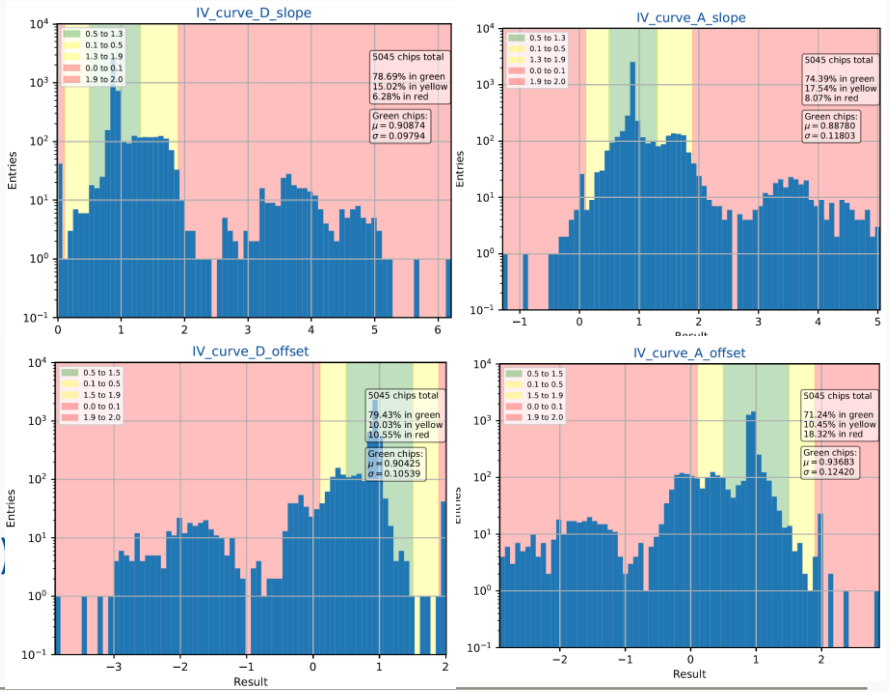


→ in most FE chips, the extra current would be shunted – only adds to the already inhomogenous power distribution

INTER CHIP VARIATIONS

- precision resistors need to be used for the offset and slope SMD components
- level of mismatch from process variation?
  - indication from waferprobing data of RD53A chips
  - variation of k-factor and offset currents significant
    - poorly matched modules with 1σ variation in either of these variables can lead to failure in poorly matched modules:
      - 1σ variation in slopes: -1.5% local headroom
      - 1σ variation in offsets: -15% local headroom
- do we have to handpick chips that go on one module?
  - don't expect this to be necessary (see improvements)
  - algorithm developed for chip matching if it is

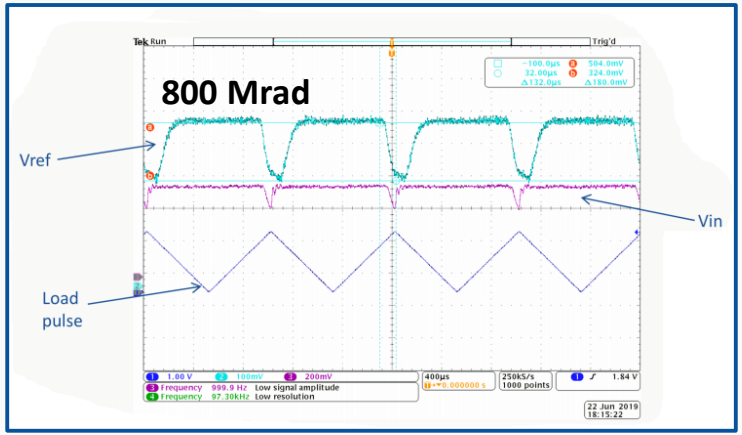
F. Hinterkeuser, M. Daas,
F. Huegging, H. Krueger,
D-L. Pohl, M. Standke, M. Vogt

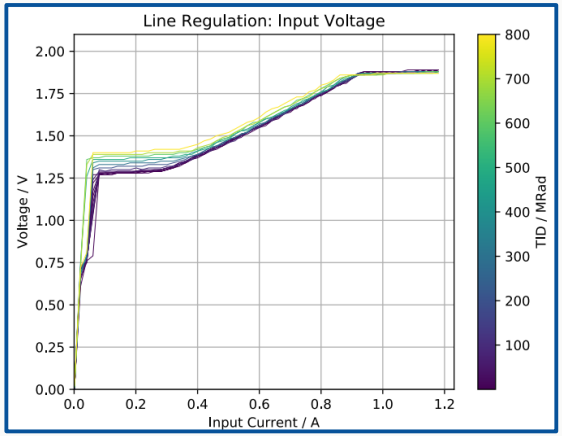


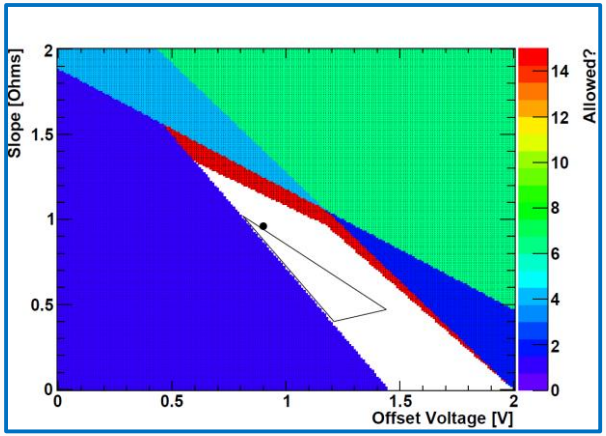
Improvements in RD53B

IMPROVEMENTS IN RD53B

- improvements we expect in ITkPIxV1/RD53B-XYZ
  - significantly improved startup behaviour, also at cold temperatures
  - undershunt current protection – should limit impact of SLDO overloading
  - overvoltage protection - caps input voltage at about 2 V
  - common offset voltage for analog and digital domains and option for common offset voltage for all chips on one module







M. Schuessler, F. Hinterkeuser, MH

Summary

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SUMMARY

- ATLAS and CMS implementations of Serial Powering Scheme very similar
  - few substantial differences, mainly for what concerns the monitoring of the running system
- evaluation of large test structures with FE-I4 done in ATLAS
  - pointed to some relevant system issues that will be tackled on the chip and system level in both experiments
- tests with RD53A chips have mostly confirmed previous findings and did not show new problems
  - CMS successfully tested RD53A chips with new SLDO test chips
- will start testing with ITkPixV1/RD53B-ATLAS as soon as it becomes available (ETA July)