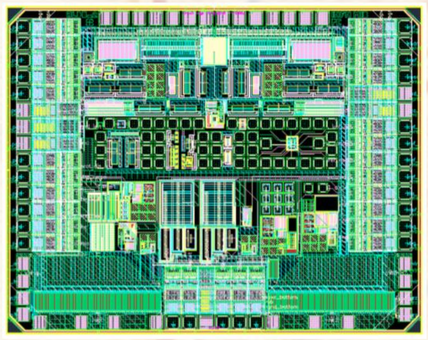
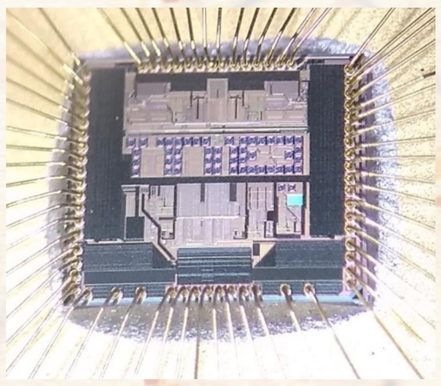
LV and bias voltage regulation for the readout ASIC and the SiPMs of the CMS MIP Barrel Timing Detector

The ALDO2 chip



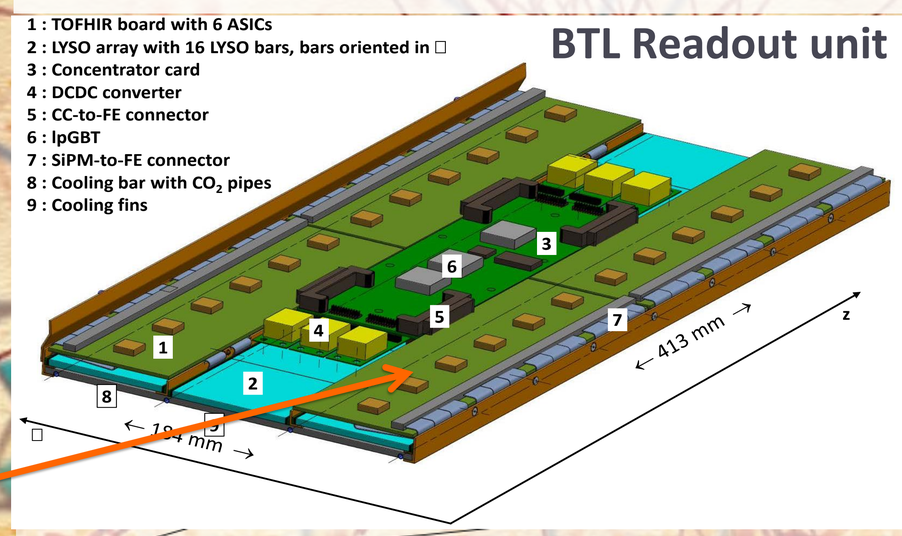


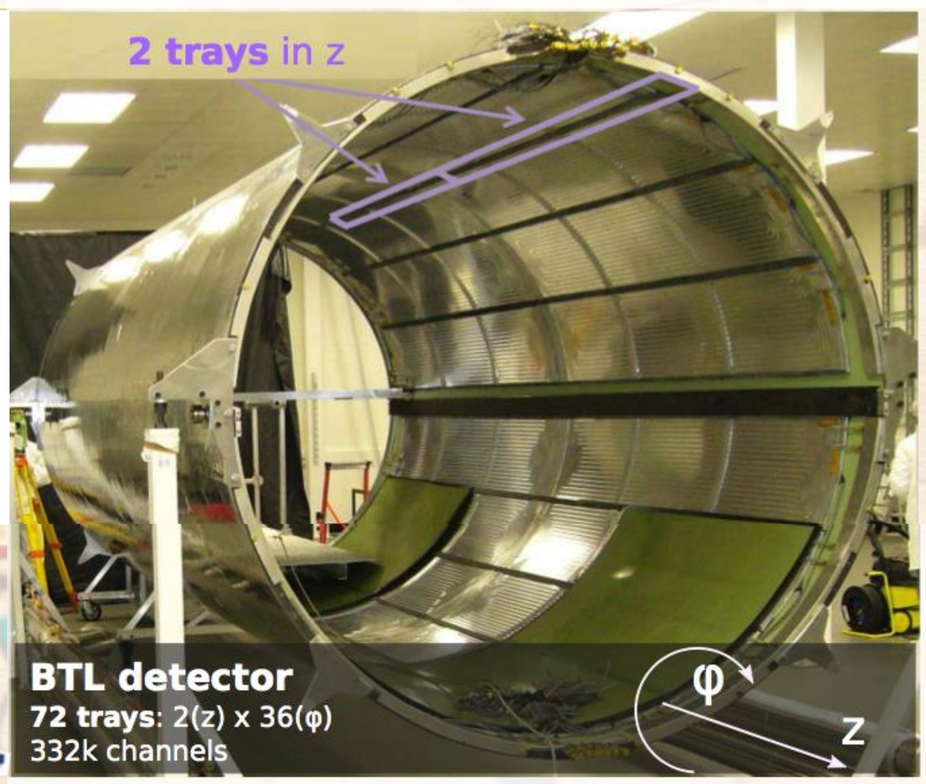
- **1 ALDO2/FE chip for LV regulation**
- **1 ALDO2/32 SiPMs for HV regulation (1 HV chan/16 SiPMs)**

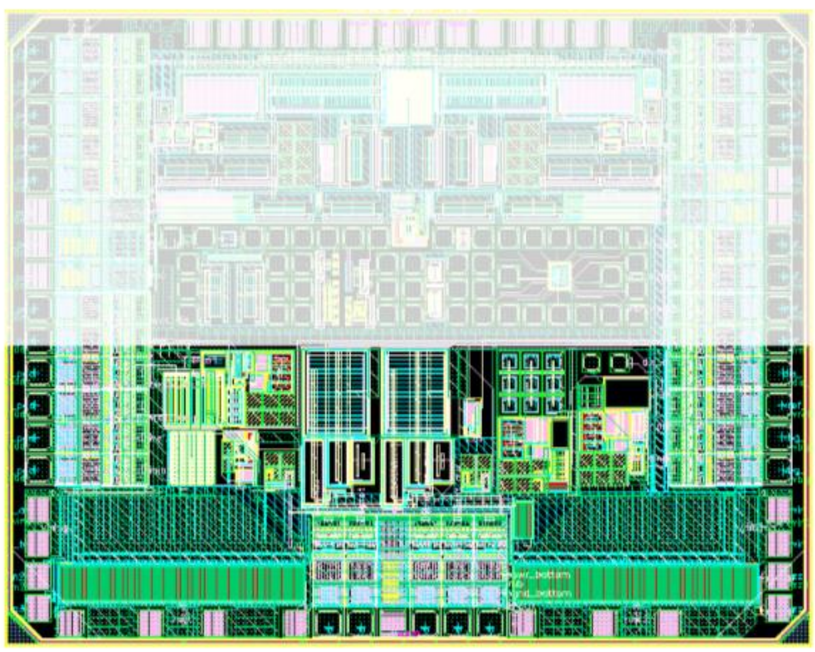
The MTD Barrel Timing Layer: LYSO bars + dual-end SiPM readout

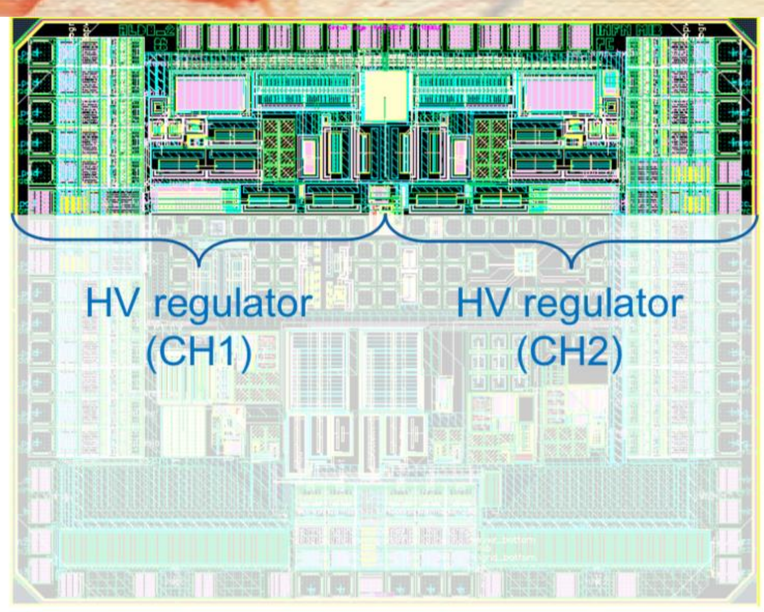
Unexplored phase-space for discoveries and precision measurements through unprecedented track-timing precision

- Fluence at HL-LHC: **1.9x10^{14} n$_{eq}$/cm^2 (3000 fb^{-1})**
- TK/ECAL interface: **~ 40 mm thick, ~38 m^2 , 332k channels**
- Mounted on the inner surface of the Tracker Support Tube









LV regulation

- **TOFHiR power supply filtering and stabilization**
- **Input voltage: 1.6 V – 3.3 V**
- **Power efficiency: 67 and 75% for input at 1.8 and 1.6 V**
- **PSRR >40 dB and stability <50 ppm/°C**
- **2 channels:**
  - Main regulator: 500 mA output;
  - Aux regulator: 20 mA output
- **3 bandgap voltage references:**
  - 2 based on BJTs
  - 1 based on MOSFETs

HV Regulation

- **Input voltage: 10 V – 70 V**
- **Output voltage adjusted using DACs on TOFHiR**
  - Range 1: 100% – 75% of input voltage with 0.1% LSB (8 bit)
  - Range 2: 100% – 87% of input voltage with 0.05% LSB (8 bit)
- **Maximum output current: 25 mA**
- **Channels can be individually disabled**
- **Allows output current measurement by mirroring**

External low ESR capacitor for stability

Protected against over-current and over-temperature

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on behalf of the CMS MTD project