Developments on the Tile Computer on Module (TileCoM) mezzanine board for the ATLAS Tile Calorimeter off-detector electronics

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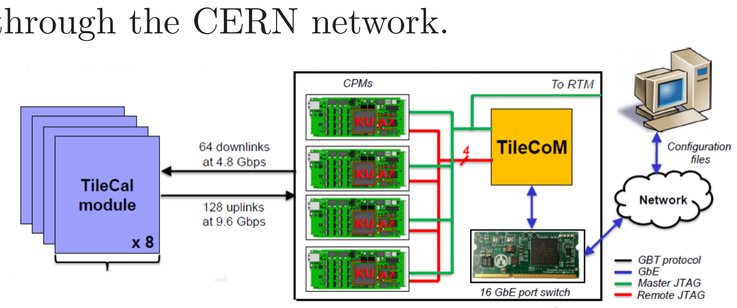
Abstract

The Tile Computer on Module (TileCoM) mezzanine board is one of the auxiliary boards of the Tile PreProcessor (Tile PPr) for the Phase-II Upgrade of the readout electronics of the ATLAS Tile Calorimeter. The TileCoM will be responsible for remotely configuring the on-detector electronics and TilePPr FPGAs as well as to interface ATLAS DCS data to the Tile PPr. The TilePPr is composed of several FPGA-based boards to operate and read-out the on-detector electronics. This contribution presents the deployment of an embedded Linux for the ZYNQ System-on-Chip (SoC) targeting an Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board. This test bench will serve as a basis for the development of the main functionalities of the TileCoM mezzanine board and the remote programming of the FPGA devices of the Tile Calorimeter.

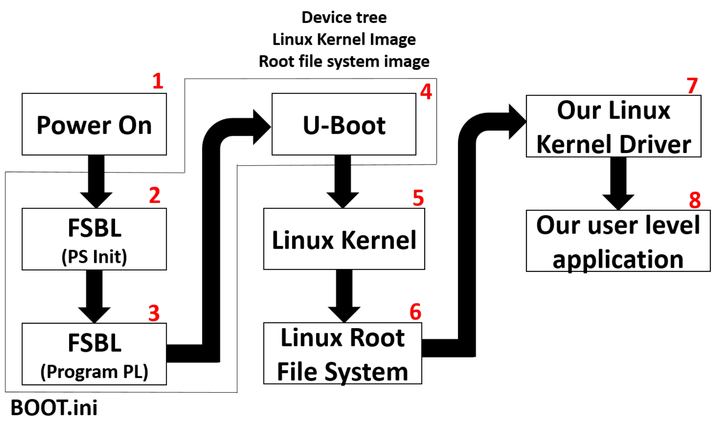
Tile Pre-Processor (TilePPr)

The TilCoM is used to remotely configure and program the on and off-detector electronics FPGA. To be able to access the TileCoM and perform this operation through the network, the TileCoM is connected to the Tile 16 GbE port switch that is used to access the TileCoM through the CERN network.



TileCoM Embedded Linux

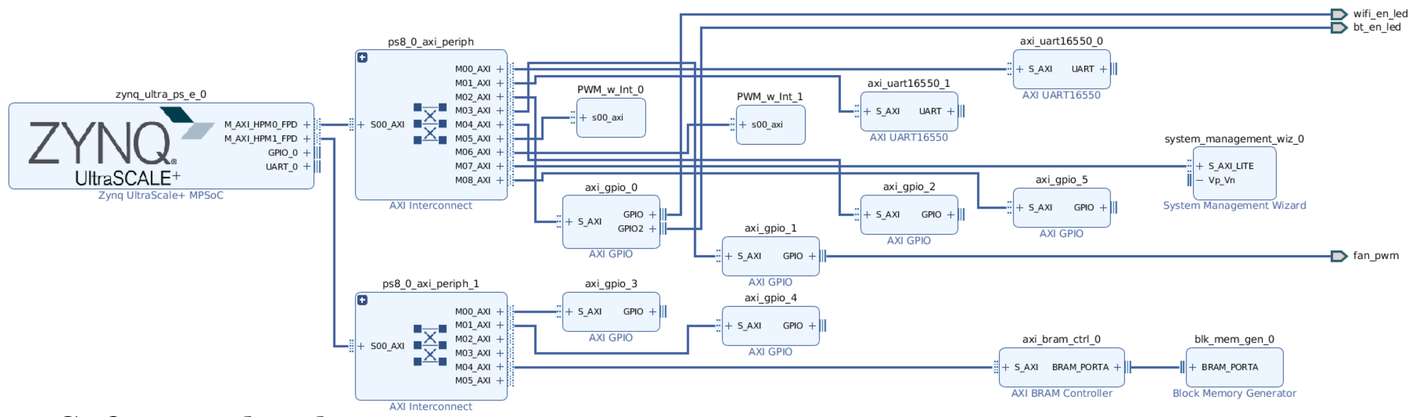
CentOS 7 embedded Linux was deployed on the ZYNQ System-on-Chip (SoC) targeting an Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board. The boot files for the embedded linux were created using petalinux and the root files were created using yocto tools.



Firmware and software developments for remote programming

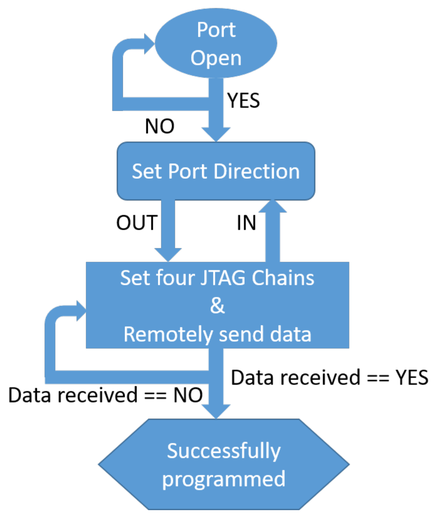
The XVC protocol allows the Vivado design tools to communicate JTAG commands over Ethernet to an embedded system so that a target Xilinx FPGA can be programmed and/or debugged. This solution can be used to program and/or debug more than one FPGAs in parallel. Although XVC can be implemented with several different processors, this application note provides design utilizing Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board. GPIO ports are used in the design as virtual TCK, TMS, TDI and TDO.

1. Firmware development:



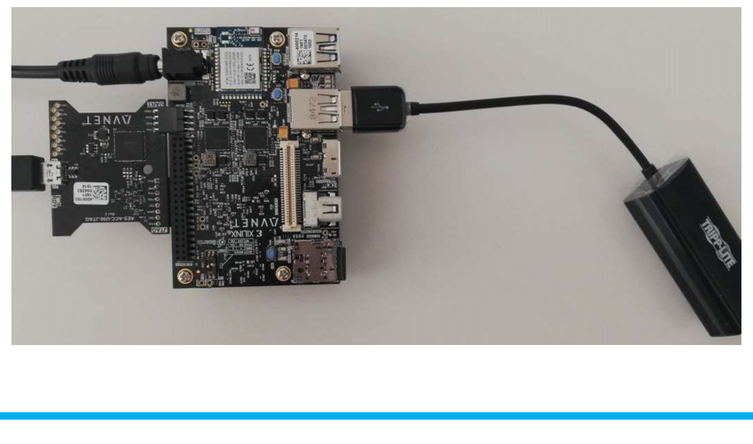
2. Software development:

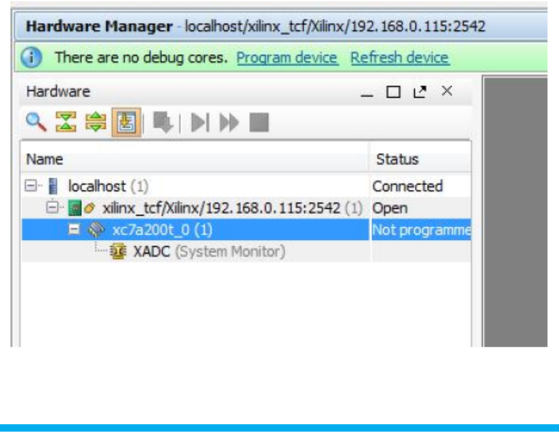
The software application was developed and implemented on the Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board to access the virtual ports through the GPIO Sysfs Interface using C language. Xilinx SDK version 2019.1 tools were used to debug and implement this software on the evaluation board. The application software handles the setup of the TCP/IP socket as well as communication with the GPIO to JTAG Controller. The Ethernet payload from the socket is accepted, parsed, and stored in buffers. The first bytes out of the socket indicate the commands. The XVC Protocol only has three commands namely; getinfo and shift and settck for transmitting data.

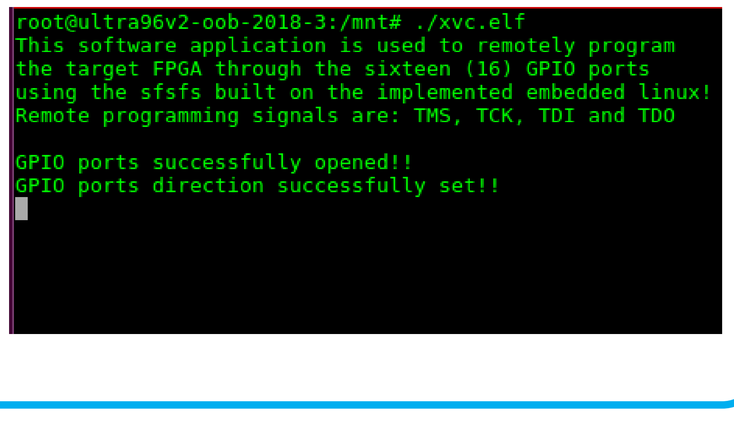


Experimental Results

Test results involved detection between the virtual GPIO ports and real JTAG ports on the Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board.







Summary and Acknowledgement

Communication between the virtual and real JTAG ports proved that the firmware and software development are working successfully on the Avnet Ultra96-V2 Zynq UltraScale+MPSoC evaluation board. The current work focus on the developments of the IPbus software and firmware development in order to integrate with OPC UA Server in DCS. A special gratitude to the South African government, NRF and iThemba labs for funding this project.

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