sFGD board readout

Draft for specifications

LLR/UniGe group

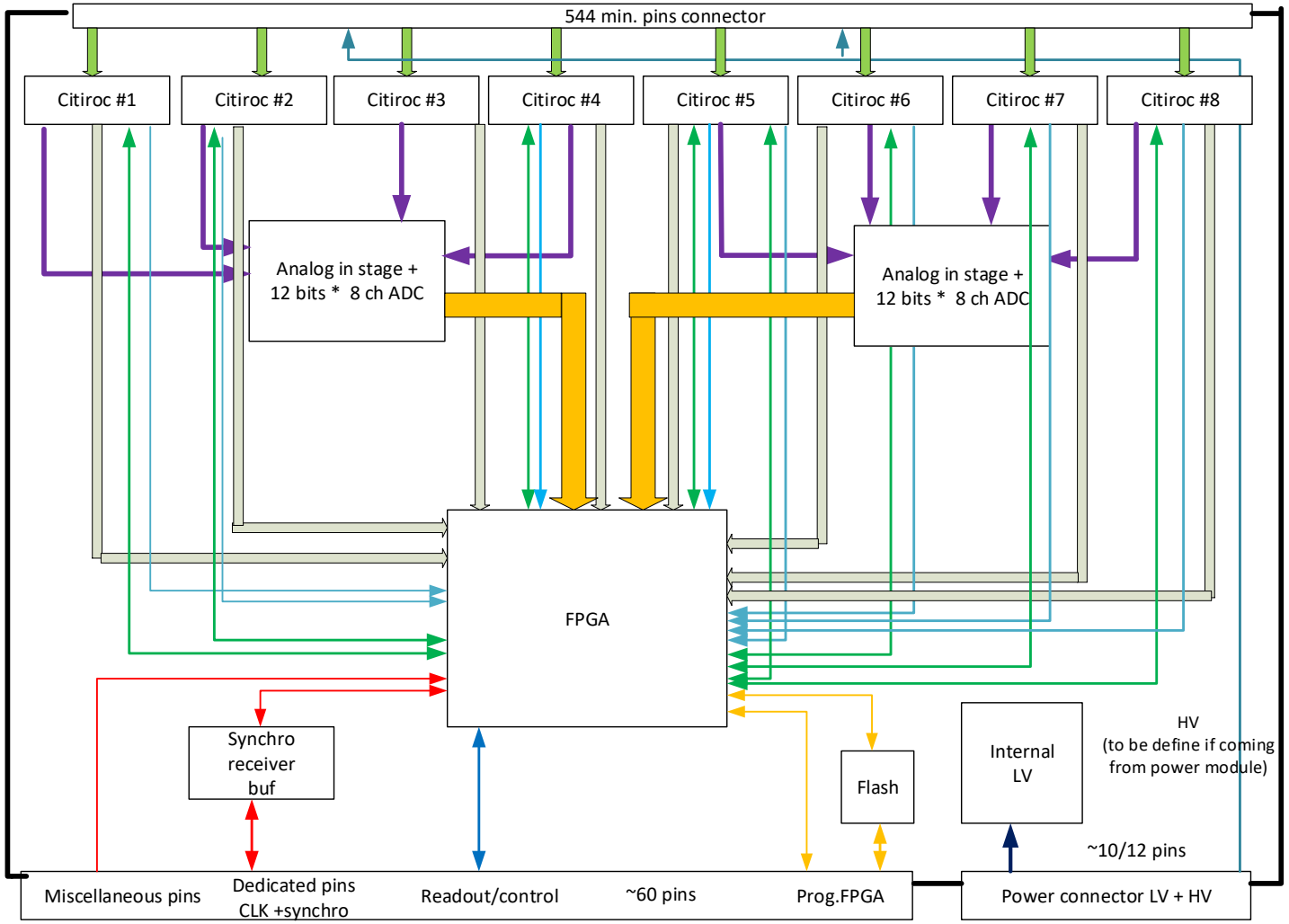
Context (1/2)

- That is following based on Baby Mind project and it's a starting point for sFGD
  - The electronics for this board(FEB) is based on the CITIROC developed by Weeroc Microelectronics group.
  - Environmental conditions :
    - Confined space for the board (constraint of dissipation) and Magnetic field in the order of 0.2T maximum.
  - The FEB will be installed on the Left and right side of the detector.
    - Left : 111 boards
    - Right : 110 boards
  - Size of the board : 6U
  - Nbr of crates / sides : 8 (2 rows x 4 columns) –> *Must be confirmed*
  - Nbr FEBs/crate/side : 14 (*rounded value*)
  - Nbr of CITIROC/board : 8
  - Nbr ADC /board : 2 (same ADC than Baby Mind : AD9637, 8 channels ADC)
    - Low Gain and High Gain signals from CITIROC
  - Main FPGA : ARRIA 10 (10AX057)

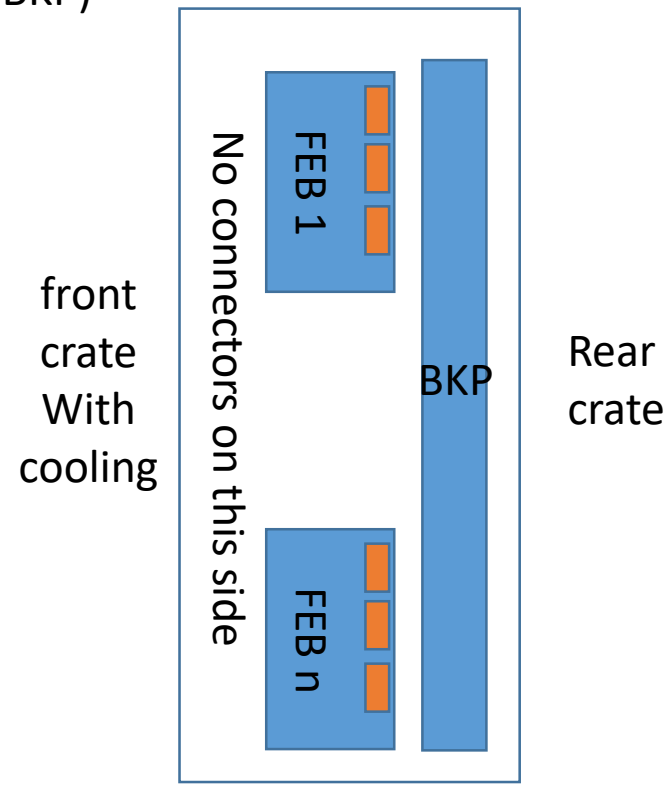
Context (2/2)

- DAQ system architecture
  - Each FEB are connected in point to point to the optical board (serial link) Must be confirmed
  - A protocol must be put in place – readout & slow control
    - UDP, Baby-Mind protocol ? Open question
  - CITIROC are connected in deasy-chain on the board for the slow-control part (configuration)
  - Synchronisation (same as baby-Mind ?): Clock line (value : 100Mhz), reset, trigger, spill start/end, Frame Synchronisation.
- Power distribution
  - Low voltage : based on DC/DC and LDO
    - For DC/DC : some issue must be resolved (magnetic field, inductor)
  - HV : question : is it supply thru FEB or not ?

Preliminary overview of FEB architecture



Remark : the 3 connection zone will be implemented on the same side on the FEB. (Connection to the BKP)

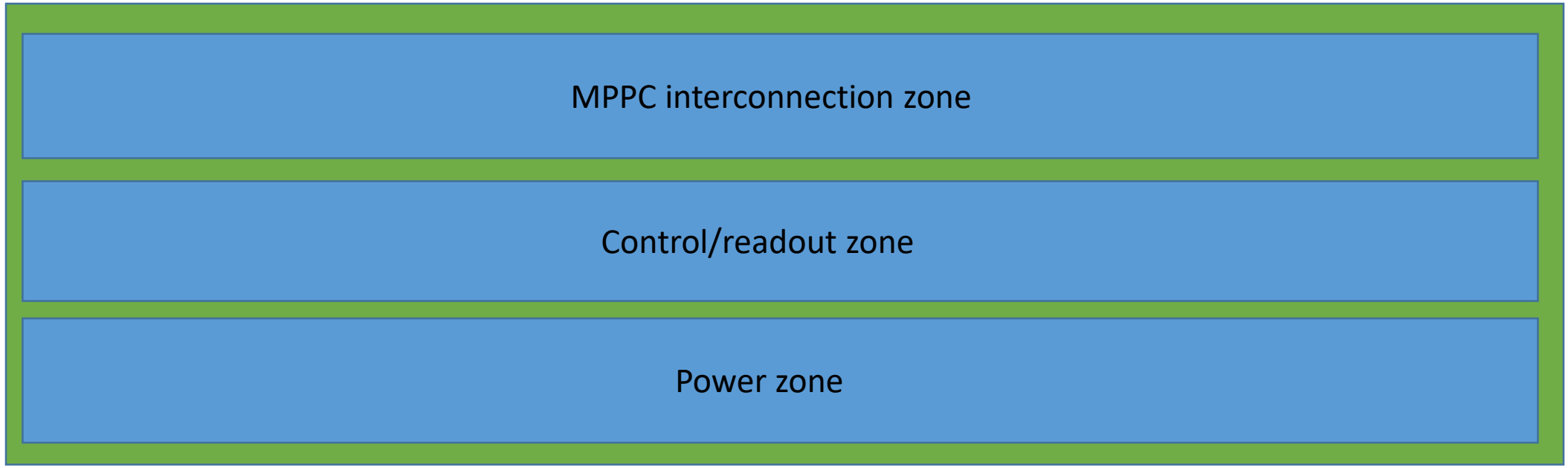


Backplane slots (reflexion)

Who take it in charge ?

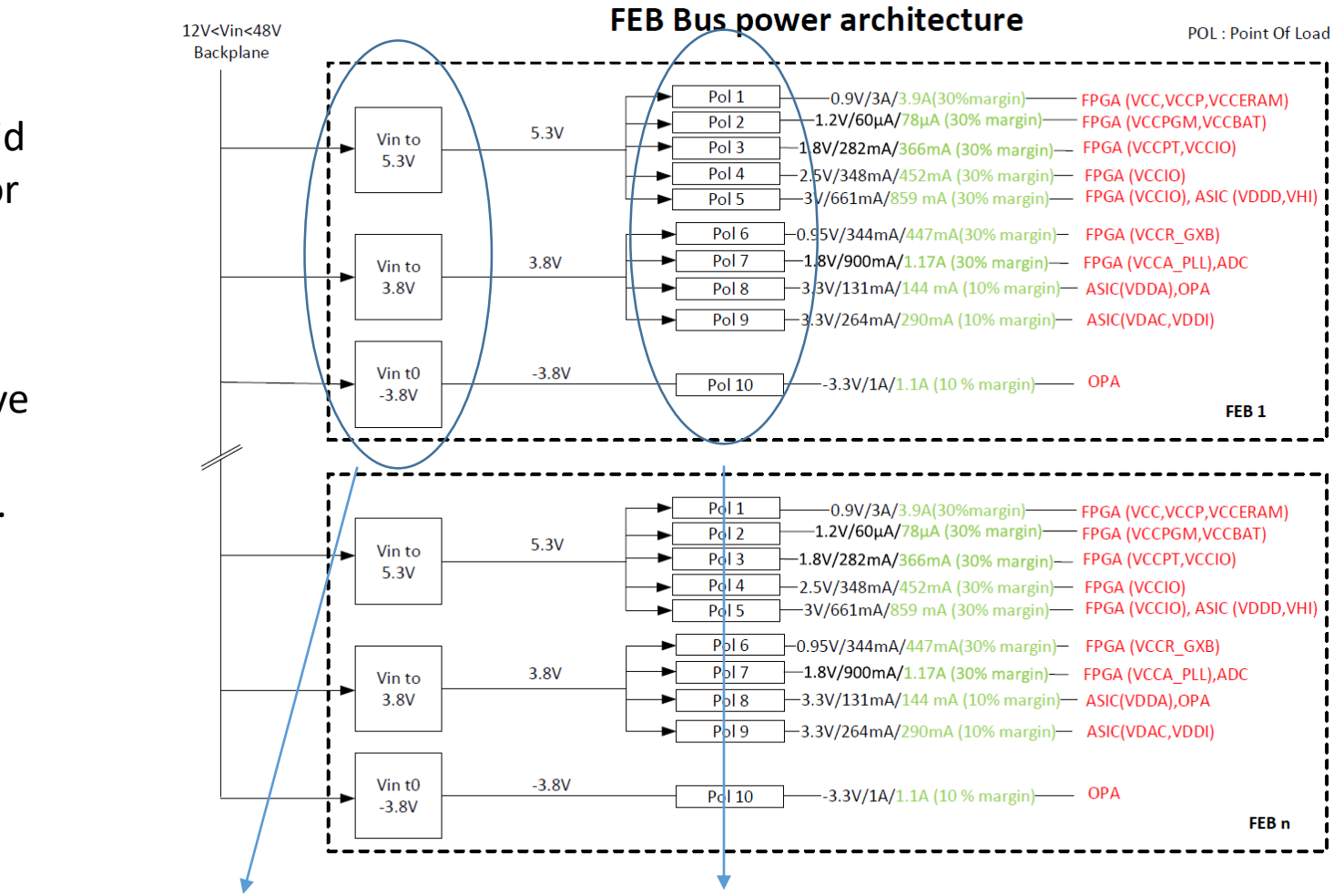
- 1 slot/crate for optical module
- 14 slots/crate for FEBs

On BKP each part (zone) will be separated with the others
Each slot will have a harcoded value (14 slots : 4 bits) and added 3 or 4 bits with jumper or other to coded the bkp number.



Low voltage

New topology
After last meeting and discussion we have decided to remove a power module to avoid supply a high current thru the backplane for each FEB.
In this case 2 solutions (idea) about DC/DC were investigated.
1 – CERN FEAST DC/DC : forget – advice give from CERN for our project – Du to the low efficiency compare to a commercial DC/DC.
I have not more details
2 – Commercial DC/DC:
Main investigation: air core inductor (magnetic field)
Issue : value less than 1µH , needs 3µh or more.
Need to find and simulate or test with an evaluation board the behavior with an inductor <1µH. (Check the efficiency)
Texas Instrument and Linear Technology have this kind of simulation tools

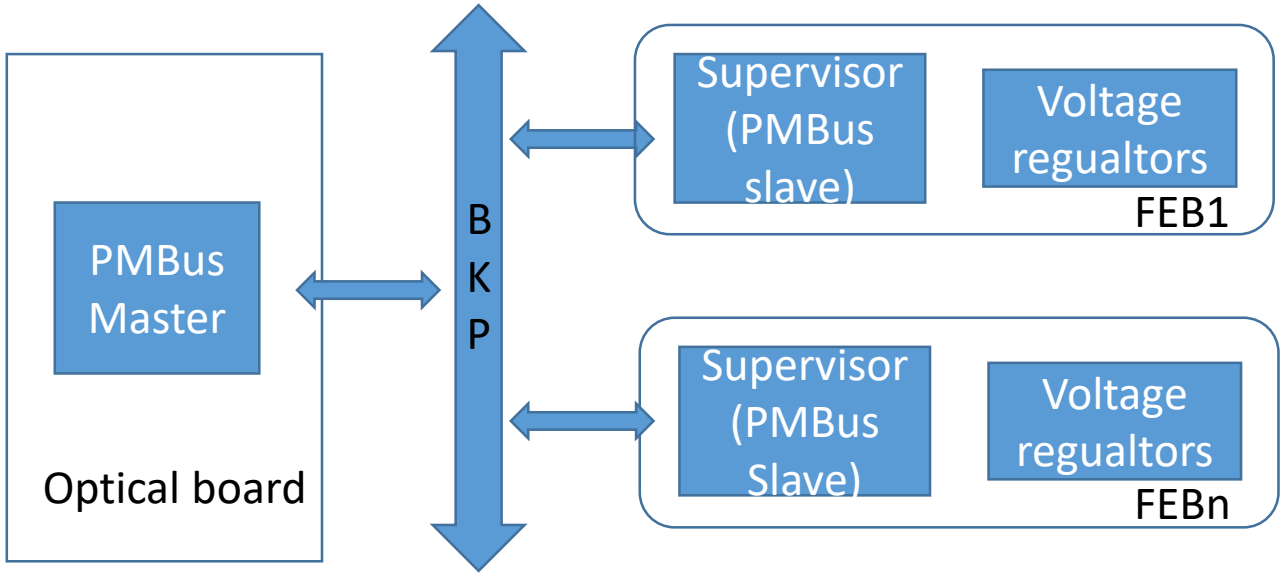


These blocs contain a DC/DC converter These blocs contain DC/DC and LDO

Others topologies are possible

Supervisor & sequencer chip

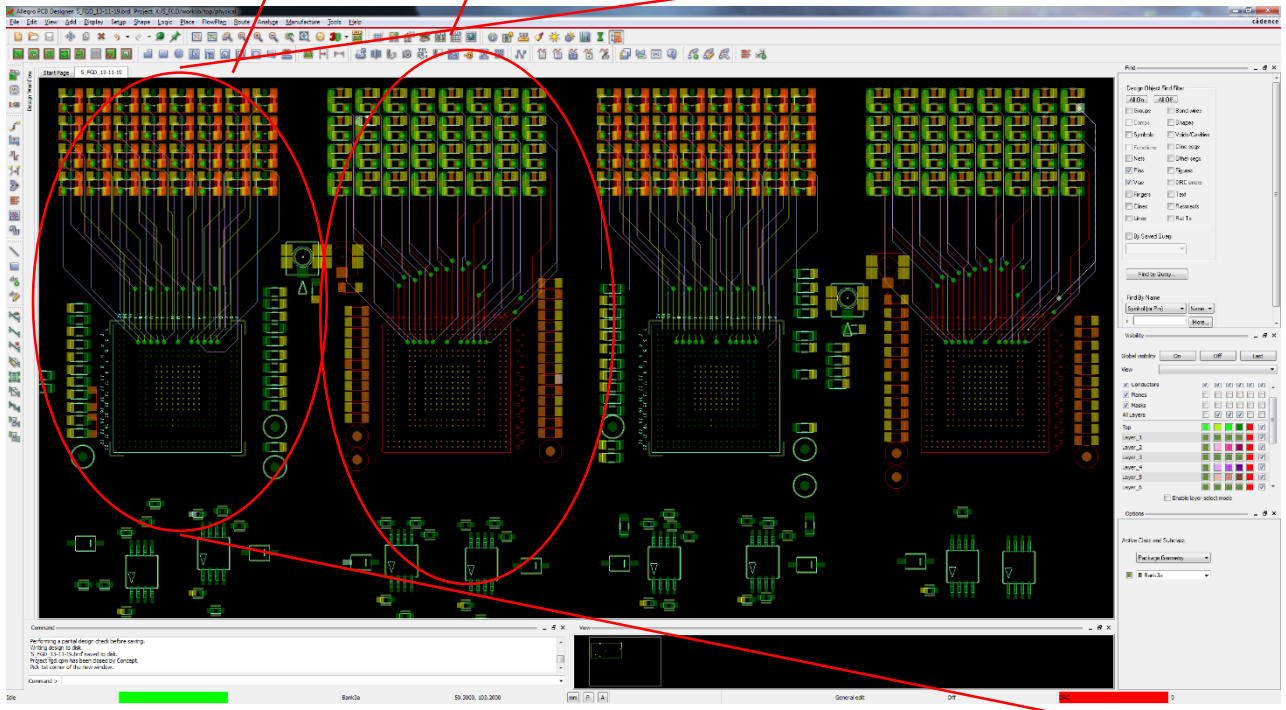
- Supervisor chip
  - FPGA needs ~7 low voltages
  - Monitor current, voltage and if possible temperature
  - Can sequence the start and stop FPGA supply voltage
  - This chip have a PMBus/I²C compatible interface (UCD90120A or others)



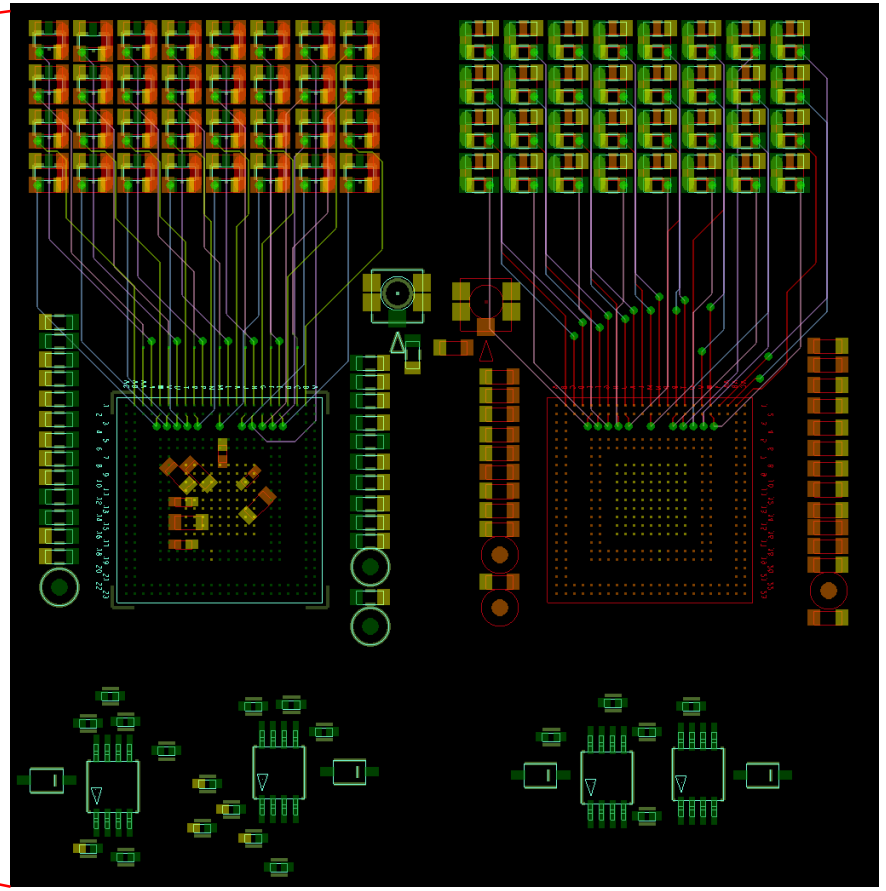
Preliminary Layout on ASIC

Top

Bottom



No near channels routed on the same layer
Currently : Distributed over 5 layers but not yet fixed



Layout: overview of the components placement

Backplane side

cooling side

Start layout: 10 layers

Possible placement of DC/DC converters

Rating of low voltage regulators placement