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Performance Simulations of High-Speed, Low-Bit Resolution Analog-to-Digital Converters

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Direct digitization of signals at low-bit resolution can be realized directly using FPGAs, allowing for systems that have very high channel density, and more information bandwidth than simple discriminator-based designs. Such systems may be a good candidate for high channel density, low power, integrated readouts for future high energy physics applications. We have studied such systems at 3- and 4-bit resolution, running at sampling rates of 1 and 2 GSPS, consistent with designs that can be implemented on low-cost FPGAs. In particular, we will present the simulated performance of such systems on silicon photomultiplier data, focusing on pulse height and timing resolution. We will also discuss the analysis algorithms, and progress on adapting them for realtime implementation in experimental systems.

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