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The Terabit Readout Architecture for the LHCb VELO Upgrade

Thursday 28 May 2020 11:18 (18 minutes)

The current Vertex Locator (VELO) detector will be replaced from strips to pixels in the LHCb upgrade in 2020. This work focuses on the architecture of the readout chain and the challenges of the high speed data transmission and processing. The readout is divided in 3 parts: frontend VeloPix ASIC, the control and timing interface ASIC (GBTx), and the the FPGA backend board. The VeloPix is a new radiation hard, high speed ASIC with specific data transfer protocol. The highest occupancy ASIC will see 900 Mhit/s adding up to 4 Tb/s for the whole detector. The detector is placed in a retractable system in vacuum at an extremely high radiation environment. The data transmission at 5.13 Gb/s is performed through low mass and flexible links, which underwent a long simulation and testing campaign. The backend board must collect and time order data from different frontends sending them to the high level trigger at 100 Gb/s, where the full event reconstruction occurs.

Funding information

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