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The CMS Data Acquisition System for the Phase-2 Upgrade

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During LS3, the CMS Detector will undergo a major upgrade for the Phase-2 of the LHC physics program, starting around 2027. The upgraded CMS detector will be read out at a data rate of up to 50 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size of 8 MB. We present the baseline design of the DAQ.

A DAQ and Timing Hub (DTH) board acts as an interface between the synchronous clock-driven domain of the back-end electronics of the sub-detectors and the asynchronous data-driven domain of the the networking and processing equipment for the event building and selection.
The design of the DTH in ATCA standard and measurements with the prototype board will be presented. Results will be presented on the data flow from aggregating back-end electronics end-points into sub-events and transfer over simplified TCP/IP from the FPGA in to multiple 100 Gbps Ethernet network ports and PC hosts, and subsequent event building with RDMA over Ethernet.

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