

Integrated Readout Electronics for Large Area Picosecond Photodetectors

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Large Area Picosecond Photodetectors (LAPPD) are a new generation of microchannel plate photomultipliers. LAPPDs use 28 stripline anodes to give 1-3 mm spatial resolution via fast timing at low channel density. We have developed extremely compact and low-power electronics that mate directly to LAPPD tiles. An FPGA controls readout and parallel digitization of 2x28 channels, sampled by DRS4 switched-capacitor array ASICs. This fast data pathway is multiplexed with a slow control pathway operated by a soft-core processor. All data flows over a single commodity Gigabit fiber using standard UDP and IP protocols. An open-source ecosystem for firmware, embedded software, and DAQ has been developed, providing complete control of the device and “plug and play” operation within existing environments and commodity hardware. In this report, we describe our project status and report results from the first tests mated to an LAPPD tile.

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