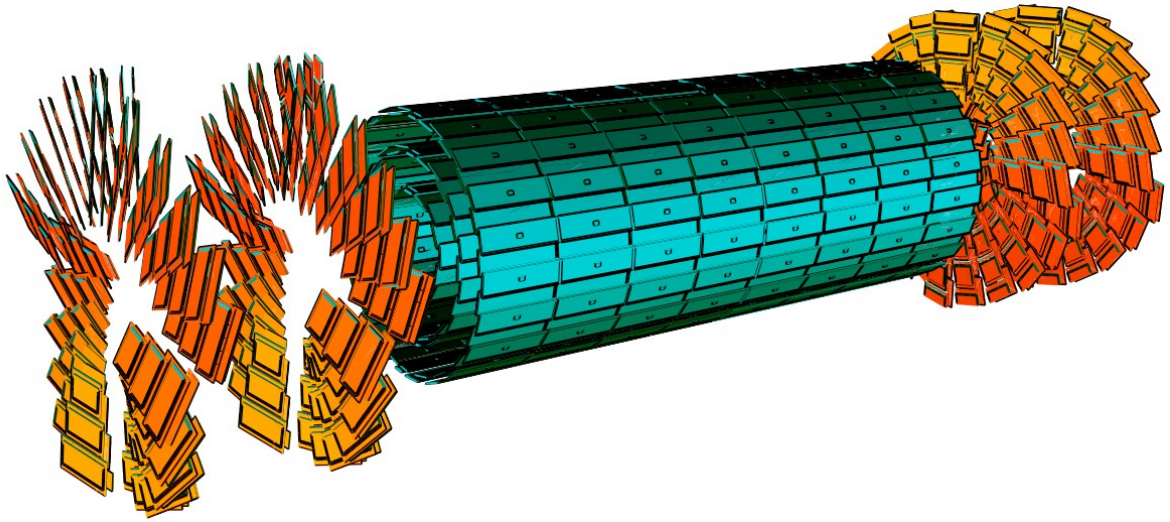
The Design, Construction & Performance of the CMS Pixel Detector

Danek Kotlinski/PSI

Vilnus, 28/11/2019

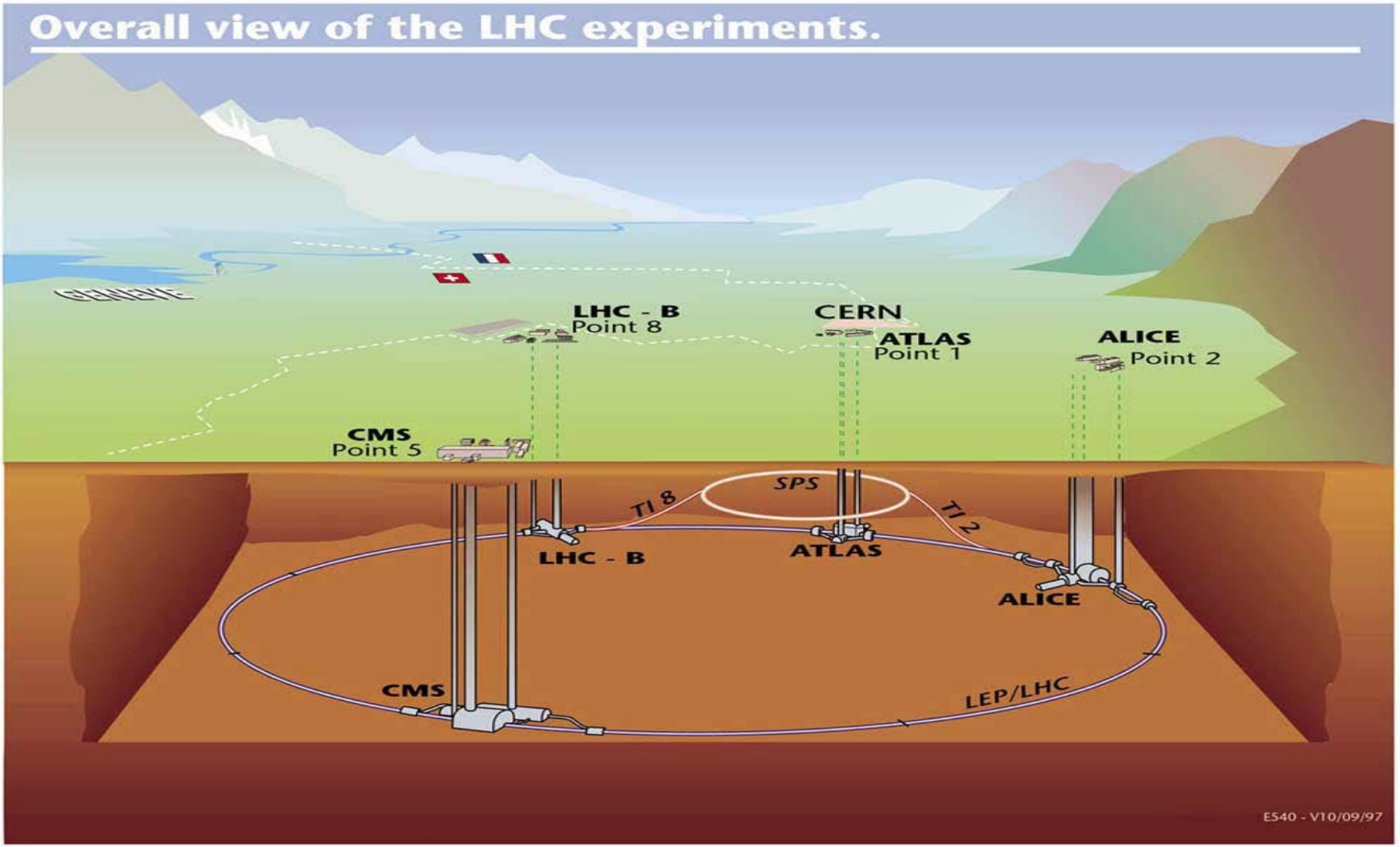


Content:

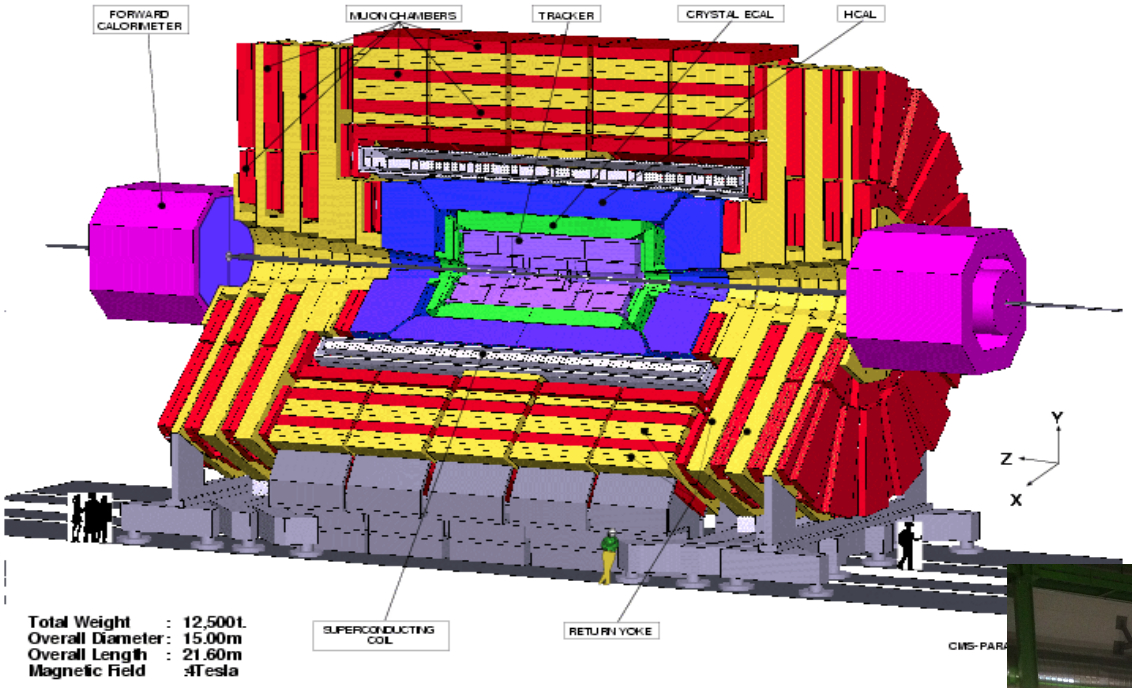
1) Introduction
2) Design
3) Construction & Performance
4) Upgrades
5) Future detectors

Introduction

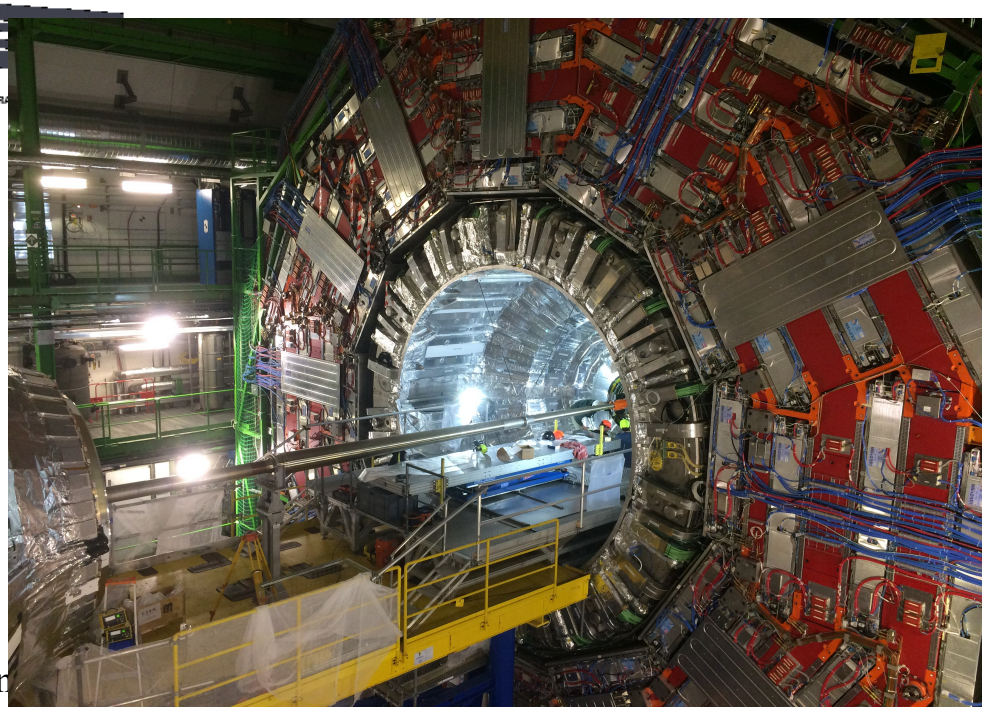
LHC/CMS


Overall view of the LHC experiments.
GENEVE
LHC - B
Point 8
CERN
ATLAS
Point 1
ALICE
Point 2
CMS
Point 5
SPS
TI 8
TI 2
LHC - B
ATLAS
ALICE
CMS
LEP/LHC
ES40 - V10/09/97

The CMS Detector



A sketch

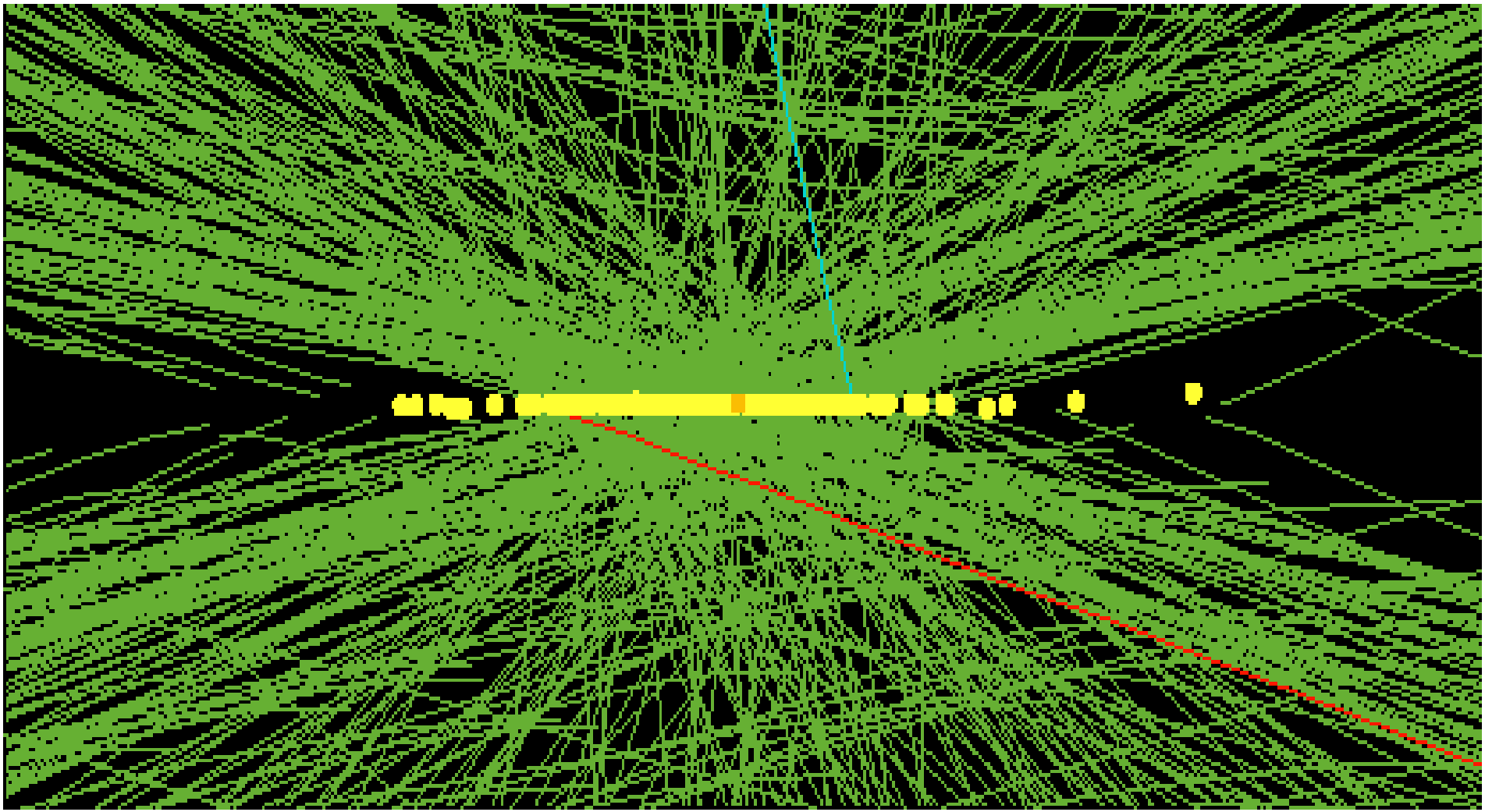


The real thing

These are big detectors,
pixels are a very small
part in volume/weight but a large
part in the number of channels.

Why pixels?

Example event from CMS. July 10th 2012, run 198609, 78 collisions in one event



How can we reconstruct all these tracks?

What are pixels useful for?

Pattern recognition

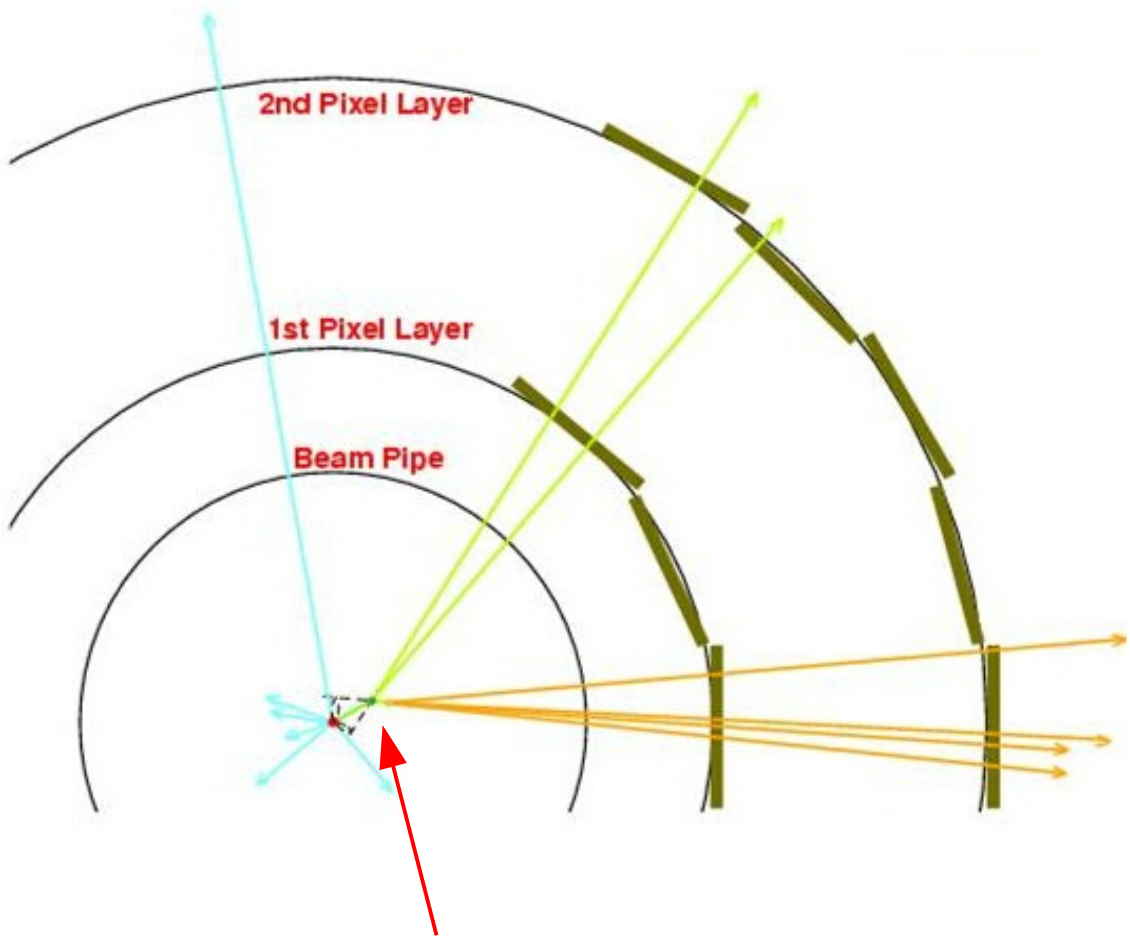
High granularity allows to build track candidates out of 2 pixel hits.

Vertexing

Very good position resolution allows to find precise track impact parameter (displacement from the origin) and the track vertex (origin of the track).

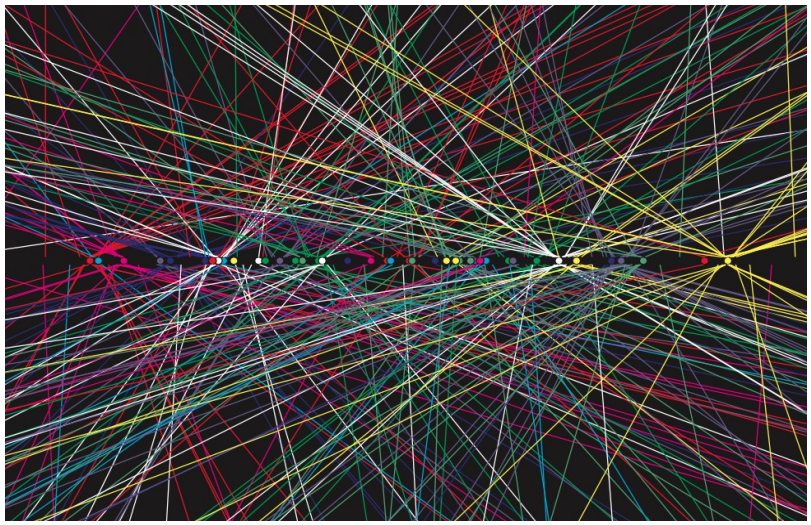
Main requirements

High hit efficiency (100%).
Very good position resolution.



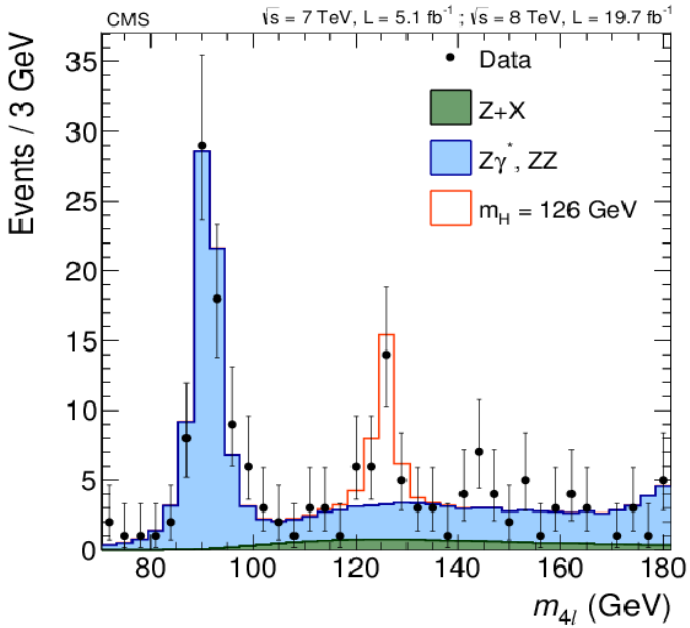
The importance of pixel detectors

Charged tracks from a typical CMS event



LHC experiments have to deal with simultaneous multiple interactions. Pixel detectors make it possible to separate charge particles from individual interactions. This feature is essential for almost all analysis.

An example: H ➔4 leptons



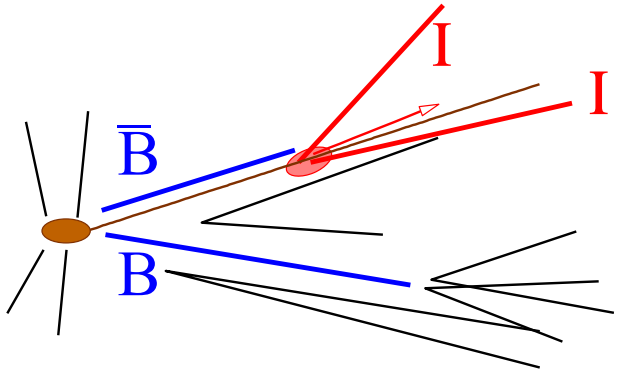
The pixel detector is so important for physics analysis that the CMS rule is : If less than 97% of the pixel detector is functional the data is declared to be "not good for physics".

Bs➔μμ Analysis

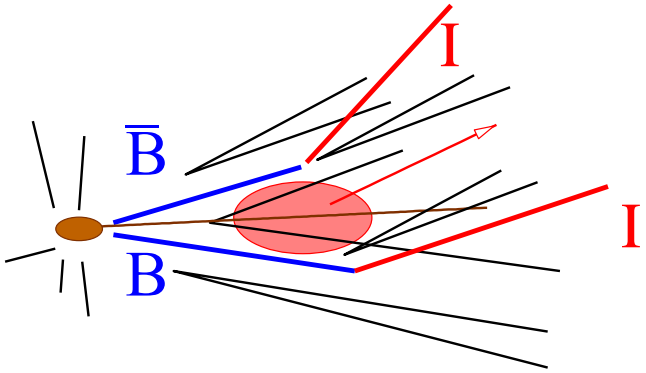
Pixel detector essential for discrimination of signal versus background.

This decay is strongly suppressed in the Standard Model

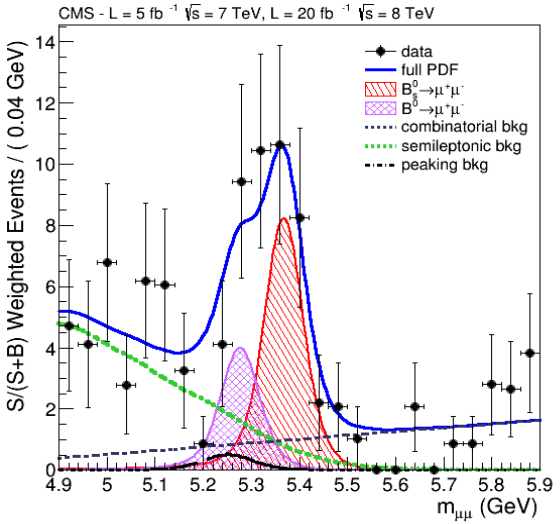
signal



background



Results



BF(BS0➔μμ) = 3.0(+1.0,-0.9) × 10-9

BF(B0➔μμ) < 1.1 × 10-10 (at 95%)

(Phys. Rev. Lett. 111 (2013) 101803)

Consistent with the SM predictions.

Analysis lead by the PSI group.

Performed using the CMS/CH T3 computing center located at PSI.

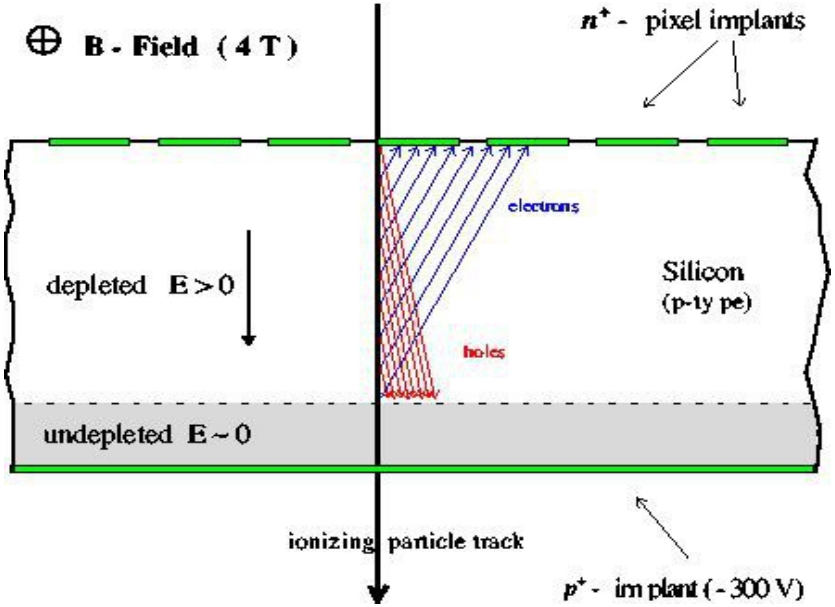
Design & Construction

Detector Requirements

- High granularity – small pixel size
- Very good position resolution (10-20μm).
- Fast - High Readout Speed
  Each collision on the average produces
  Hits – 4000 per event, 30 M hits/cm^2/sec
  Pixels – 16500 per event, 150 M pixels/cm^2/sec
- Large data volume - for one event 66 kbytes
  at 40MHz interaction rate – 2.6 Tbytes/sec (internal rate)
  at 100kHz trigger rate - 6.6 Gbytes/sec (readout rate)
- Radiation:
  instant particle fluences up to ~10^8 particles/cm^2/sec
  integrated fluence up to – 10^{16} particles/cm^2, dose 100 Mrad (1 MGy)
- Has to run cold (-20/30 deg) – needs active cooling (remove a few kW)
- Low mass (light mechanics) – not to disturb the rest of the experiment

Some of these requirements are contradictory!

CMS Pixels - Analog readout



Make use of the large charge drift in Magnetic field (Lorenz angle) to enhance the charge sharing and therefore the position resolution.

Therefore CMS can use almost square pixels 100 * 150 μm^2

good position resolution -> charge interpolation -> low pixel thresholds

Design – Hybrid Pixels

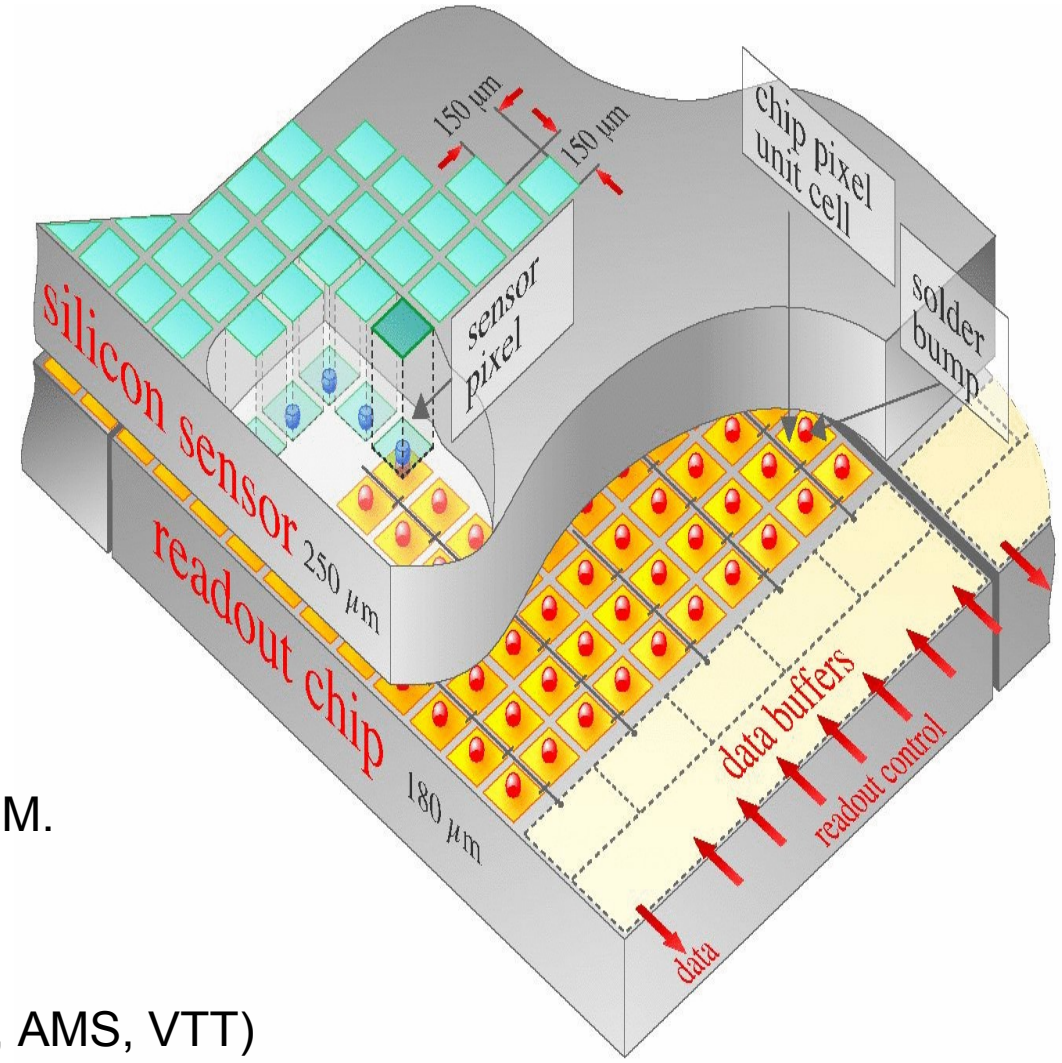
Some design parameters
had to be fixed in **mid 90-ties**.

The only realistic choice at that time
was a **hybrid detector** with a
silicon senor bump bonded to
a silicon **CMOS readout chip**.

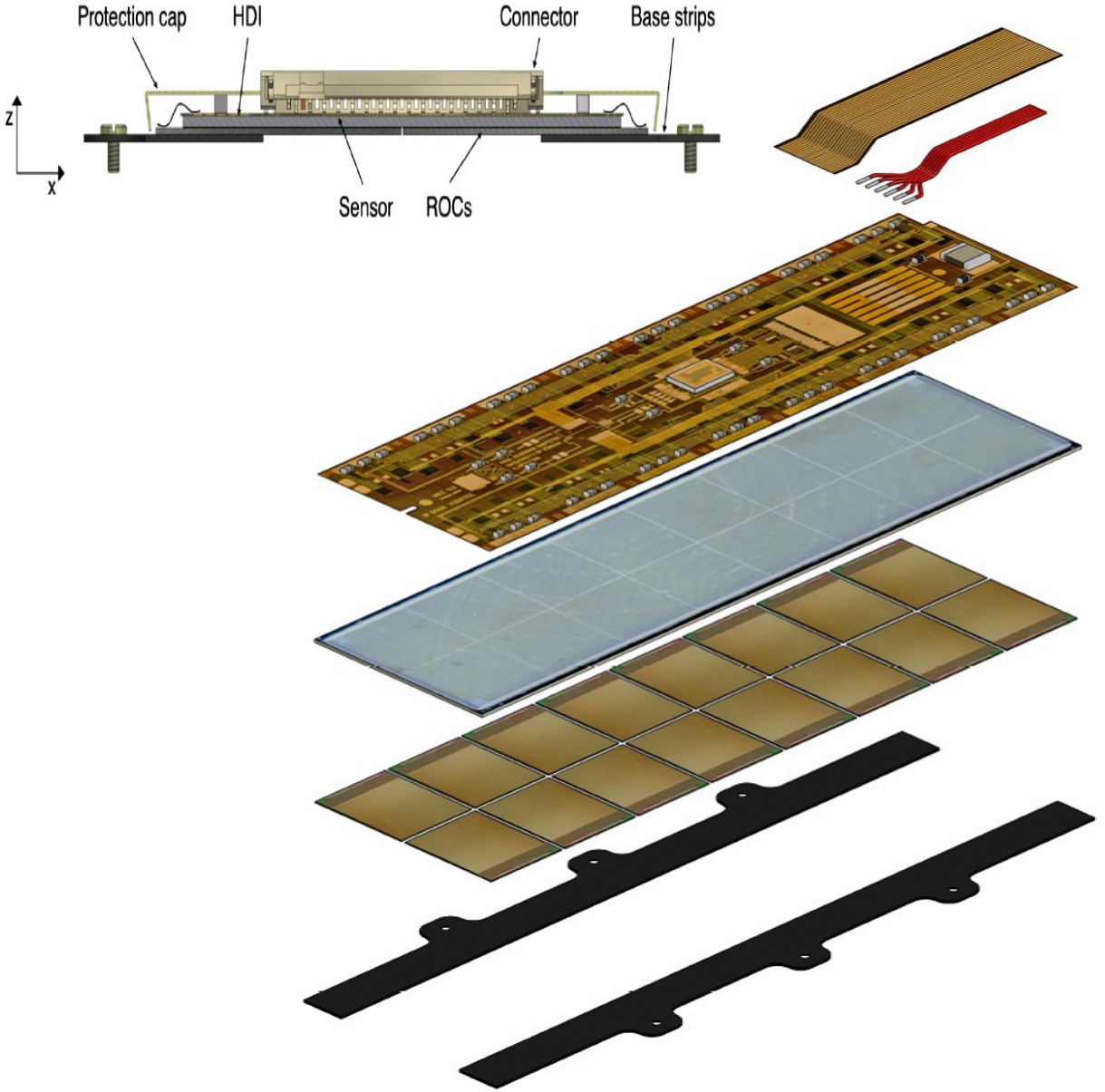
Sensor:
Both Diamond and GaAs sensor were
considered. Silicon won by far!

Readout chips:
Several technologies were considered.
For a while it looked like the DMILL
process was the winner.
Finally we all went to 0.25 micron CMOS IBM.

Bump bonding:
Very new technology in 2000.
Several companies learnt how to do it (IZM, AMS, VTT)
PSI developed its own bump-bonding in-house!



CMS Module Design



Cables: signals & power

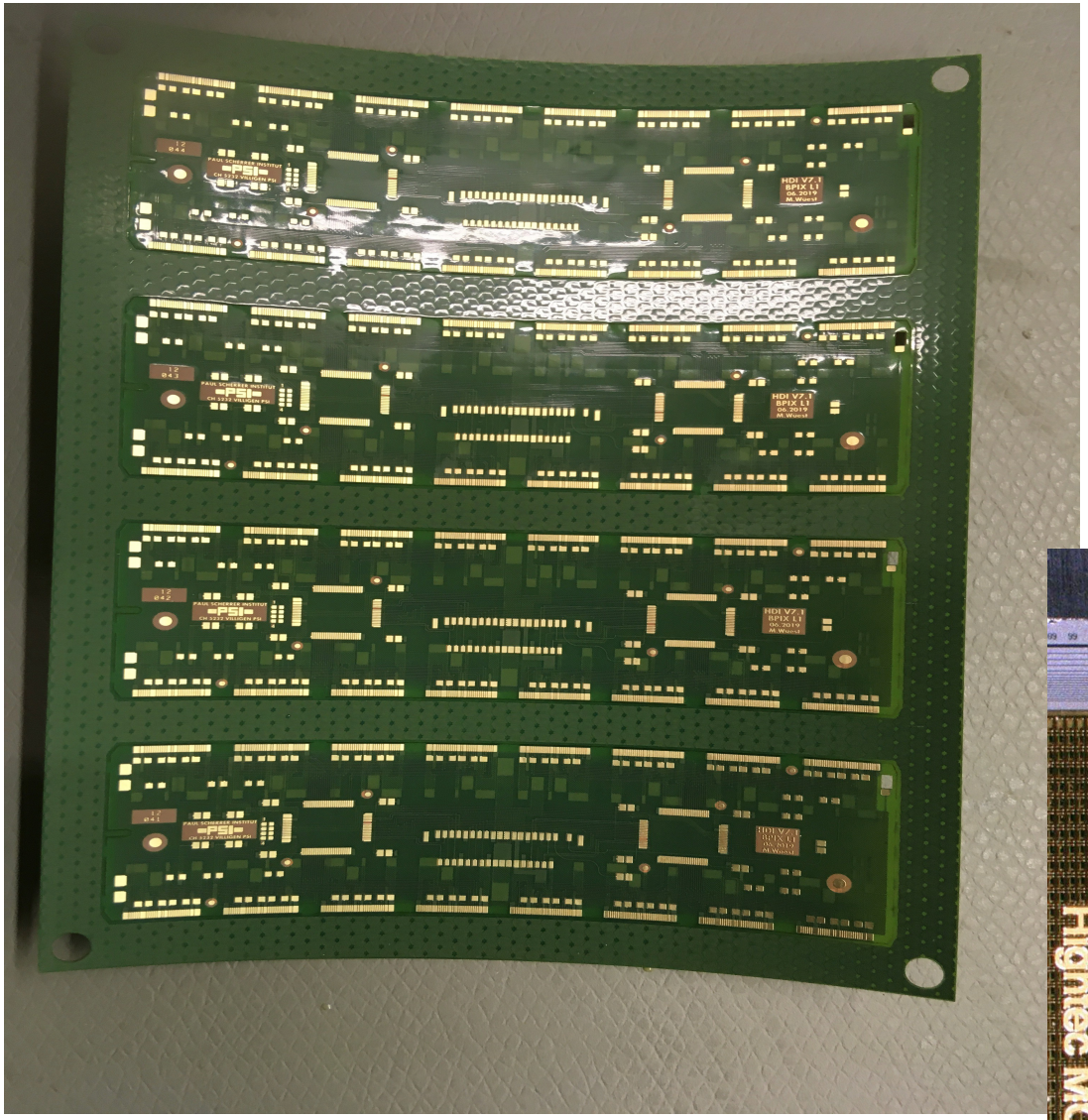
HDI print with the TBM chip

Si sensor (280um thick)

16 ReadOutChips (ROCs, 180um)

Base strips: Si3N4

High Density Interconnect (HDI)

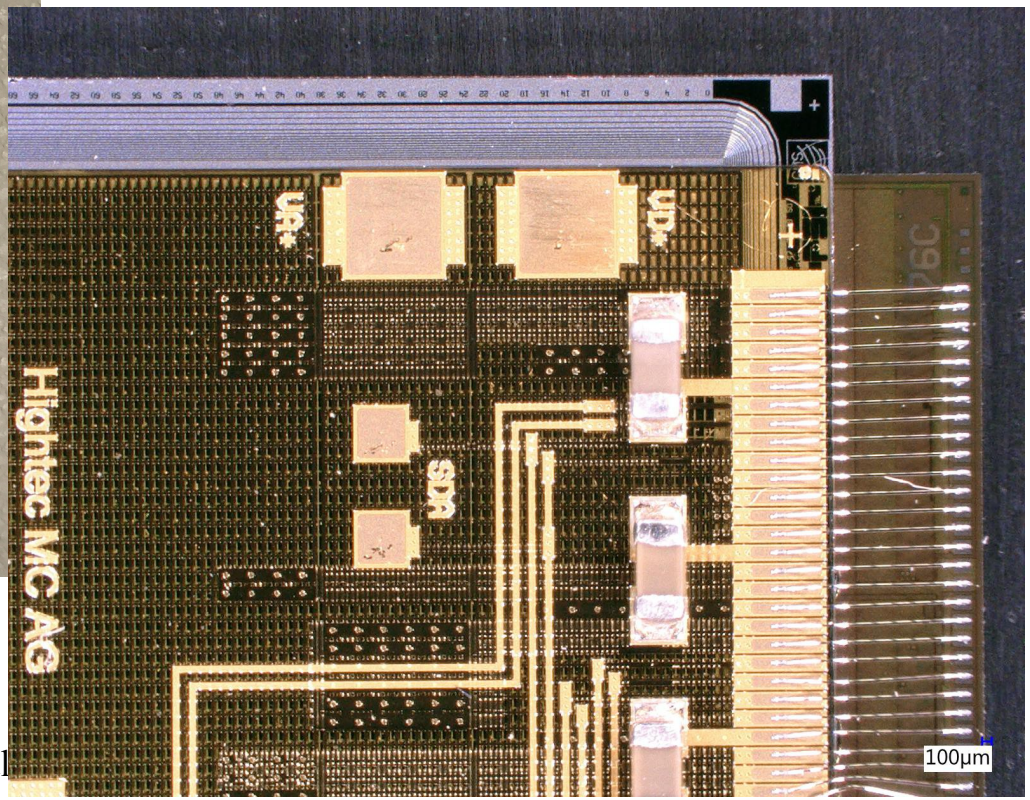


A sandwich of Kapton an Cu (3 layers), a very thin (~50um) flex print.

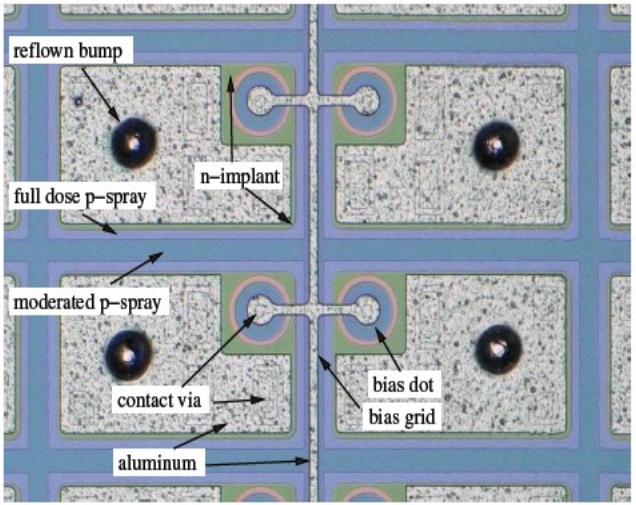
Has to stand high radiation & 1000V

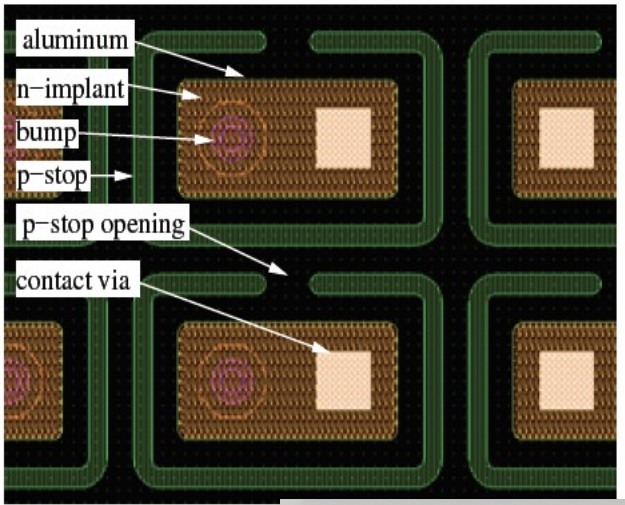
Designed by us, manufactured in industry

Details



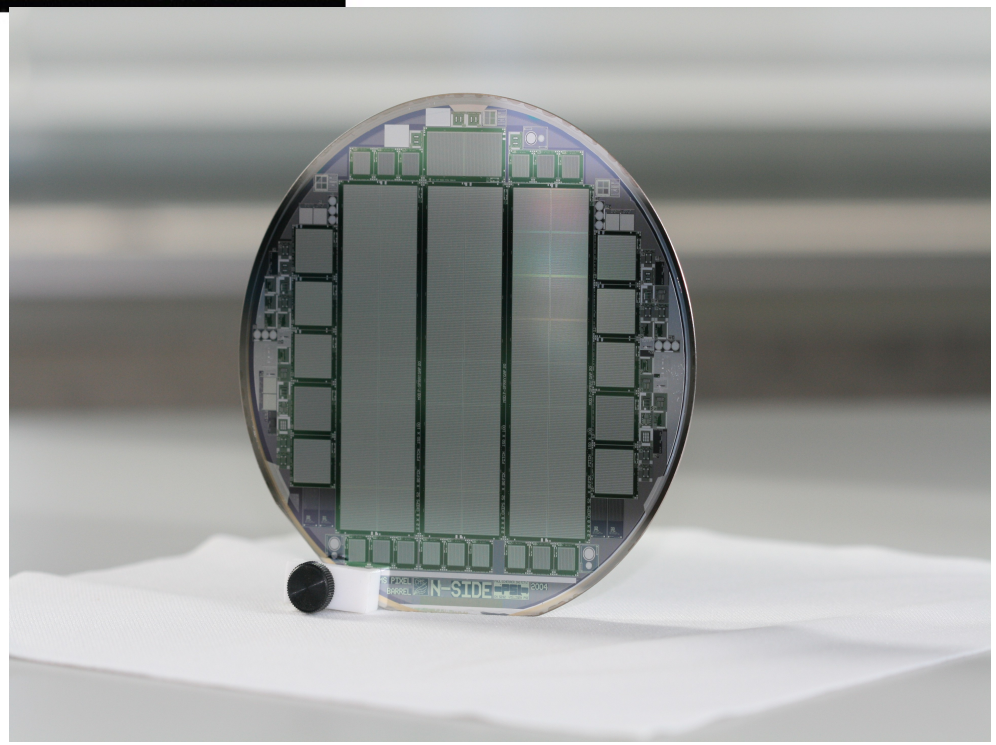
Sensor design





Details of the pixel structure bpix(left) , fpix(right).

The whole Si wafer

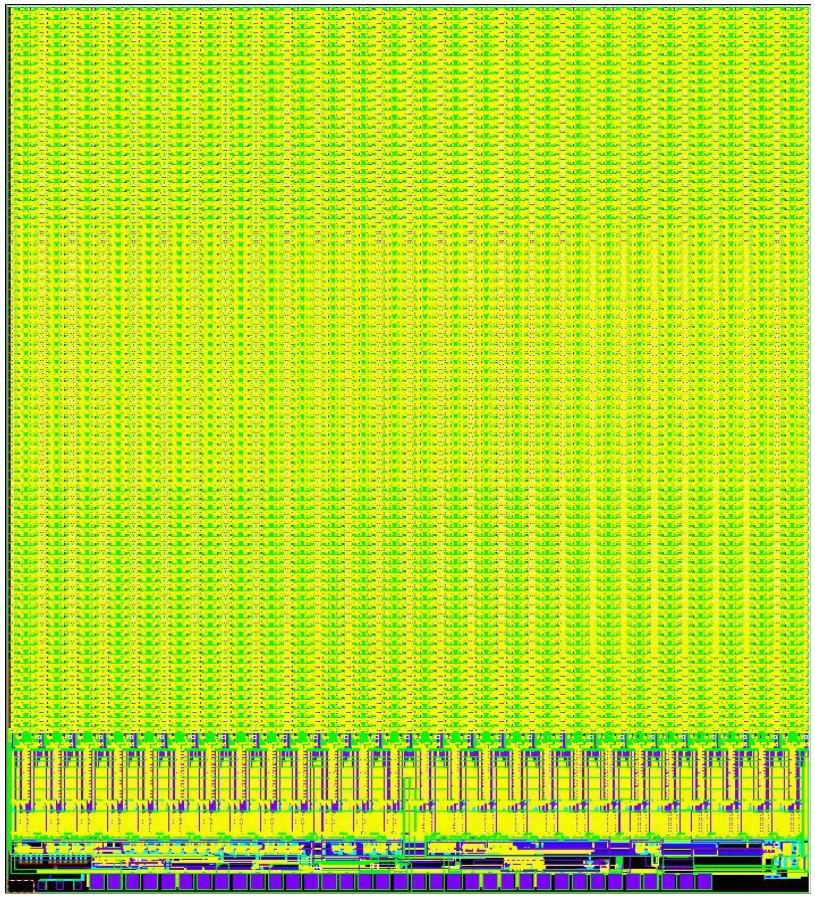


Designed at PSI, produced at CiS in Erfurt
n-in-n p-spray design, 3.7 kOhm resistance

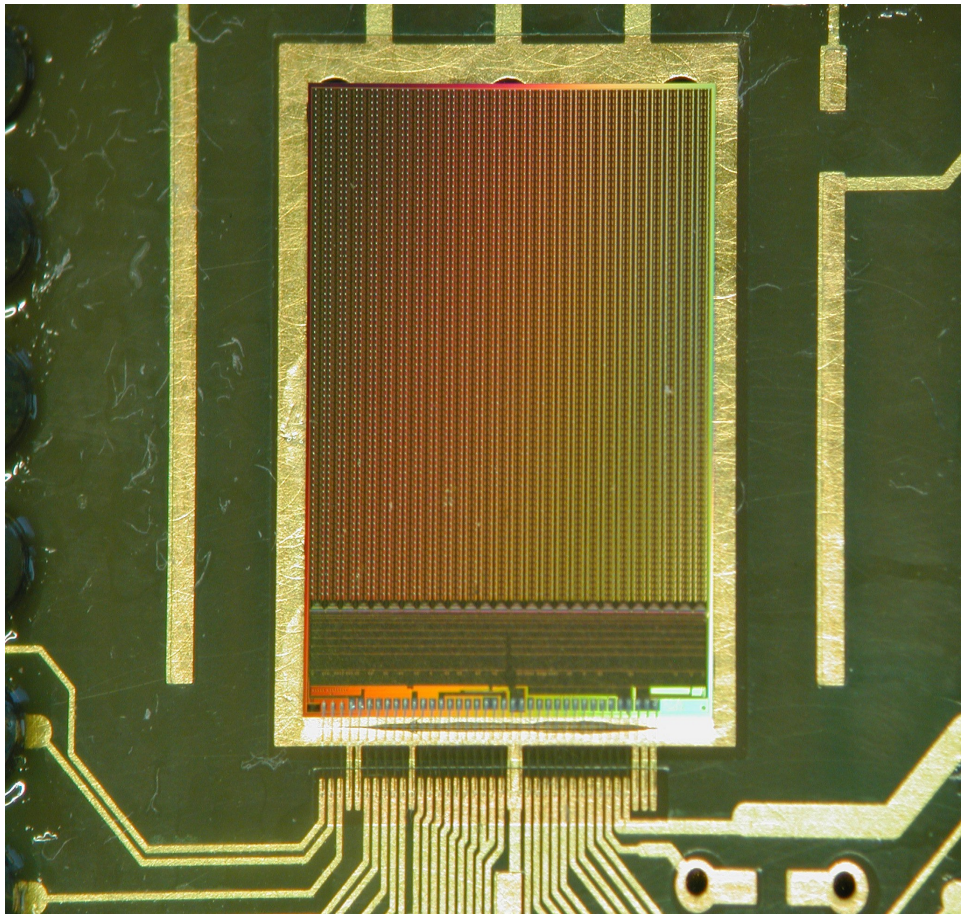
The Readout chip (ROC)

250nm CMOS technology (IBM)
Designed at PSI, produced by IBM/GlobalFoundries

Design



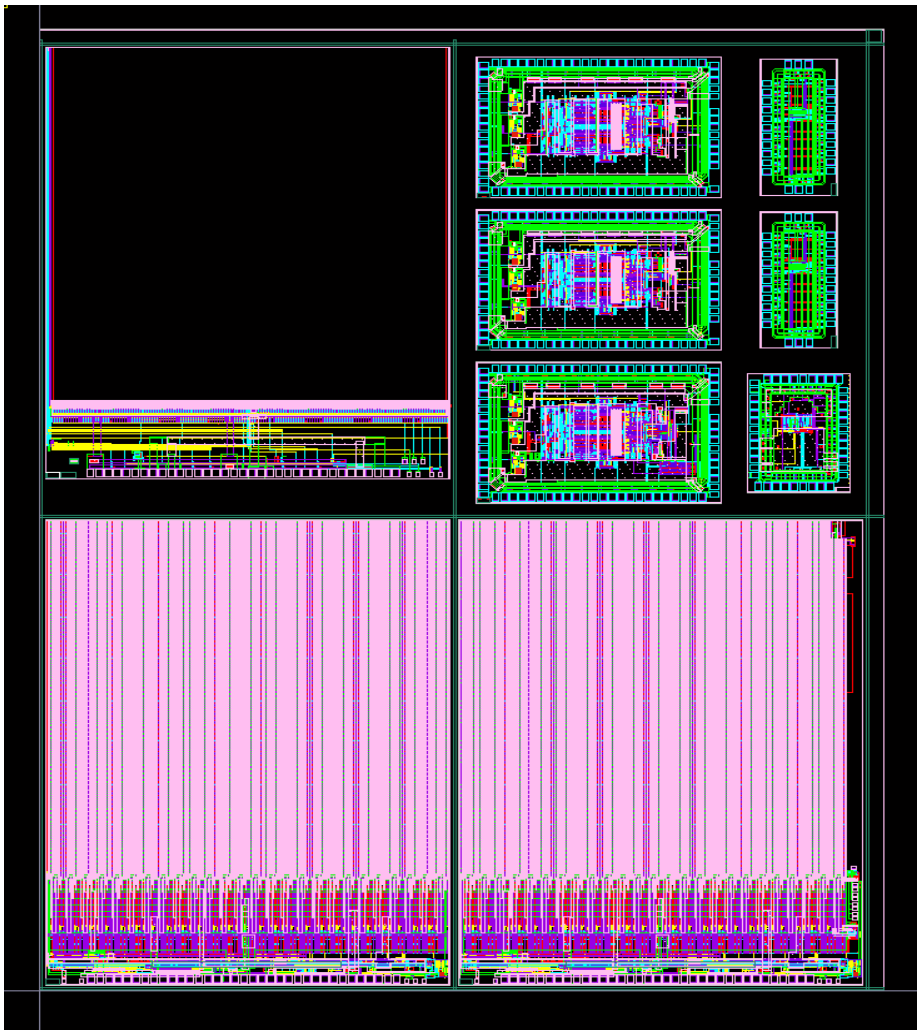
The real chip



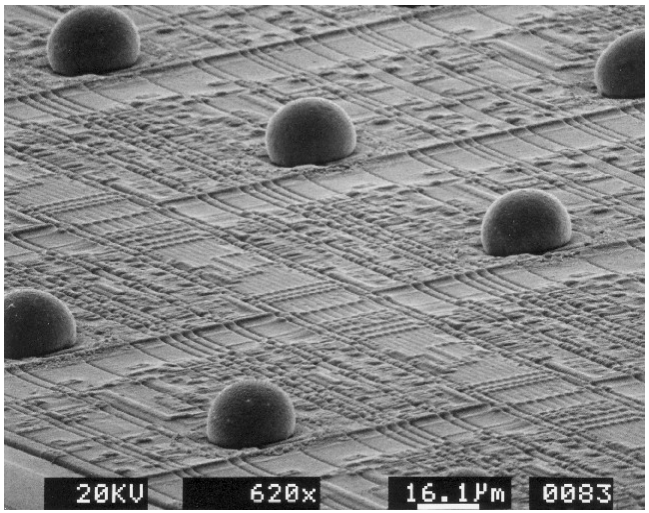
CMS Pixel Readout Chip (ROC)

- 0.25 m CMOS technology
- 80 x 52 pixels
- power: 28 W/pixel
- pixel area: **100** m**x 150** m
- 1.3 M transistors

A pixel reticle



Sensor to ROC bump bonding



indium bumps

CMS Module Design

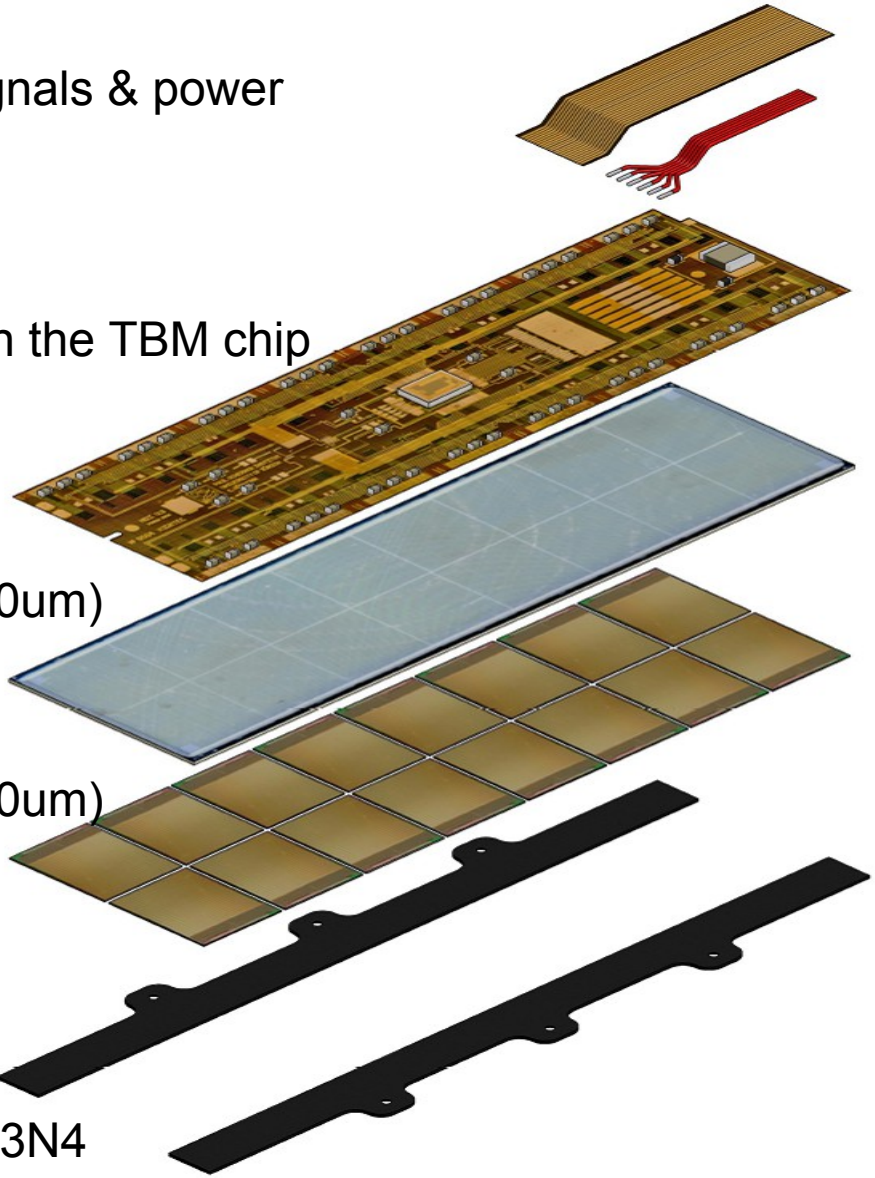
Cables: signals & power

HDI print with the TBM chip

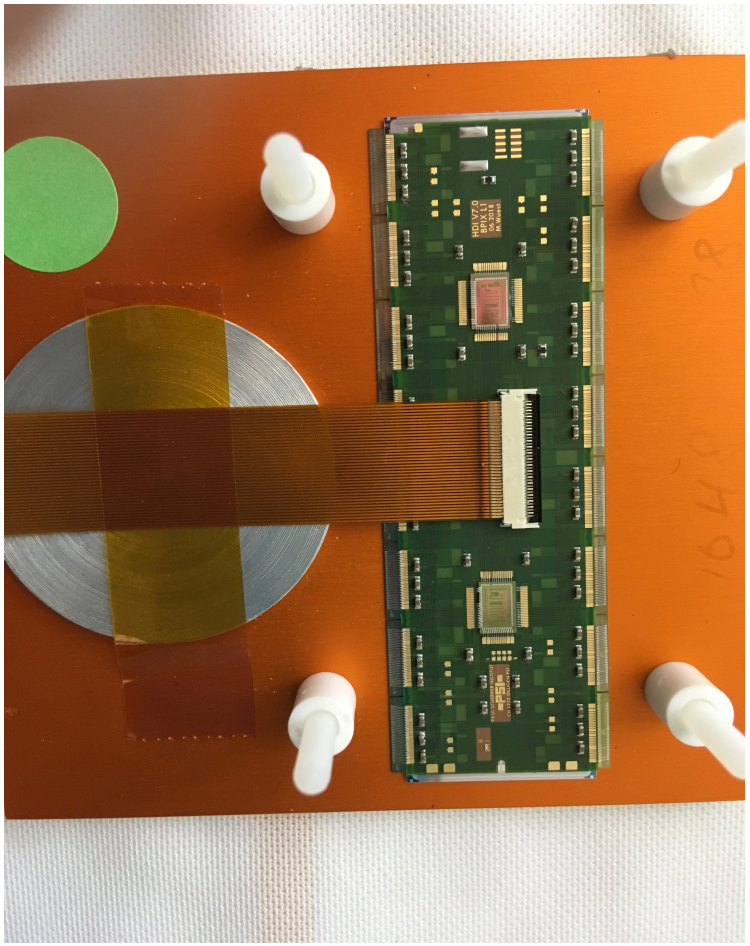
Si sensor (280um)

16 ROCs (180um)

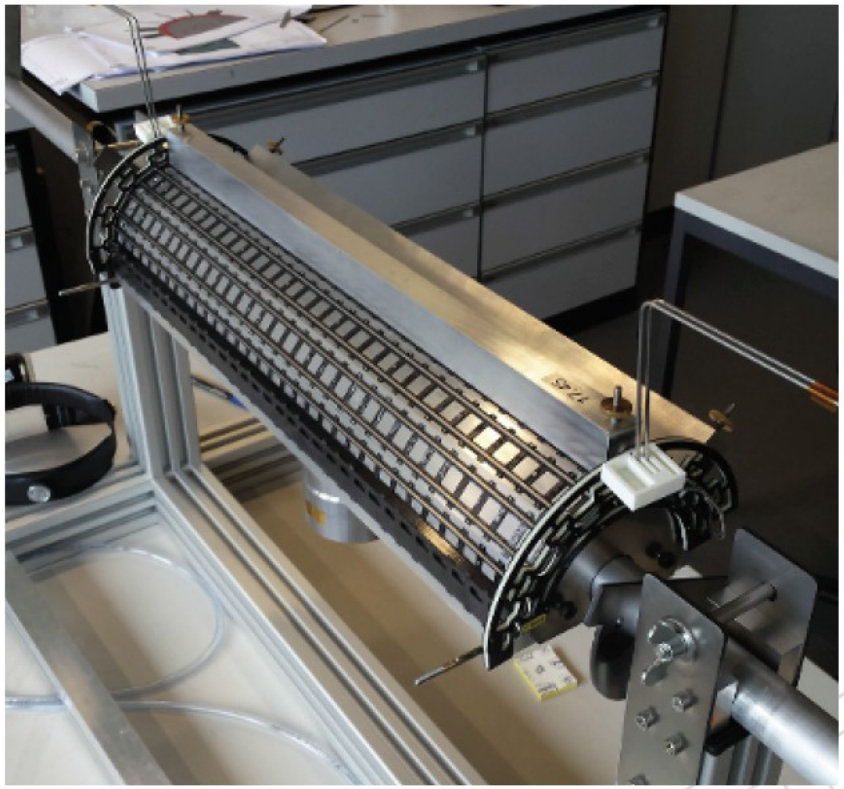
Base strips: Si3N4



A Ready module

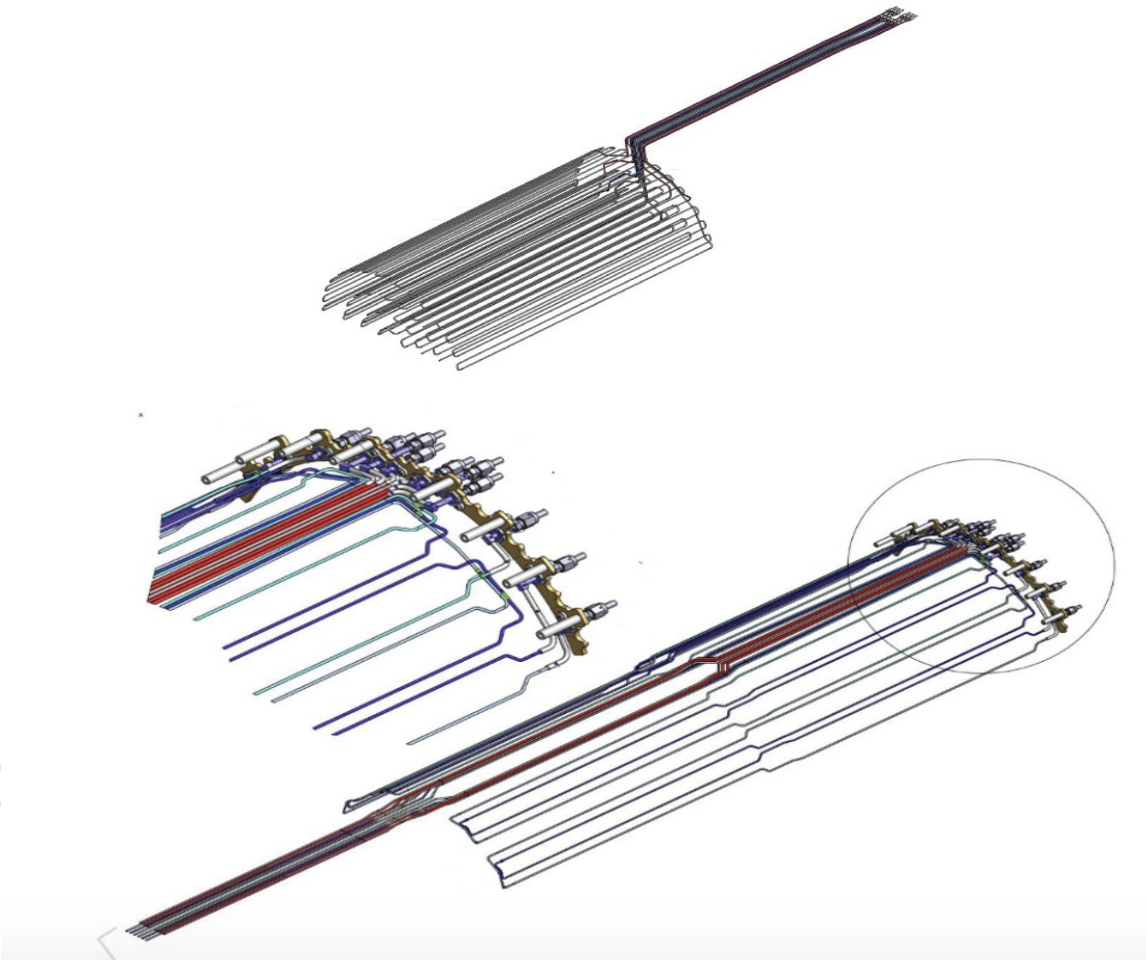


Mechanics



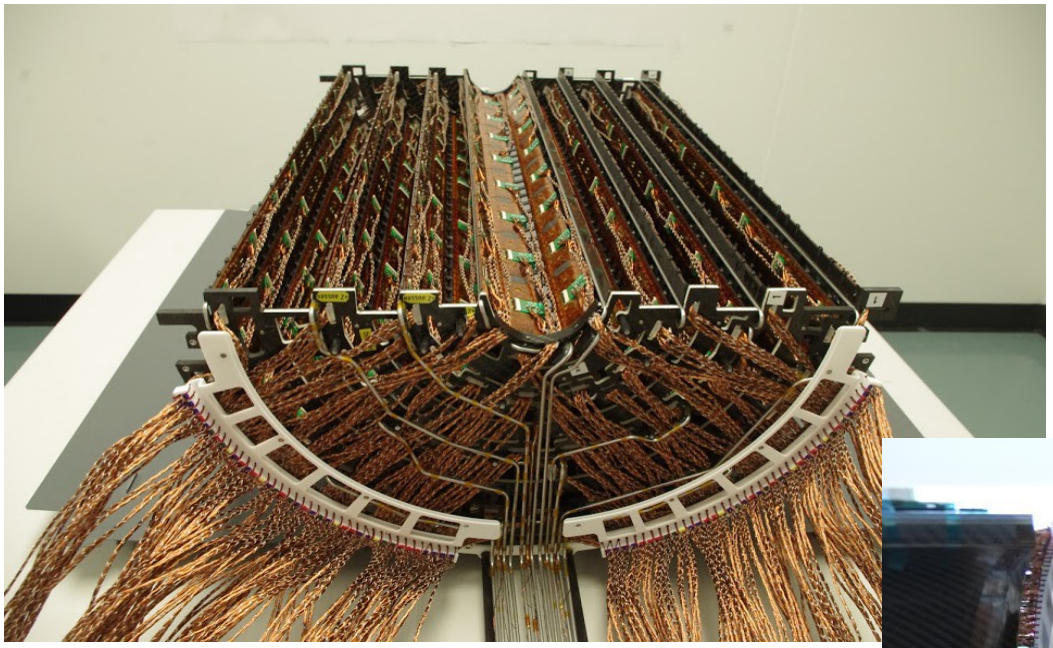
Carbon fibre structures (ladders) to hold modules

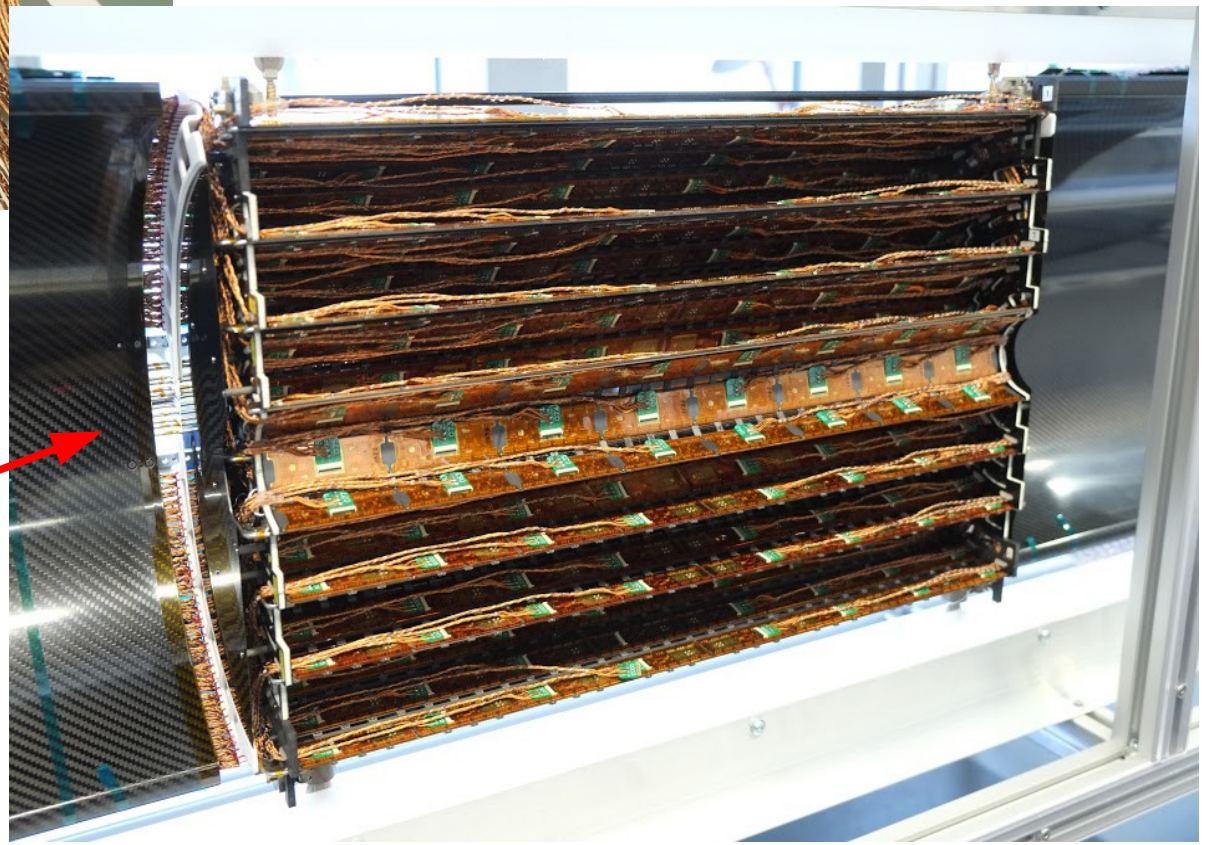
Cooling pipes



Evaporative CO2 cooling at high pressure uses StainlessSteel pipes 1.7mm ID, 50um wall thickness.

After Ladder/layer integration

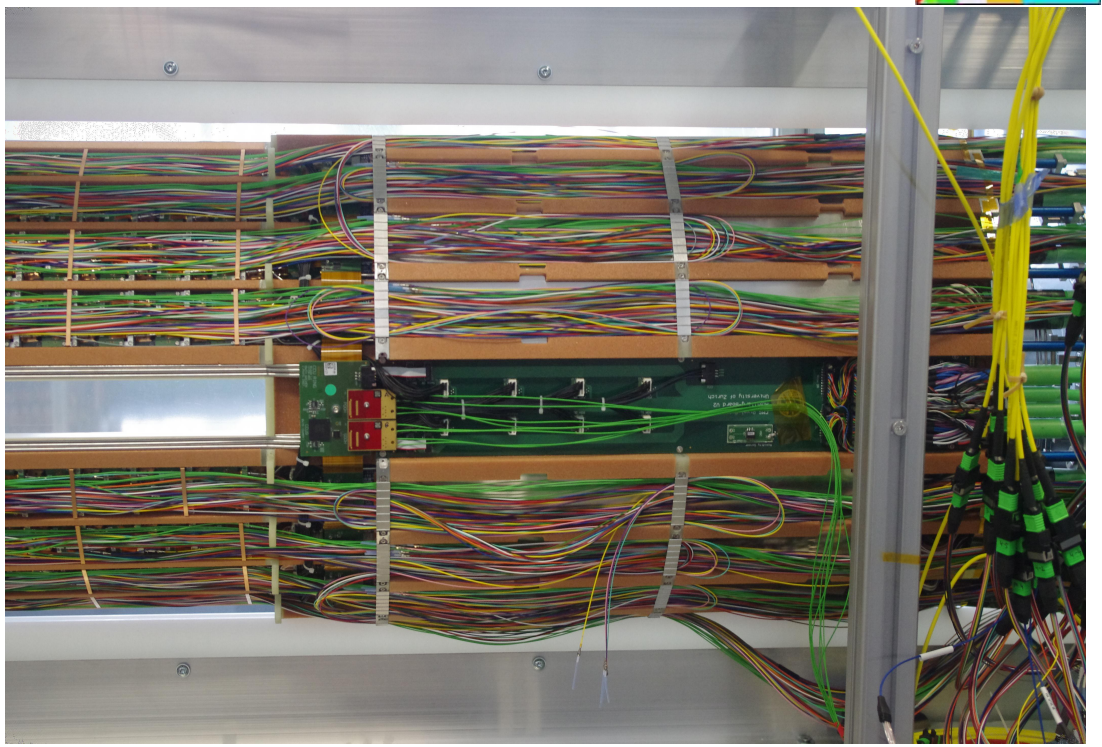


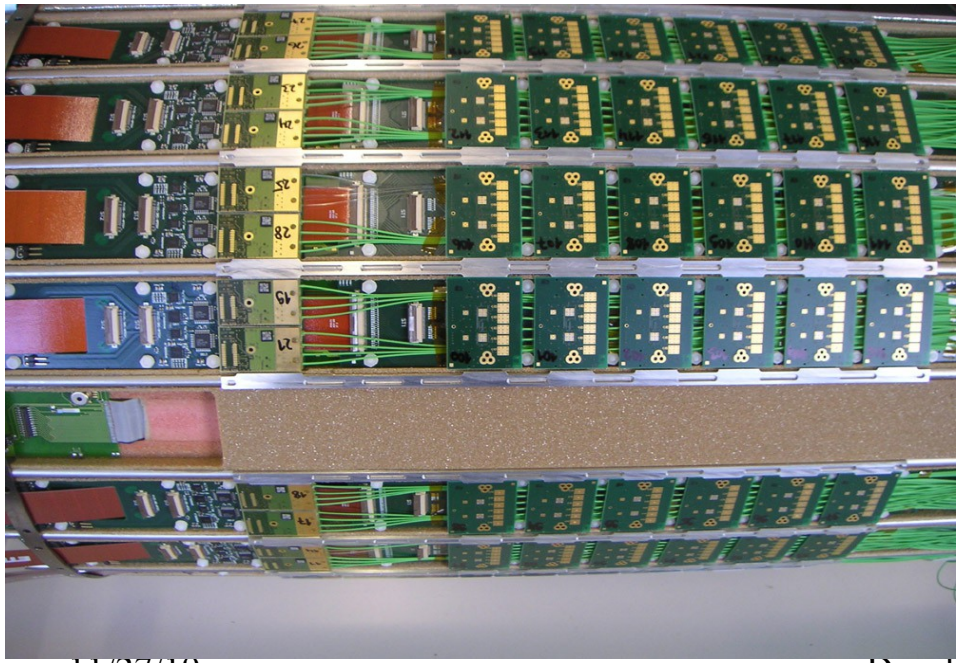


Support structure to hold cables

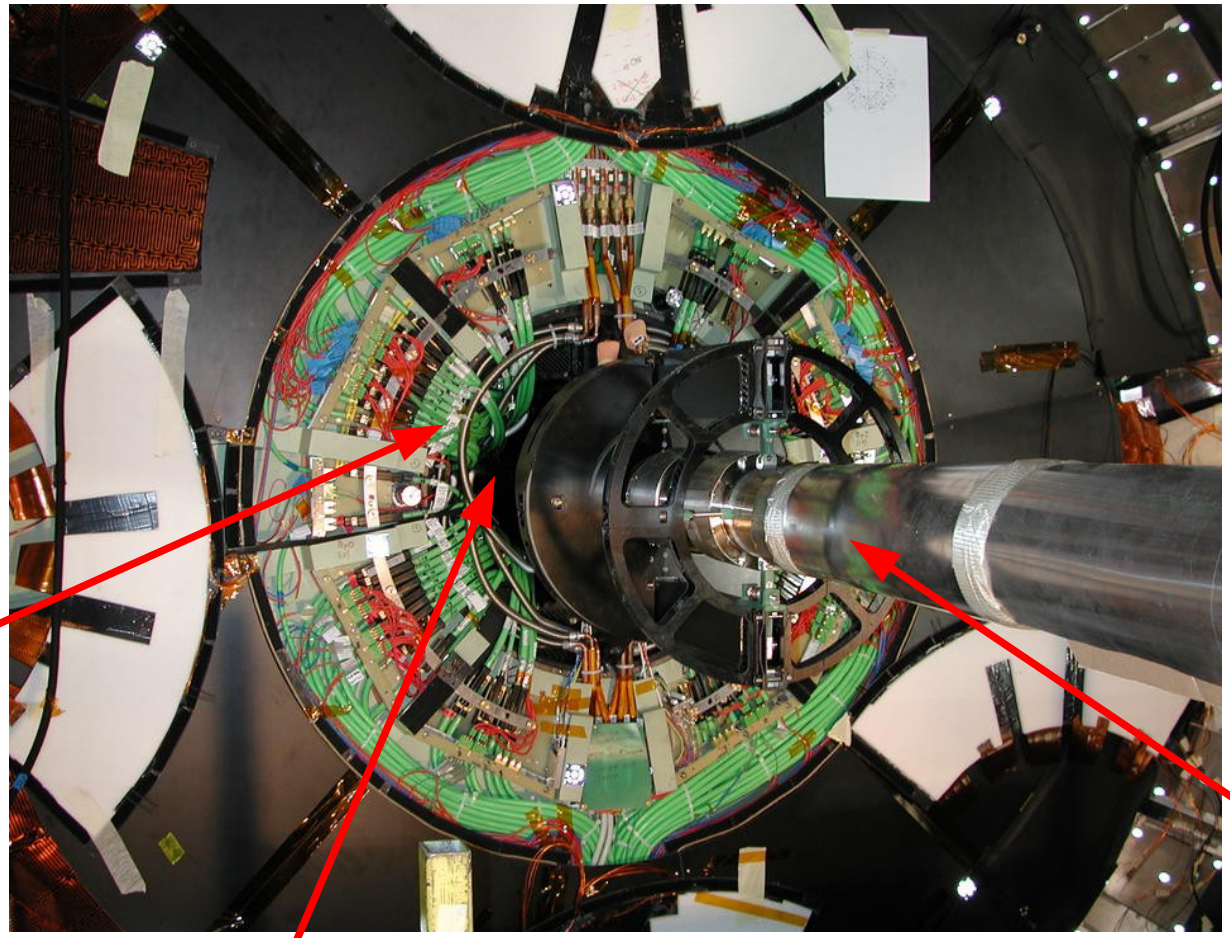
Important construction steps: the supply tubes

Many electrical components are not directly on the pixel modules but in the so called supply tube. which also brings all the electric power and cooling.





Installation in CMS



Cables & fibres

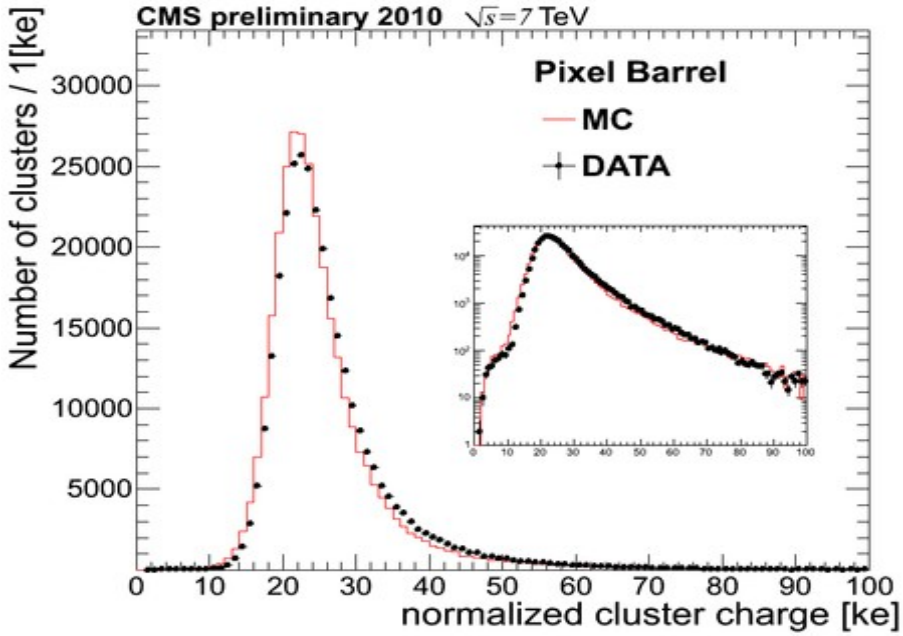
Beam pipe

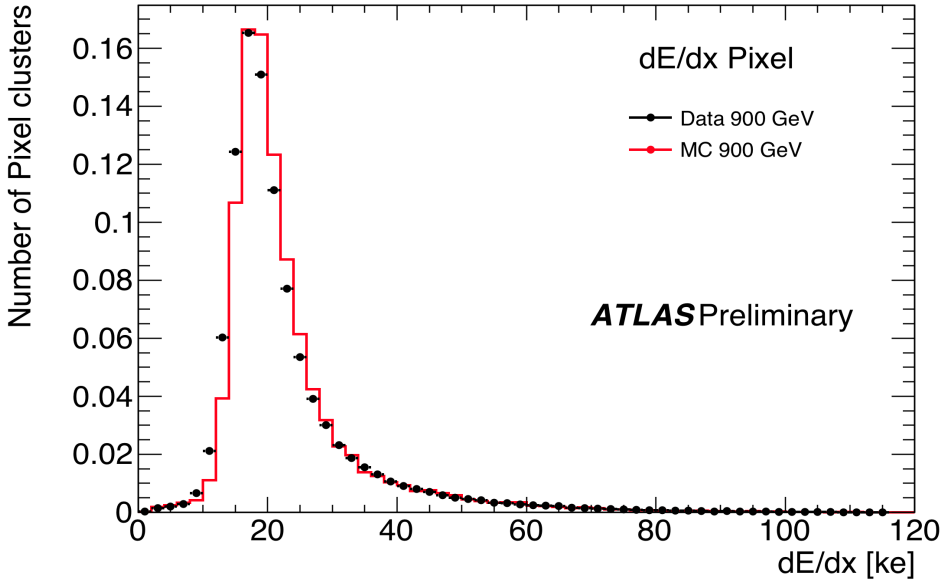
The pixel detector is inside

Performance

Cluster charge (Landau) – comparison with simulations

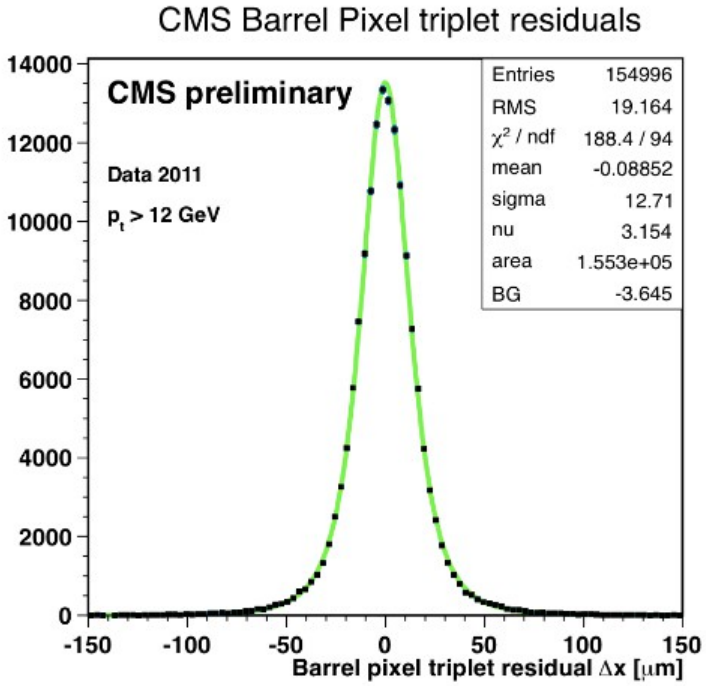
Measured cluster charge distribution compare with MC simulations.





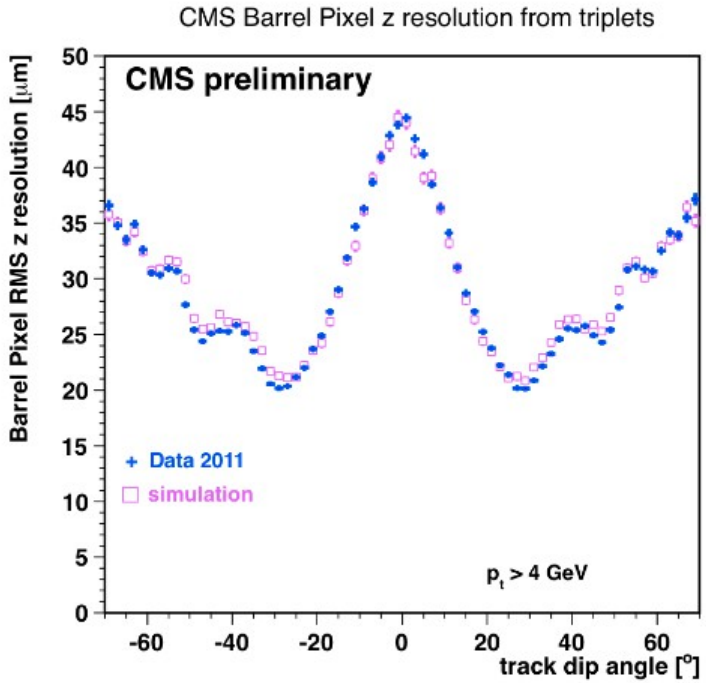
The good quality of the data-MC comparison shows that we understand our detectors very well.

Position resolution

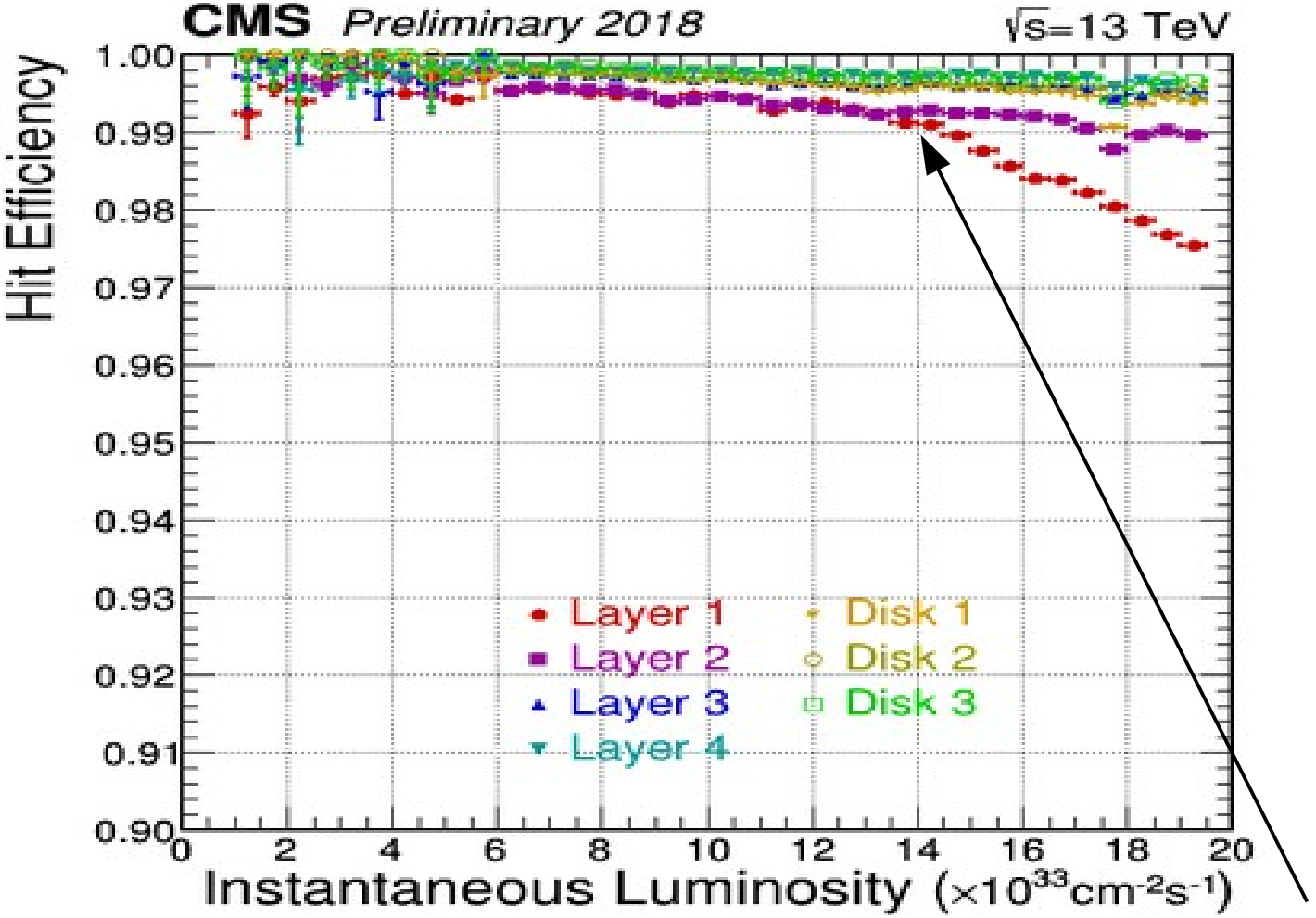


Position resolution in the transverse direction is about **10.4 um**

Position resolution in the longitudinal direction, varies strongly with the track angle.



Hit Efficiency

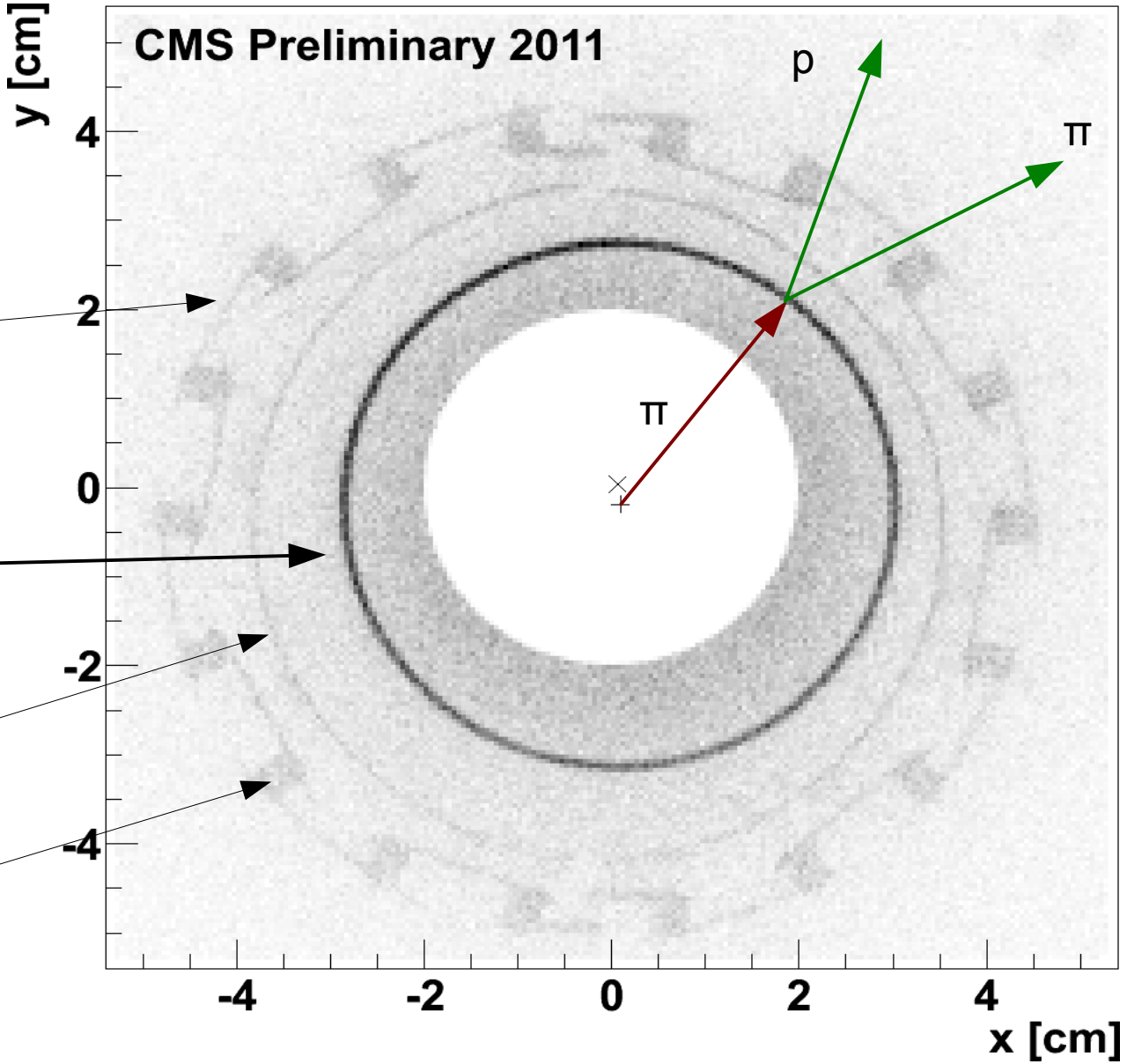


L2 - 100MHz/cm2

L1 - 400MHz/cm2

Detector Performance

Material close to the proton beam measured through secondary interactions (vertexes of nuclear/hadronic interactions).



Pixel module

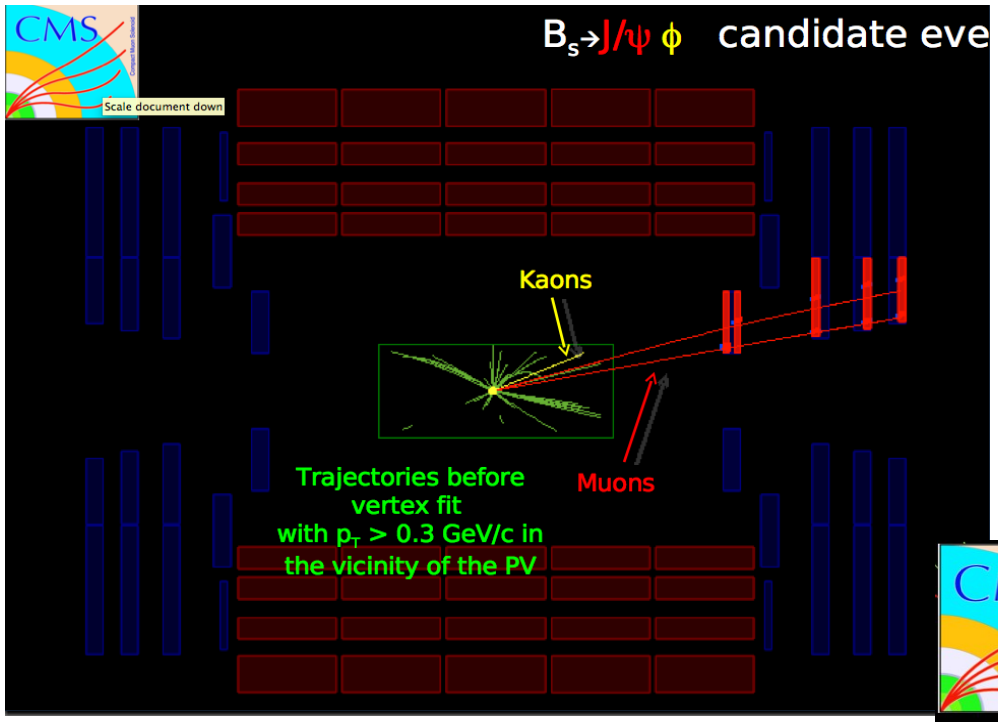
Beam pipe

Kapton-Al shield

Cooling pipe

B_s Meson

Is the detector performance good enough to measure things like this?



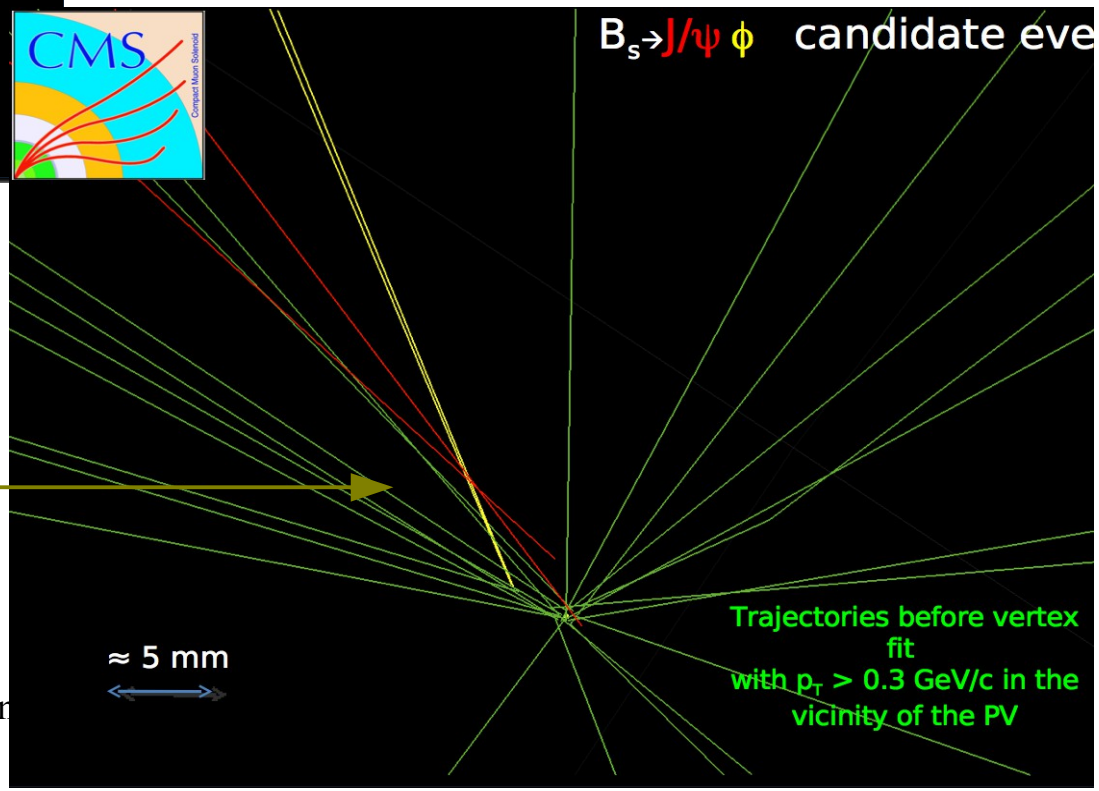
$B_s \rightarrow J/\Psi\ \Phi$

$J/\Psi \rightarrow \mu\mu$

$\Phi \rightarrow KK$

An event display of a candidate decay

See the secondary vertex



Operations

Radiation Effects

Phase0/1 detector will have to survive ~ 2-3 *$\mathbf{10^{15}}$ **particles/cm^2**.
For Phase2 (High Luminosity LHC) it will be much more.

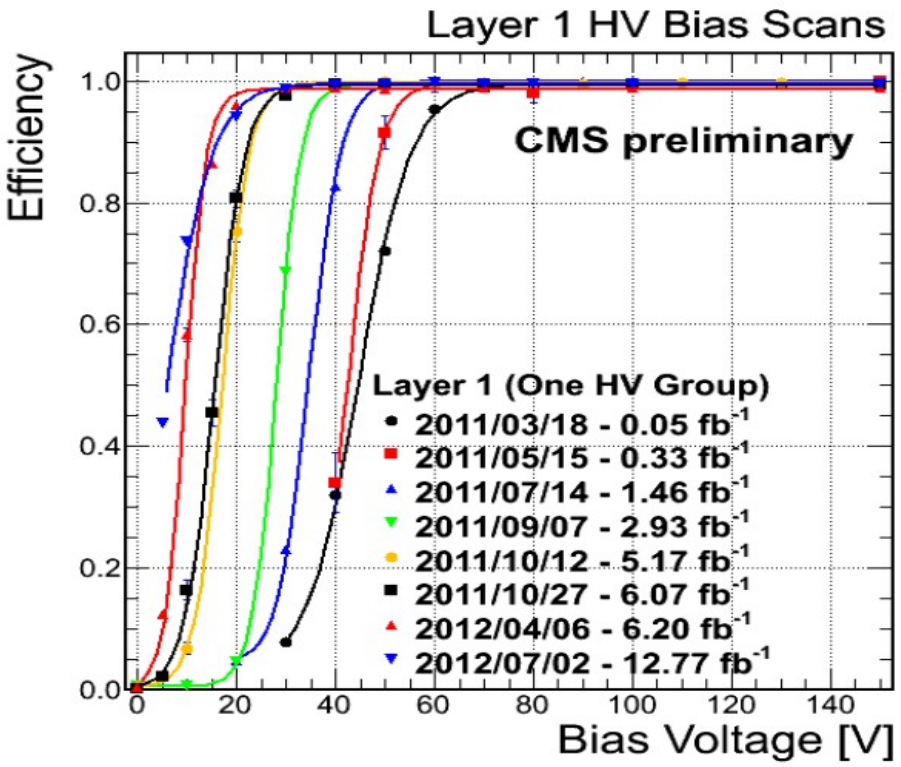
1) **Sensor damage** – increased leakage currents
Seen from the beginning (see next slide).

2) **Sensor damage** – partial depletion, charge trapping,
need to increase the bias voltage.
But we clearly see the full depletion voltage change.

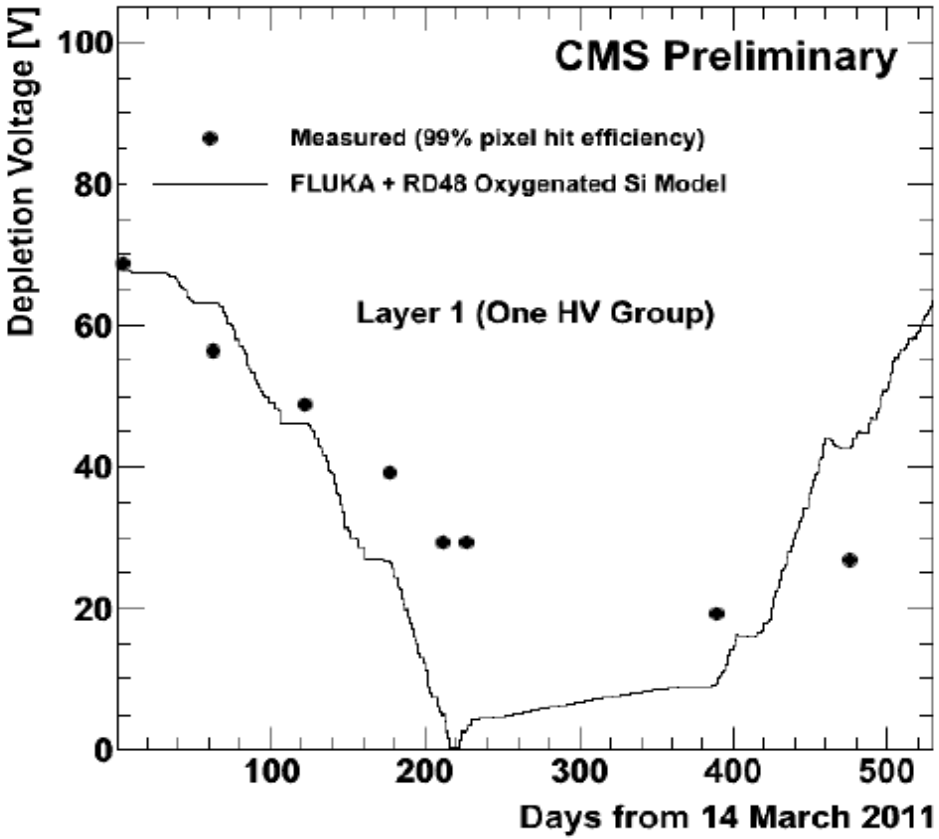
3) **Single Event Upsets (SEUs)** – change of state 0<->1 in flip-flops due to the passage of a heavy ionizing particle.
First observations at instant luminosities of 10^{33} ($2.5*10^6$ particles/cm^2/sec).
The effect manifests itself by a sudden change in some readout parameter.
Detector reconfiguration brings it back to normal.

4) **ROC (Readout chip) damage** – change of the internal voltages due to irradiation.

Bias scans

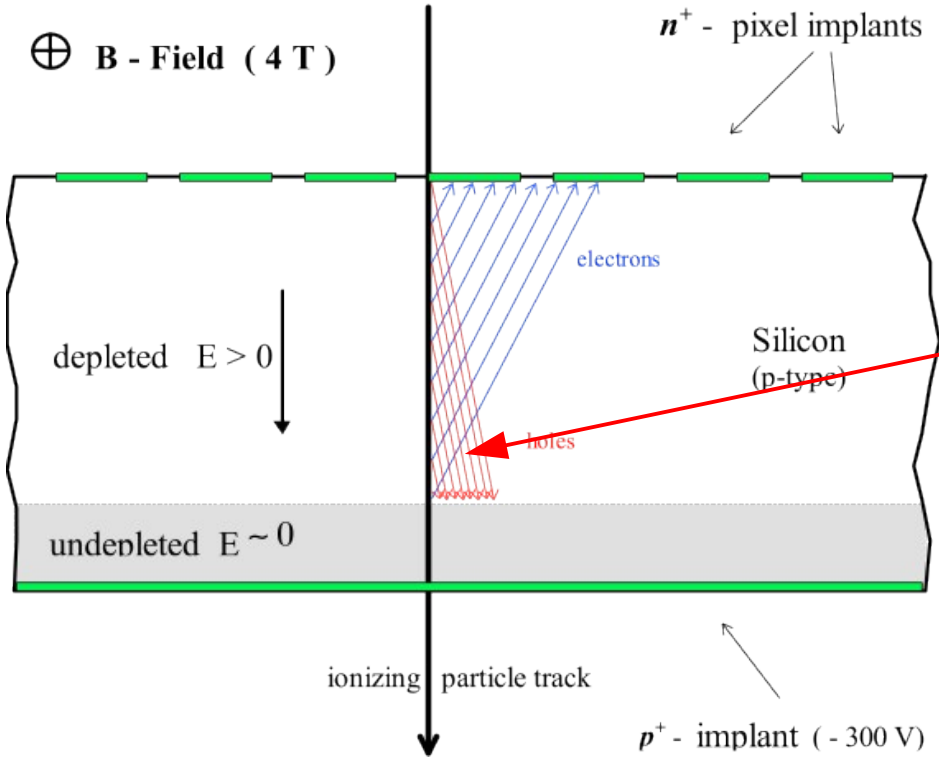


Layer 1 bias scans versus time (radiation dose)



Full depletion voltage versus time

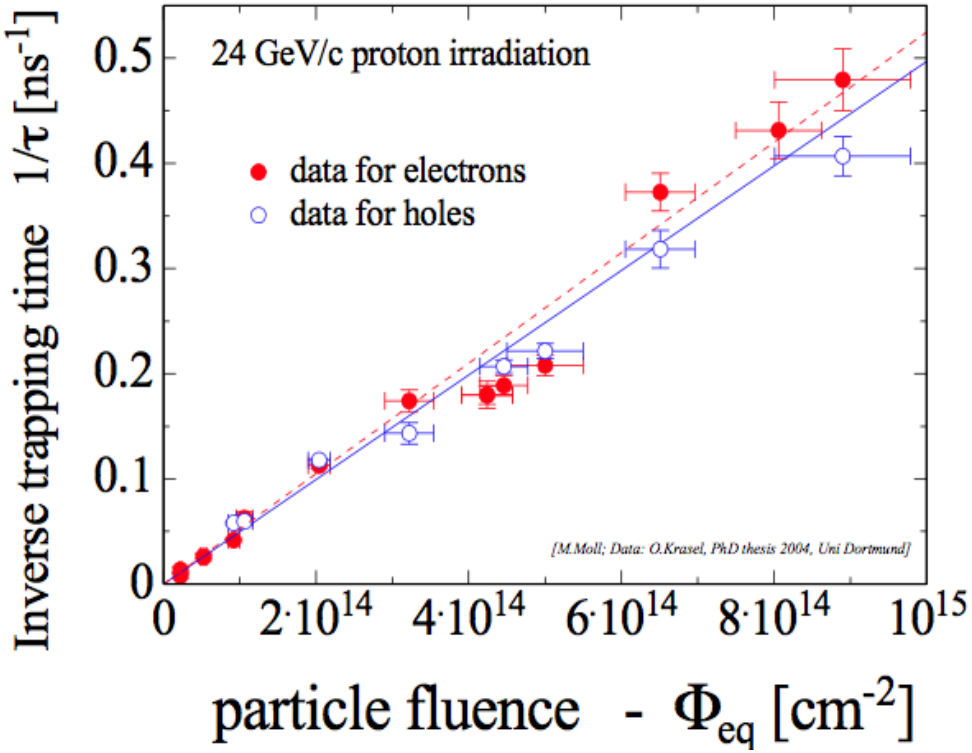
Trapping Charge Losses



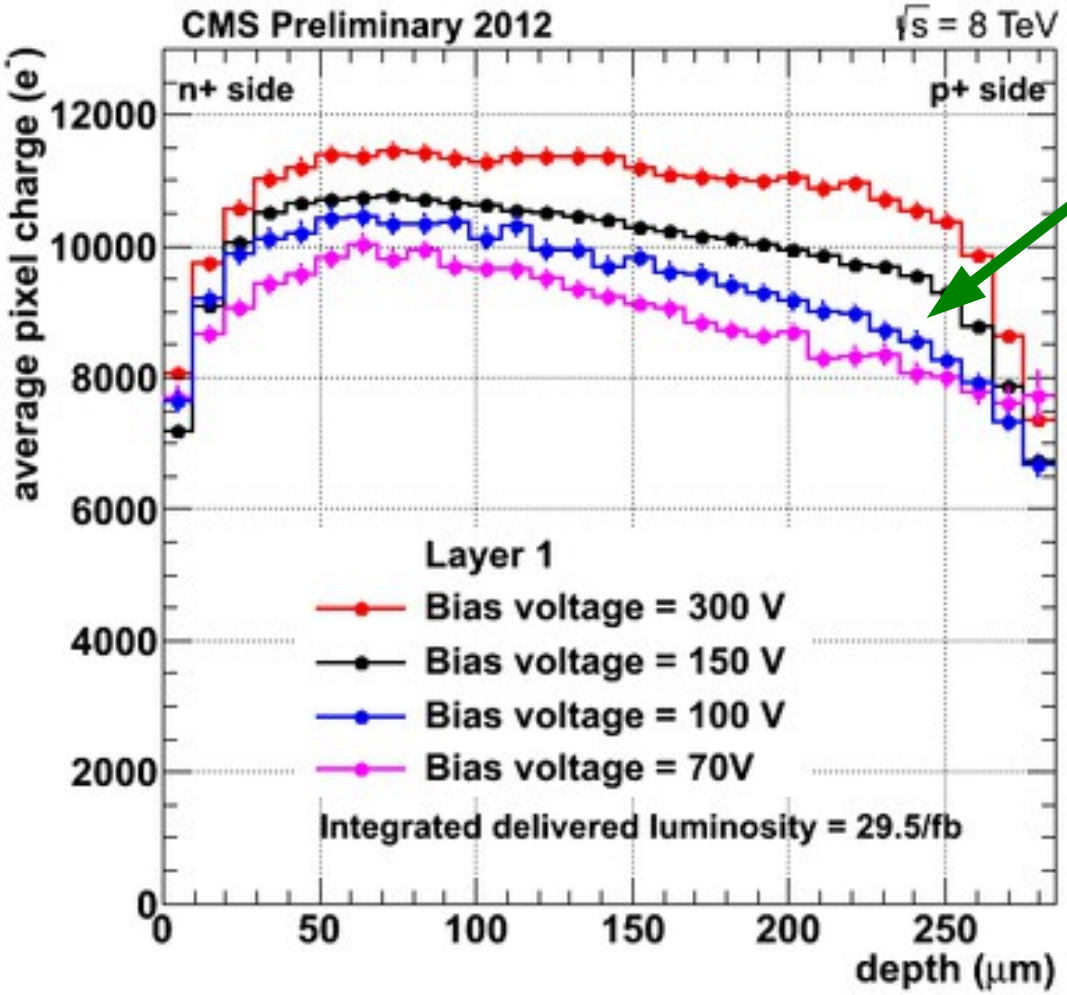
Radiation generates charge trapping centers

Even for a fully depleted sensor the charge from the back has to travel longer ->
increase of charge trapping

Result of special trapping measurements



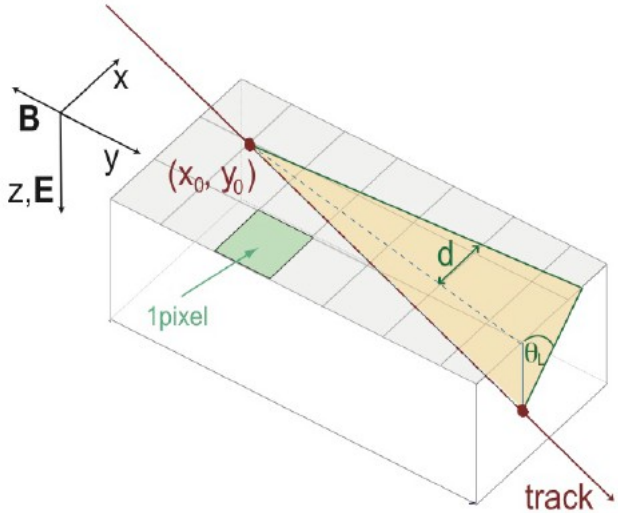
Charge Loss in CMS Pixels



Loss of collection efficiency for charges which have to drift from the far side.

Will affect the position resolution!

In simple position algorithms the position is measured from the edges.
Use "Template" method!



Transistor Effects

This is another example of how radiation affects electronic circuits.

At the surface of silicon chips there are areas of Si-oxide.
Ionization from passing charged particles will create charge also there.
The charge will not be removed and will remain trapped for a long time.
In the gate area of a transistor this charge will be equivalent to a voltage applied to the gate, and therefore will cause a “threshold shift”.

-> CMOS deep-submicron technology reduces this effect -> thin layers

Special “**radiation tolerant**” transistor design

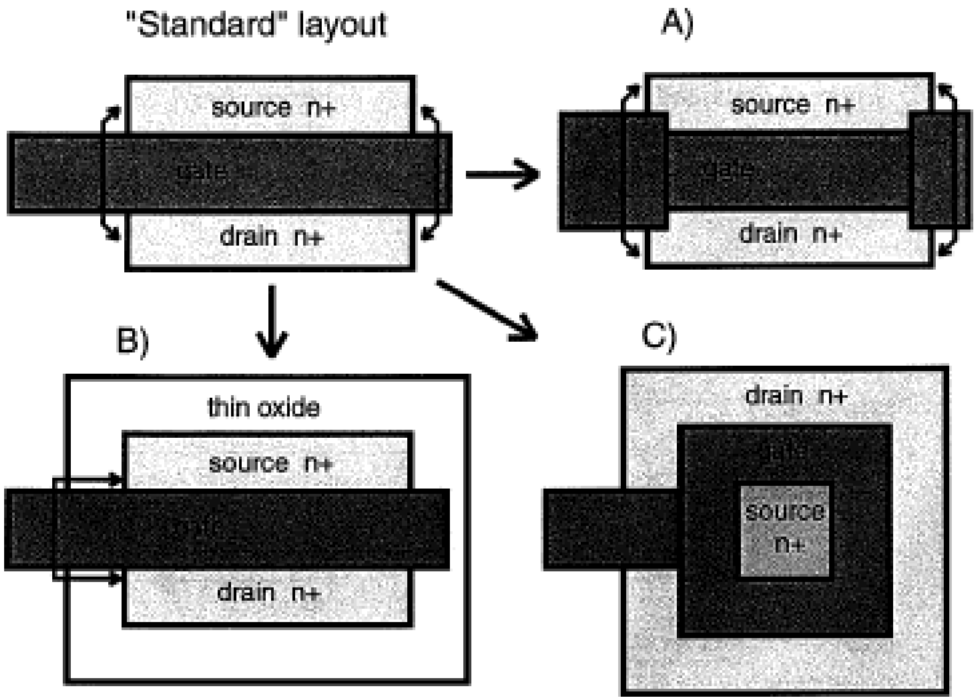
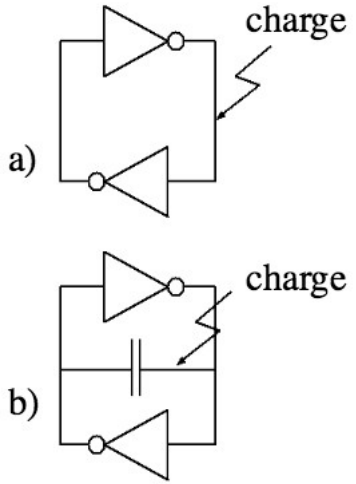


Figure 8.3: *The nmos “standard” layout, and three solutions proposed to the leakage current problem: A) Side gate layer expanded. B) Extended thin oxide region. C) The Enclosed Layout NMOS Transistor.*

Single Event Upset

Now we turn our attention to the readout chip (ROC).

- many transistors (the CMS readout chip has 1.3M transistors).
- each of them is sensitive to a Single Event Upset (SEU).



Remember:
A hadronic reaction (e.b. pion absorption) can dump a few MeV of energy in a few microns.
If the affected volume is close to the transistor sensitive area the transistor might switch its state.

For example: a memory cell can switch form 0 -> 1 or vice versa.

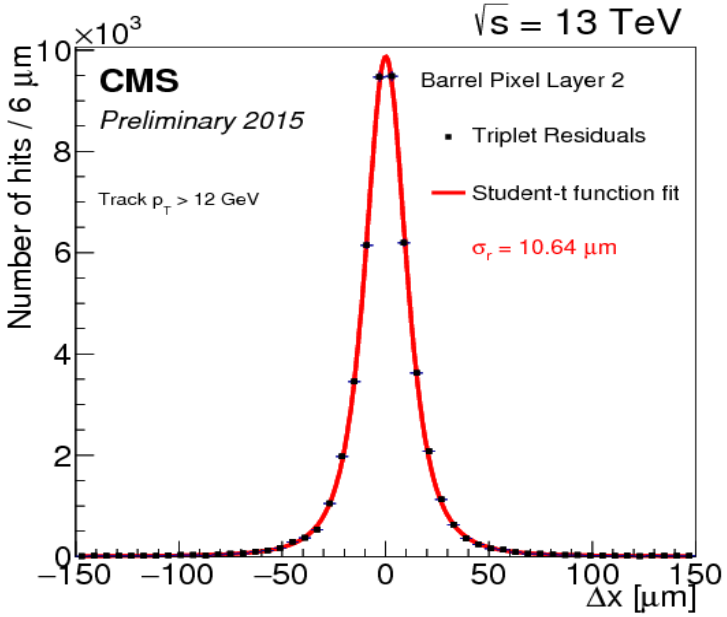
All electronics close to the detector will be affected.
Many SUEs remain unseen
e.g. a single pixel might stop to respond, no big deal (1 out of 66M).
But when a whole readout channel stops working (1 module) the result can be **very dramatic!**
The readout system of CMS stops and we (the pixel operators) suffer abuses from the rest of the collaboration.

Phase 1 Upgrade

Phase-0 pixel detector: performance evolution

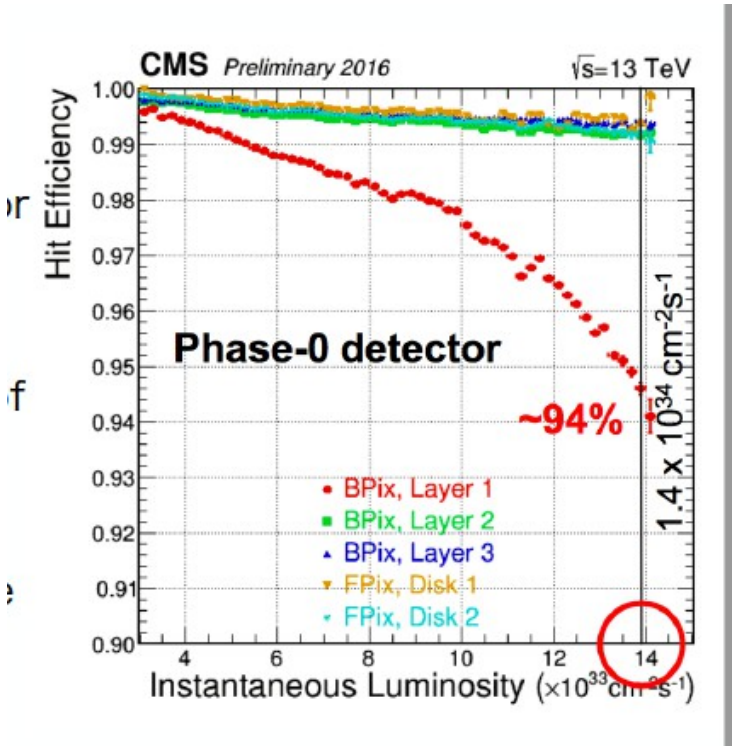
Pixel barrel position resolution measured with 2015 collisions.

Transverse (rϕ) direction



Position residual – 10.6 µm

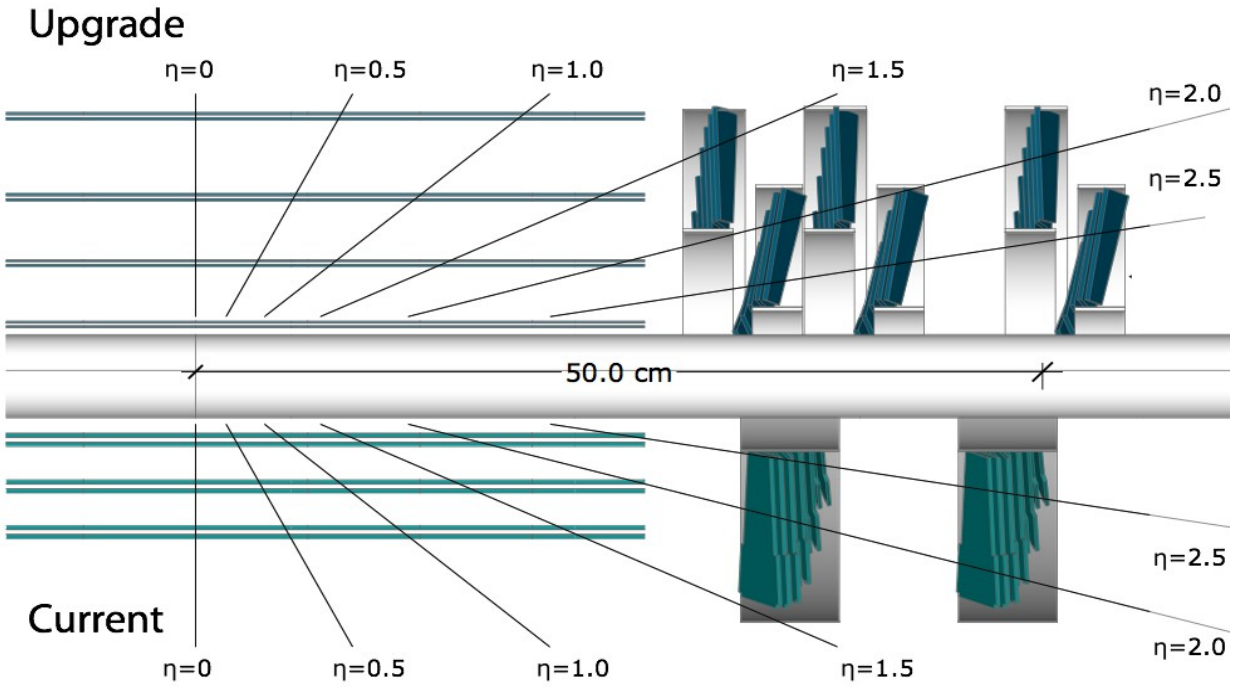
Hit efficiency versus luminosity



Loss of efficiency beyond 10^{34}

Upgrade project

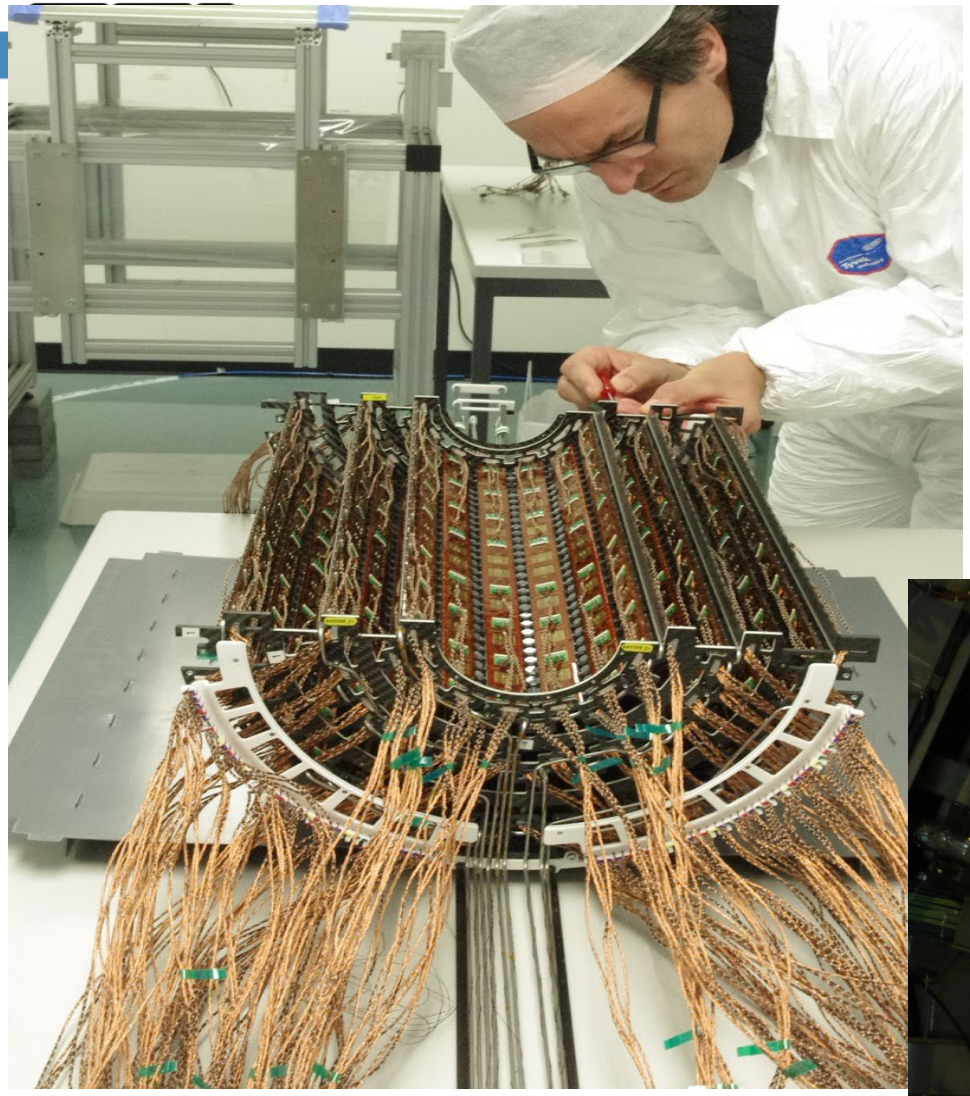
New upgraded pixel detector ("phase-1") Build in 2013-2016



4 (r_{min}29mm) barrel layers instead of 3 (r_{min} 43mm). 3 forward disks instead of 2.

BPix: by the CH (PSI, ETHZ, UZH), Germany (DESY, UH, Aachen, Karlsruhe), CERN/Helsinki/Taiwan and INFN-Italy.
FPix: USA (FNAL, Purdue, Nebraska, Chicago, Kansas, JHU)

Phase-1 Upgrade

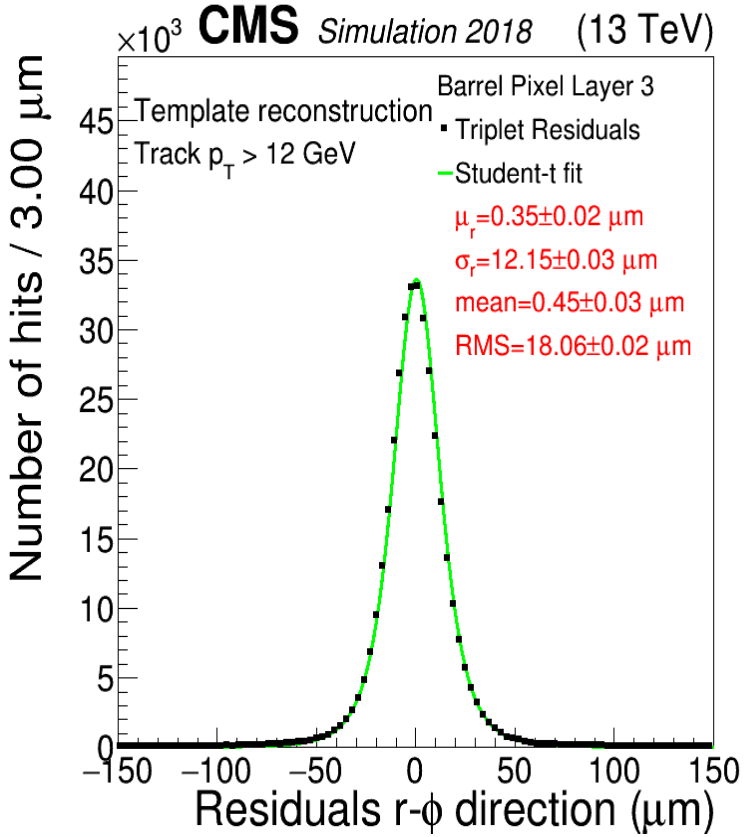


Phase-1 BPix detector
assembled at PSI in 10-12/2016

Transported to CERN 7/2/2017
Installation 28/2/2017

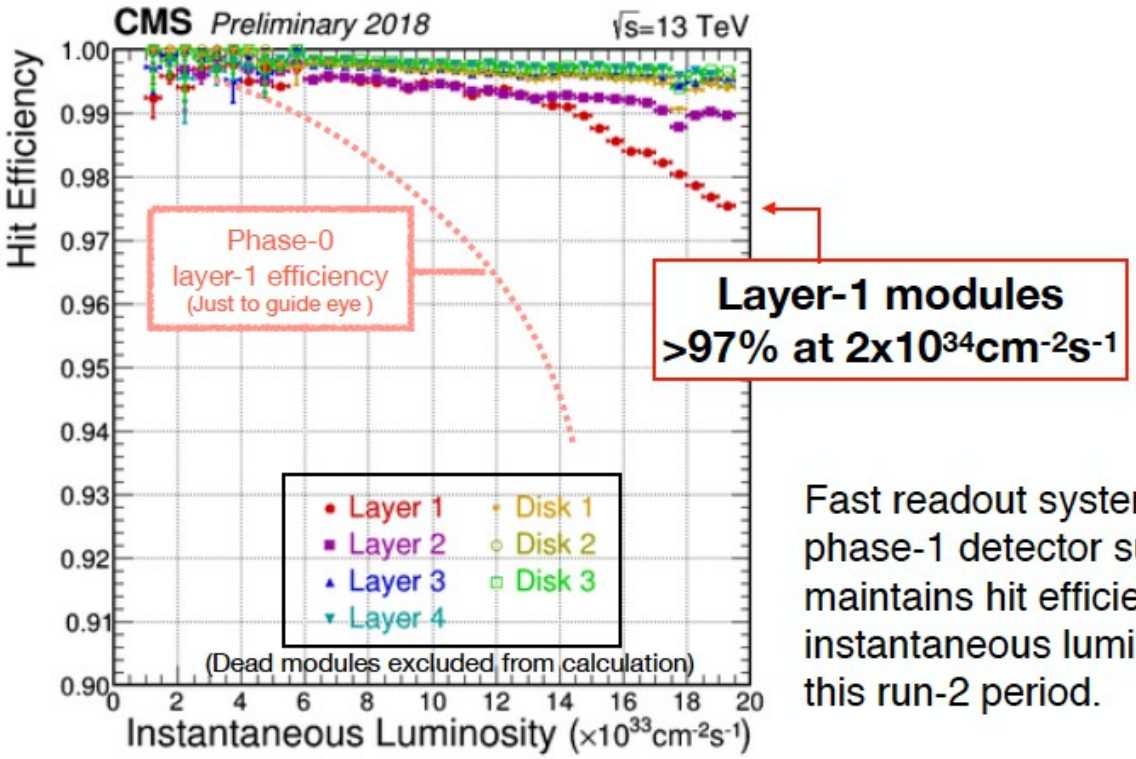
The new detector is performing very well

The Resolution is < 12µm



like in phase-0

Efficiency is much better than it would have been with the old phase-0 detector



Fast readout system of phase-1 detector successfully maintains hit efficiency for instantaneous luminosity of this run-2 period.

Phase 2 Pixel Detector Upgrade

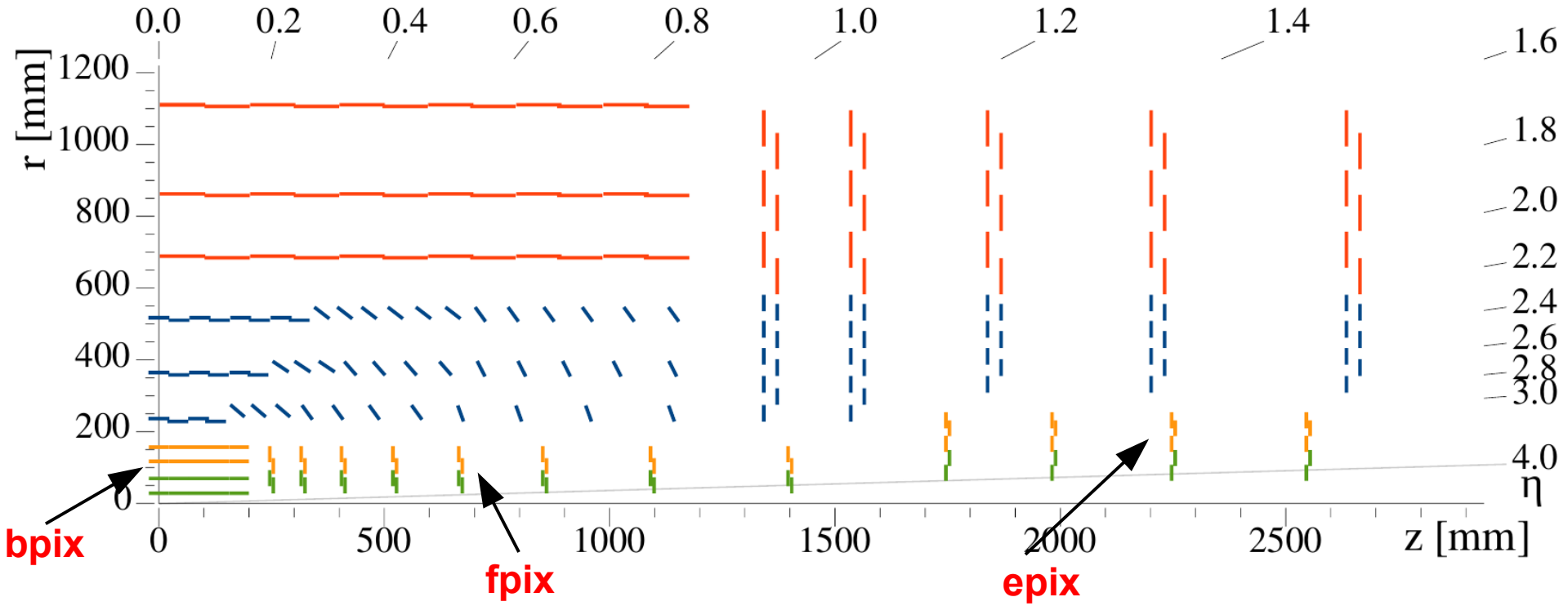
In the future (2026-35) the LHC collider will be upgraded to High-Luminosity.

The data rates will become 10 times larger and the radiation damage will increase 10 fold.

This new conditions will require a new pixel detector.

It is being designed now and will be installed in 2026 after the so called Long-Shutdown 3.
The design will be similar, the “hybrid”, type.

Phase 2 Pixel Detector Upgrade

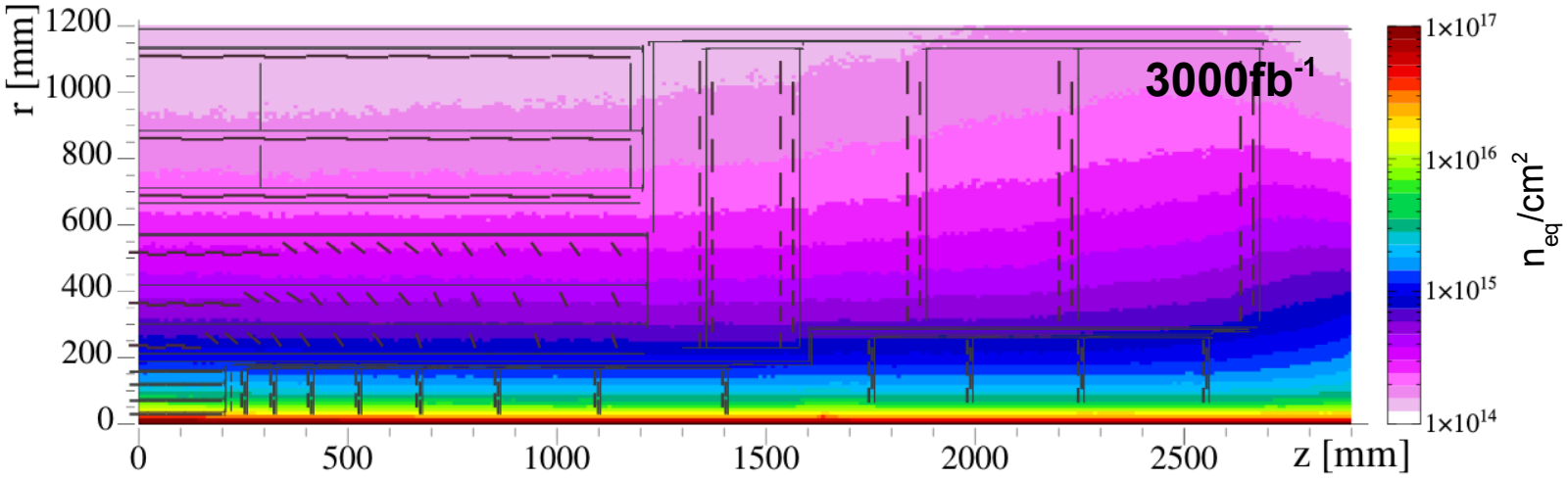


key features:

η coverage	**radiation hardness**	**finer granularity**	**L1 track trigger**
|η|<4.0 for forward signatures (VBF, VBS, b-tagging) **pixel: 12 disks**	rich sensor and ASIC R&D program for pixel and strips	<PU>=200: finer granularity to keep occupany small **factor: 4-6**	

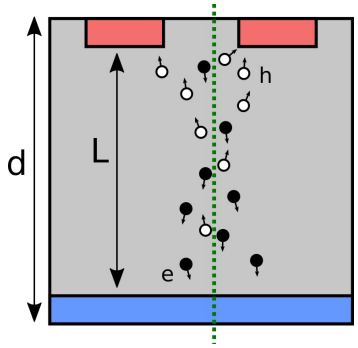
Phase 2 Pixel Detector Upgrade

- expected fluence: ~2x10^{16} n_{eq}/cm^2 in first layer
- charge trapping reduces signal cluster charge and thus single hit efficiency
- solution: reduce drift distance



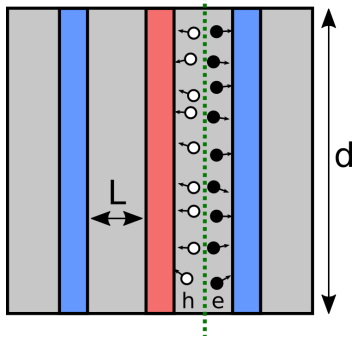
thin-planar sensor

- drift length L<200µm (now: 300µm)
- n-in-p (e signal)
- **outer** and **possibly also innermost layers/rings**

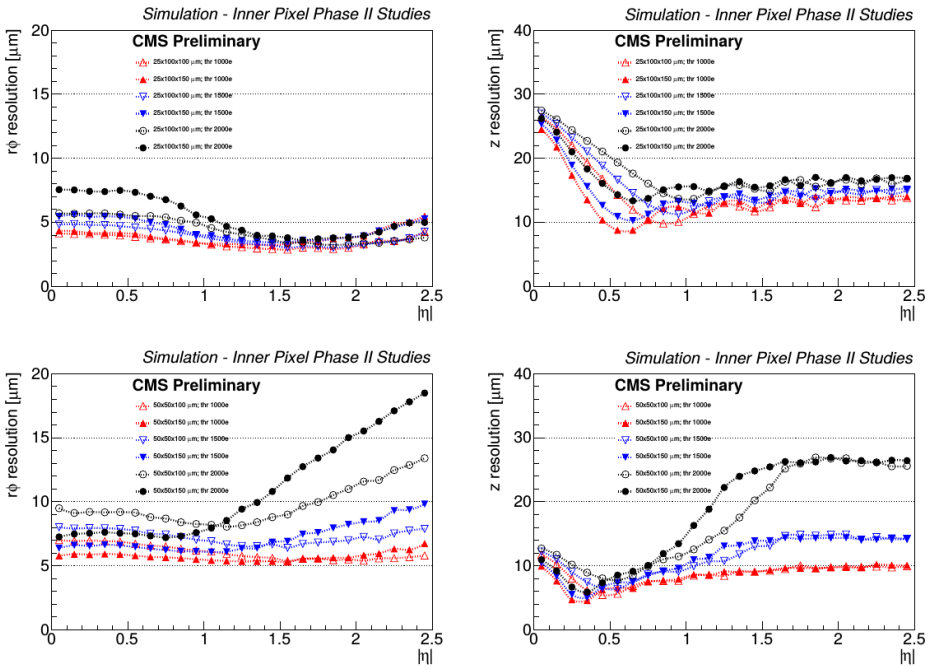


3D sensor

- shorter drift length L
- lower depletion voltage
- technically more challenging
- **inner layer (at most one)**



Phase-2 Pixels

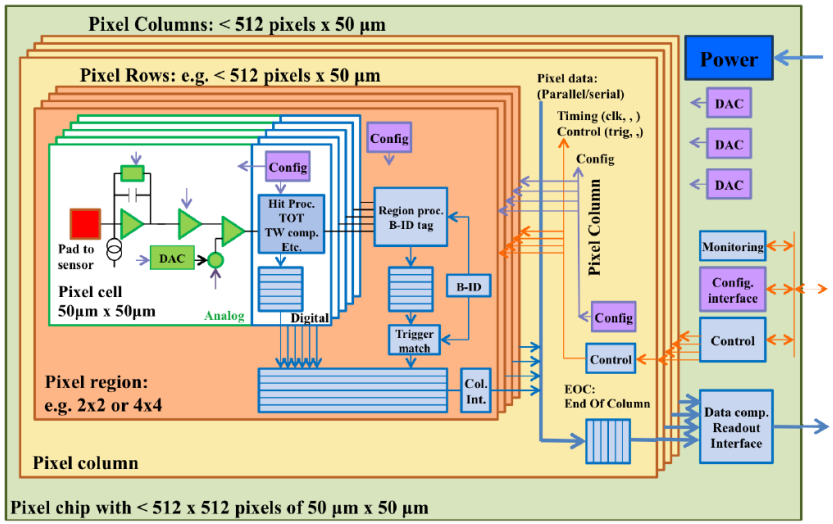


Pixel size

- affects
  - → two-track separation
  - → detector occupancy
  - → high-p_T-track resolution
- factor 6 smaller pixels:
  (50x50)μm² or **(25x100)μm²**
  current pixel detector: (150x100)μm²
  thickness 100-150 um.

Readout chip

- **RD53 Collaboration** (20 institutes, CMS+ATLAS) develops demonstrator chip for 2016
- **65nm CMOS** technology
  - → low power
  - → radiation tolerant (up to 1Grad)
- larger **hit rate** (2GHz/cm²)
- increased **trigger rate/latency** (1MHz/12.5μs)
- low effective **threshold** (~1000e)



Phase 2 Pixel activities

Our institute (PSI) together with the University of Zurich is involved in the building or Endcap pixels (“epix” or “TEPX”).
Also involved in TEPX are: Hamburg, Zagreb, Helsinki

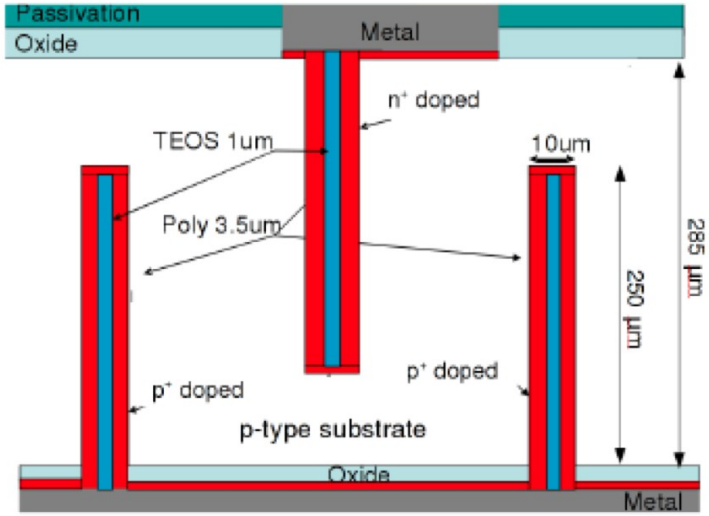
TFPX (Forward pixel disks) are build in USA.

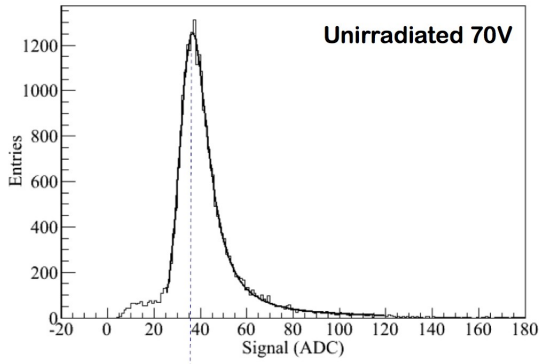
TBPX (Barrel) is build ETHZ (Zurich Technical University), Italy, Spain.

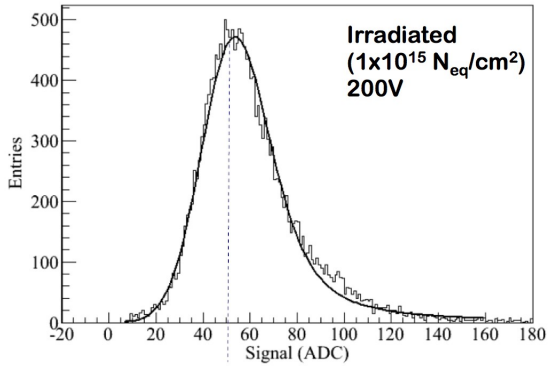
New pixel detectors

Charge Collection in 3D Detectors

Idea from Parker & Kenney







- short charge collection distance (GOOD)

  insensitive regions for tracks passing through electrode pillars.

  e.g. 90^0 tracks (BAD)

- interleaved electrode pillars → capacitance (BAD)

CMOS particle sensors (MAPS)

Use signal from ionizing particles in CMOS bulk.

commercial standard CMOS process -> low cost

signal collection by diffusion only -> speed, spread

typical signal ~ 1000 electrons on n-wells contacts

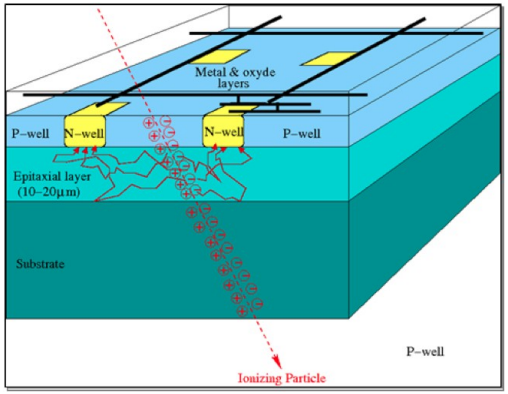
typically few unipolar pixel transistors in p-well

very small pixels with very low noise ~20electrons

rolling shutter to avoid random chip internal X-talk

well suited for high precision & low rates

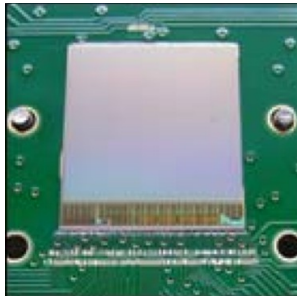
0-suppression in CMOS periphery -> digital readout

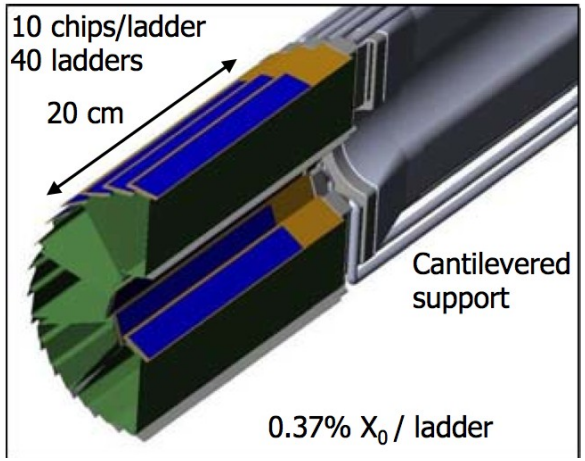


STAR Pixel Upgrade (planned for 2014)

- 2 layers at 2.5cm / 8cm
- Mimosa 28 chip ("Ultimate") in AMS-0.35 CMOS
  Developed by the group from Strasbourg
  (P. Winter & W. Dulinski))

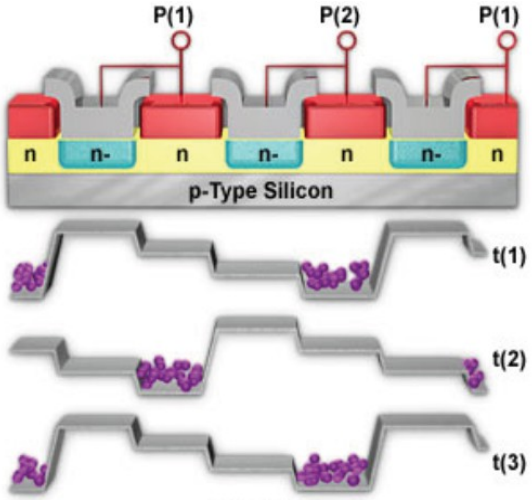
- pixel size 20.7
- chip size 20mm x 23mm
  position resolution ~10
- 200 nsec per row scan





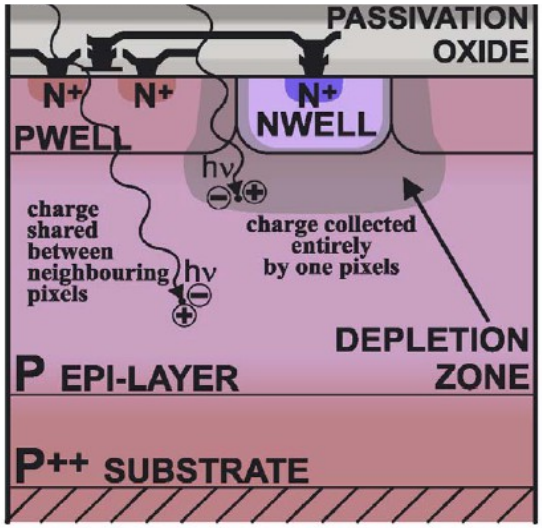
Pixel detector comparison

CCD

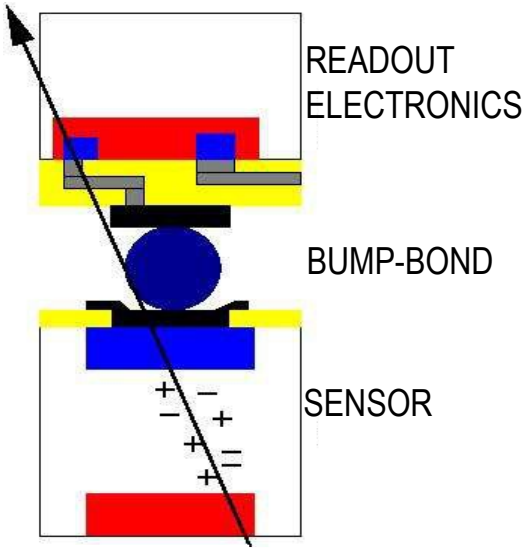


Monolithic Pixel and DEPFET

(many variants)



Hybrid Pixel



Pixel area	25 μm²	400 μm²	10000 μm²
Speed	< 1 kHz	kHz - MHz	> 10 MHz
Radiation hardness	< 50 krad	< 20 Mrad	> 250 Mrad
Applications:	SLD@SLAC, R&D for pixels@ILC	STAR@RHIC (MAPS), BELLE@SuperKEKB (DEPFET), Alice, mu3e R&D for pixels@ILC	CMS,ATLAS&ALICE@LHC SLHC upgrades

Thank you for your attention.

Spare slides

Detector Performance – Example I, Atlas

Charge measured in the Atlas pixel detector used for DeDx type of measurement, to distinguish different particle types: μ/π, K, p, d.

Proves that the charge resolution is very good and that the analog signal calibration is (almost) perfect.