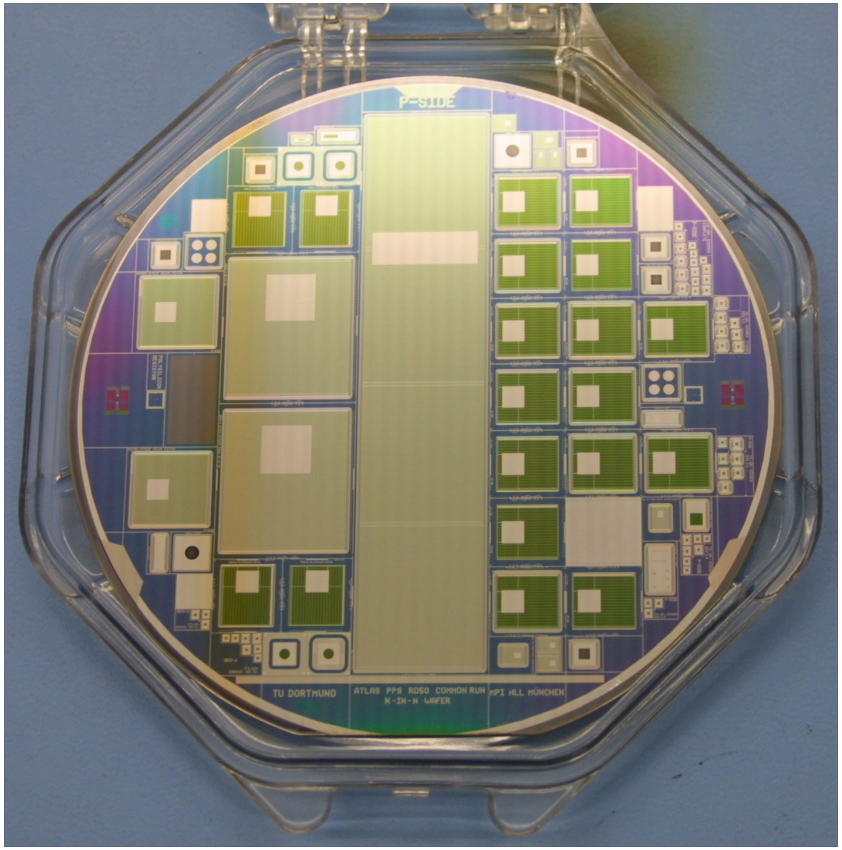
Status of the n-in-n CiS pixel production 2009

André Rummler, Tobias Wittig

TU Dortmund

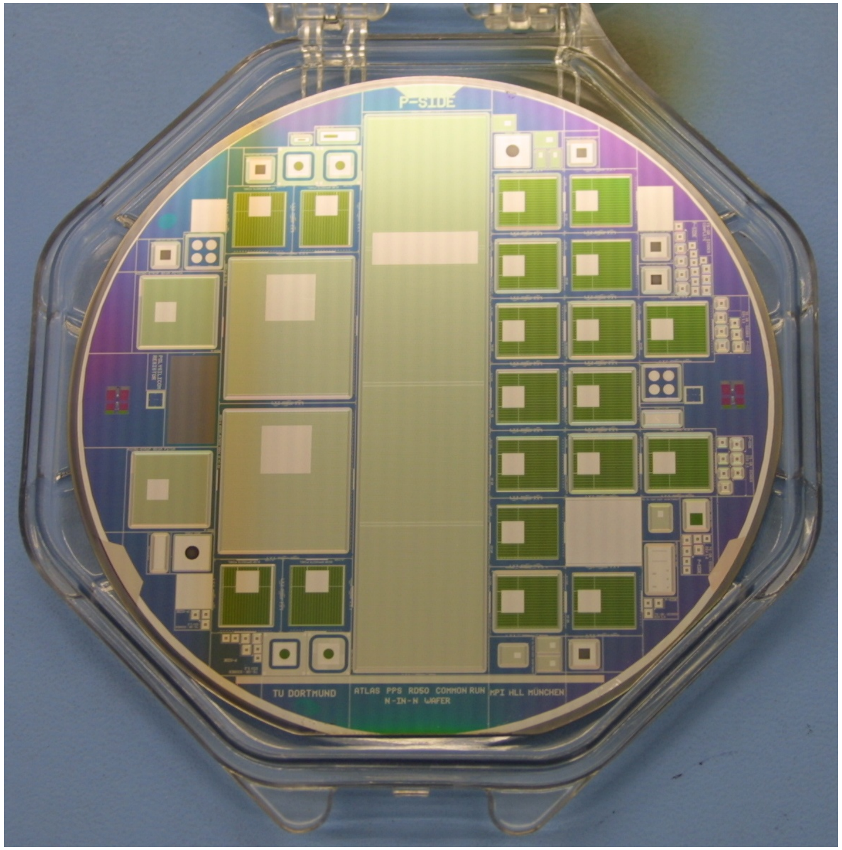
General overview

- joined submission of the ATLAS Upgrade Planar Pixel Sensor (PPS) collaboration and RD50
- Aims:
    - first planar n-in-n FE-I4 sensors for ATLAS insertable b-layer (IBL)
    - investigation of reducing the inactive sensor edges
    - charge amplification studies



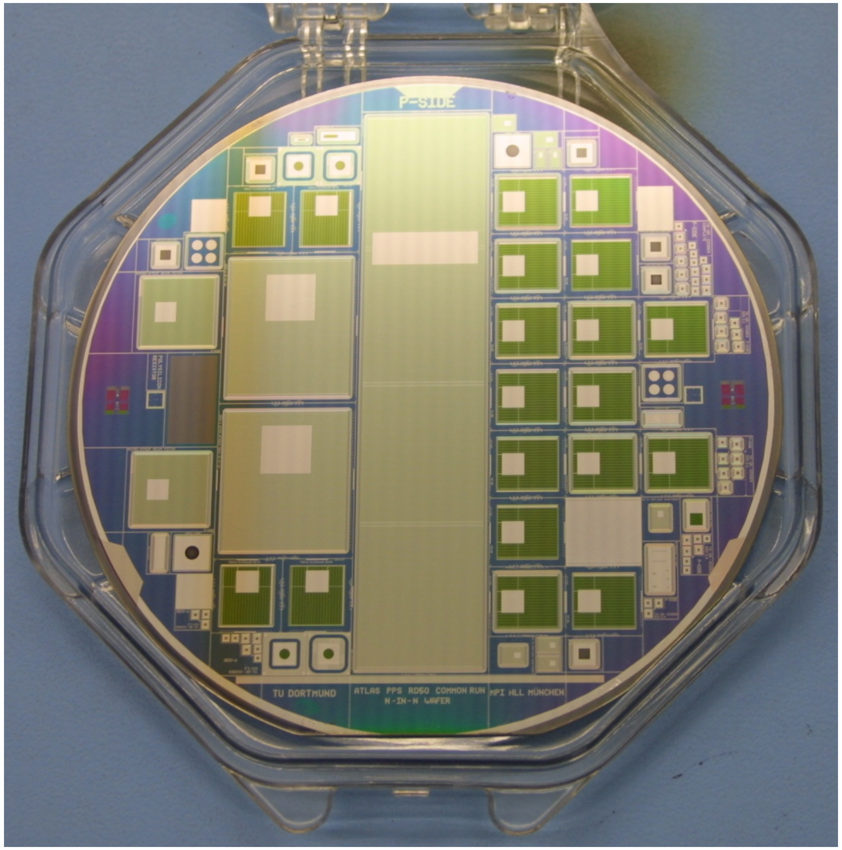
General overview

- vendor: CiS
- 4'' n-type wafer (double sided)
- thickness 285µm
- Two bulk materials:
    - DOFZ: 12 wafer
    - MCz: 12 wafer



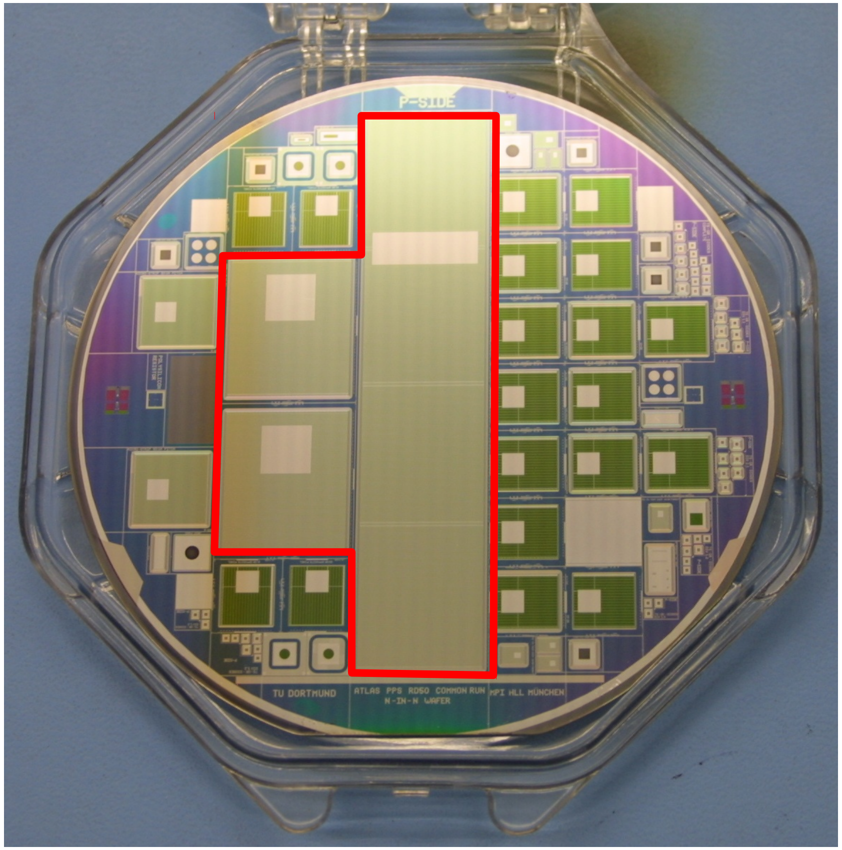
Layout overview

- Many different kinds of structures
    - FE-I4 related sensors
    - FE-I3 related sensors
    - test structures
        - guard ring diodes
        - ROSE diodes
        - GCD
        - Mosfets
        - sensors for test chips



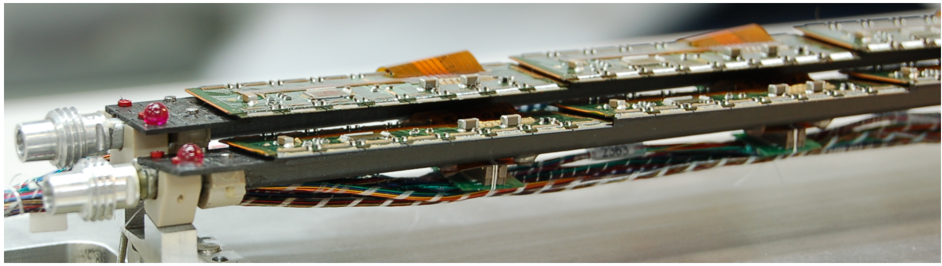
FE-I4 related sensors

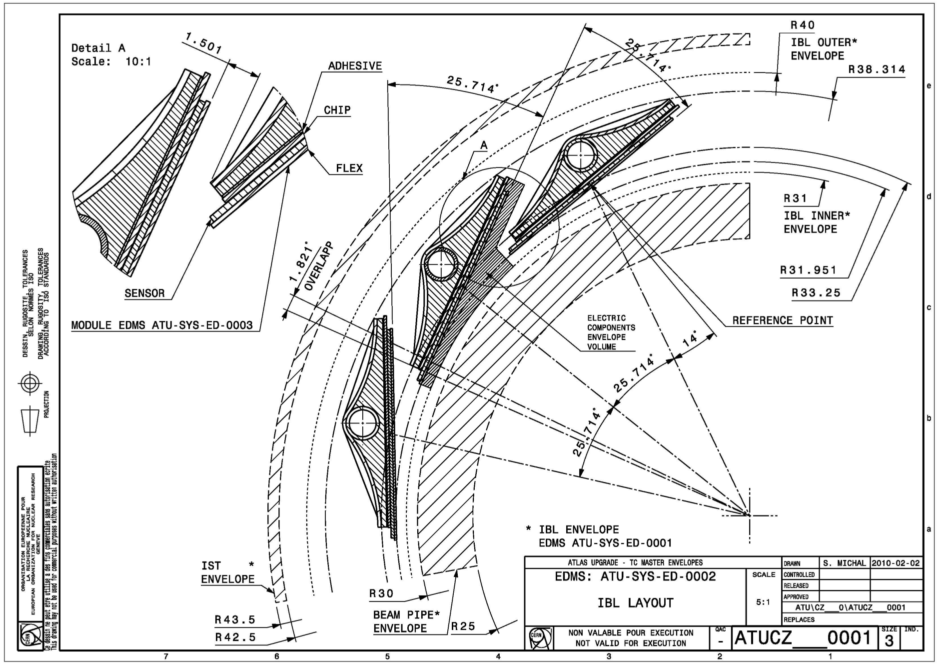
- 1 1x4 MultiChipModule
  - Last year still one of the possible IBL sensors
- 2 SingleChip sensors
  - first adapted n-type sensors for FE-I4 tests and irradiations



Summary: IBL

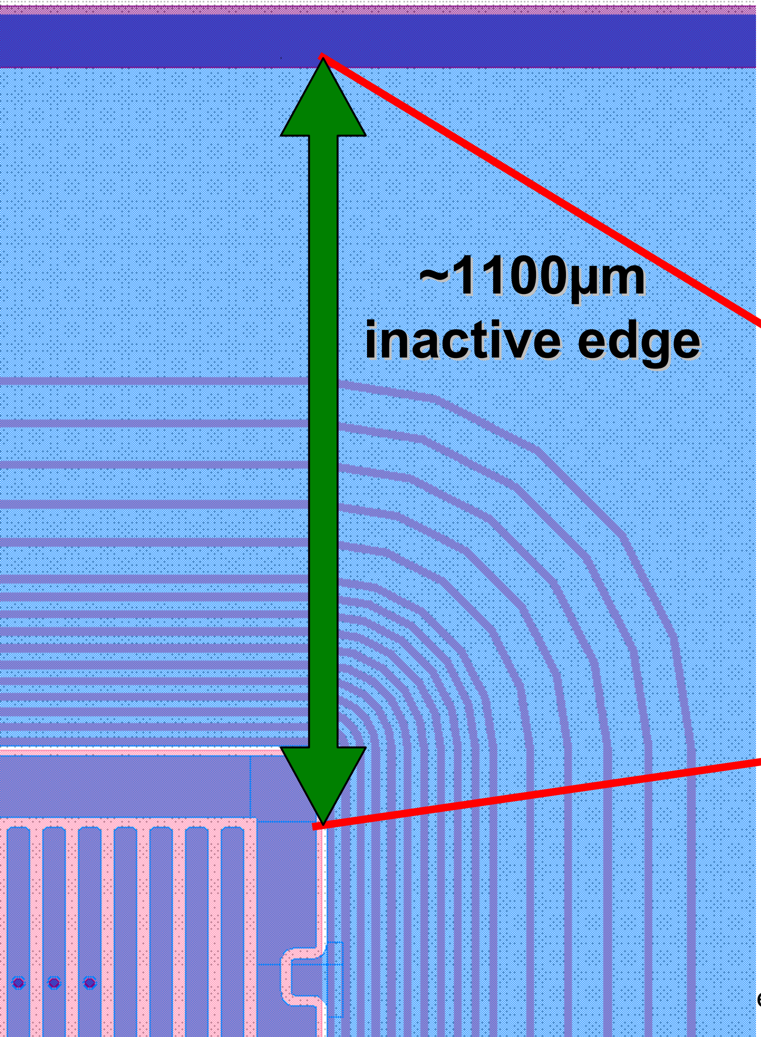
- it is planned to insert an additional layer into the current ATLAS pixel detector
- has to be mounted directly on the new beam pipe
- shingling of the modules (as on the other layers) is no longer possible
- the inactive sensor edge has to be reduced

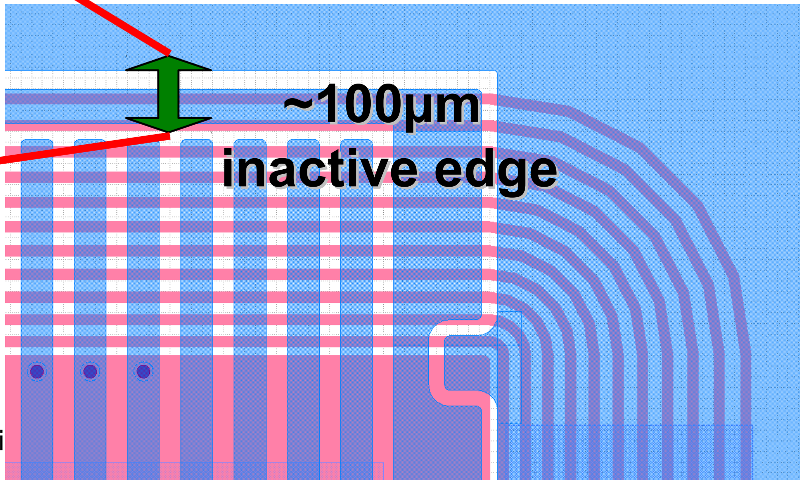




FE-I3 Compatible Sensors for Slim Edge

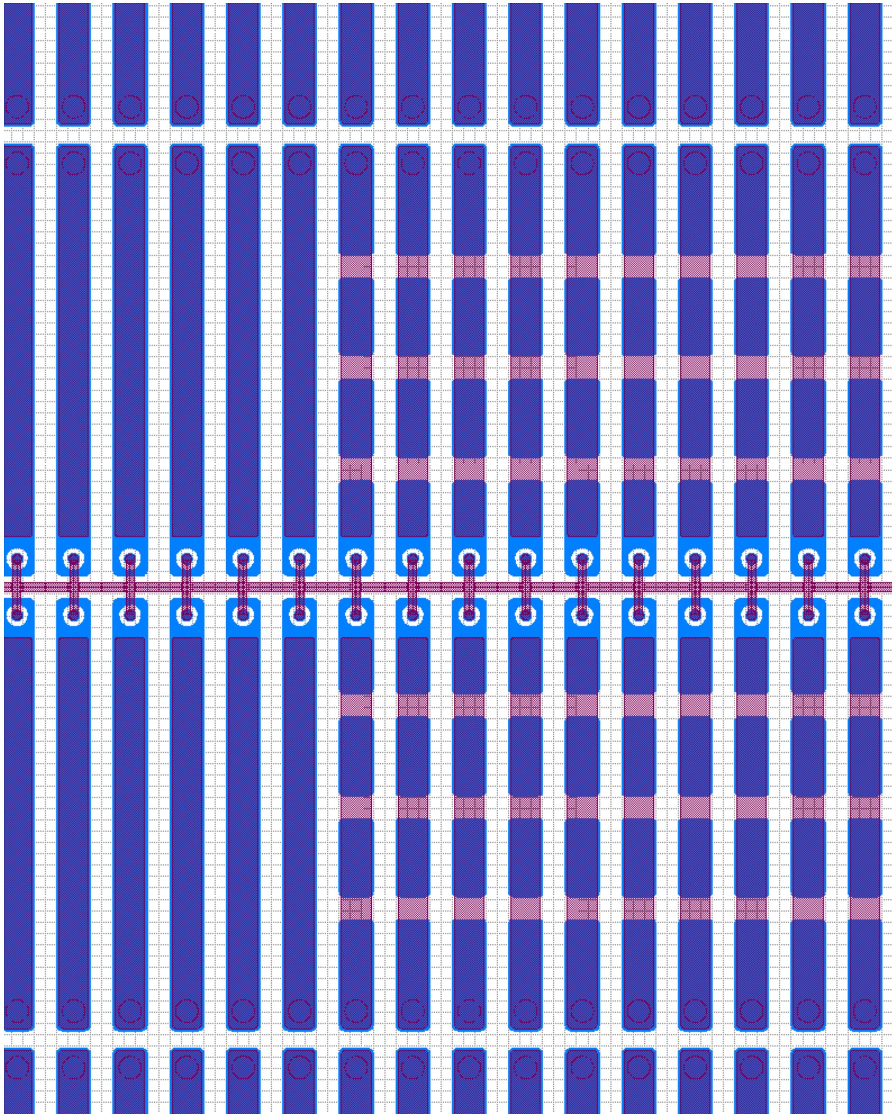
- Several versions of sensors to investigate the feasibility of reducing the inactive edge (Slim Edge)
  - reducing the number of guard rings
  - shifting the guard rings beneath the active area
  - combinations of both





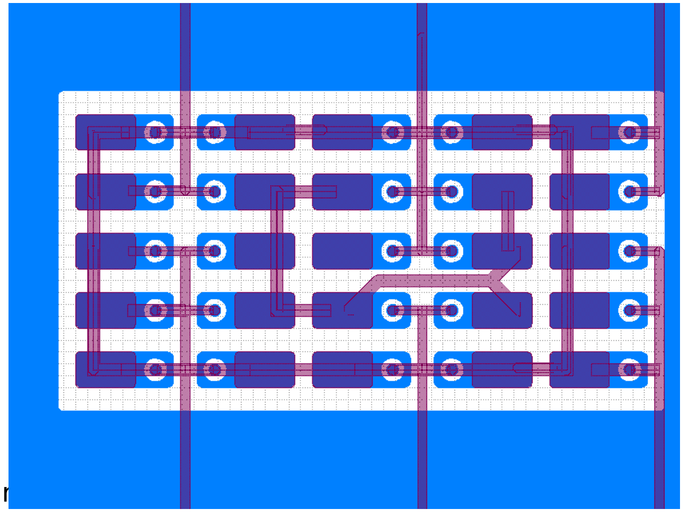
Sensors for charge amplification studies

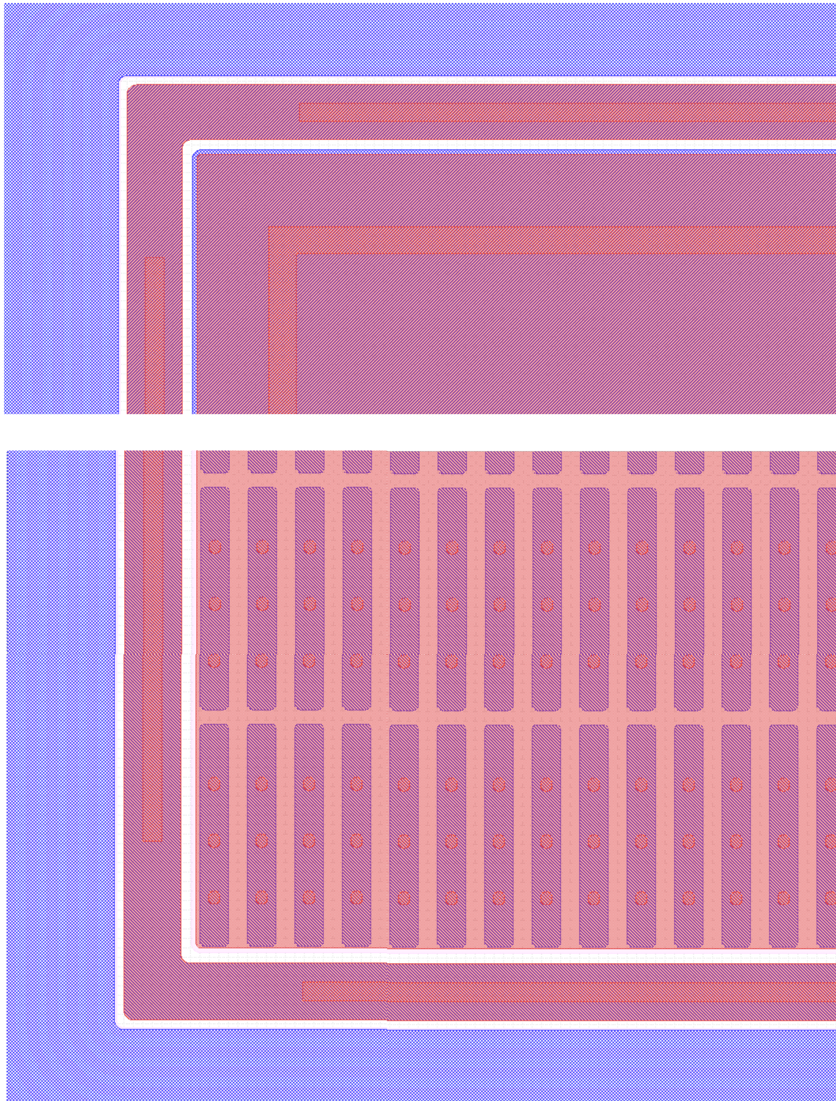
- One FE-I3 SingleChip sensor has an array of segmented pixel implantations (implants still connected by metal)
    - the segmented pixels might yield regions of increased charge amplification
    - After irradiation we are able to compare directly changes in charge amplifications between segmented and normal pixels



Teststructures for charge multiplication

- Guard ring diodes with a pad-like and a pixaleted area
  - Changes of CCE between the two versions
- Interpixel structure for a simple readout of single pixels



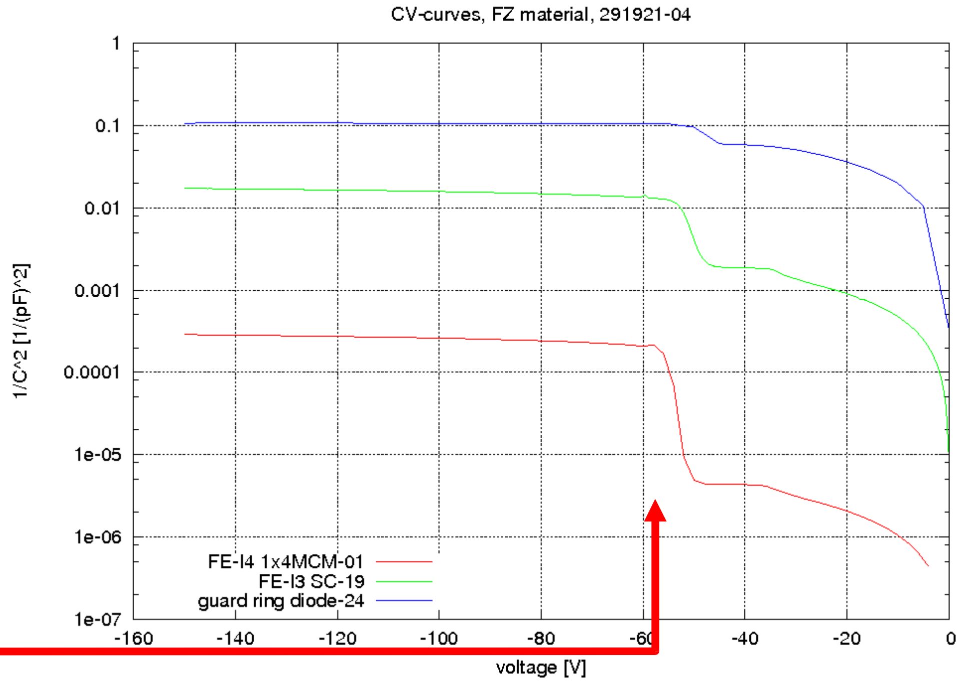


Status of production / delivery

- 9 FZ wafer are currently in Dortmund for quality assurance measurements (IV)
  - UnderBumpMetal was deposited at IZM
  - 7 wafers have already been diced at TU Dortmund
- 3 FZ wafer are in Barcelona
  - for a different UnderBumpMetal technique (electroless process, → lower cost)
  - to investigate the feasibility of anisotropic trench etching
- 12 MCz Wafer just delivered by IZM

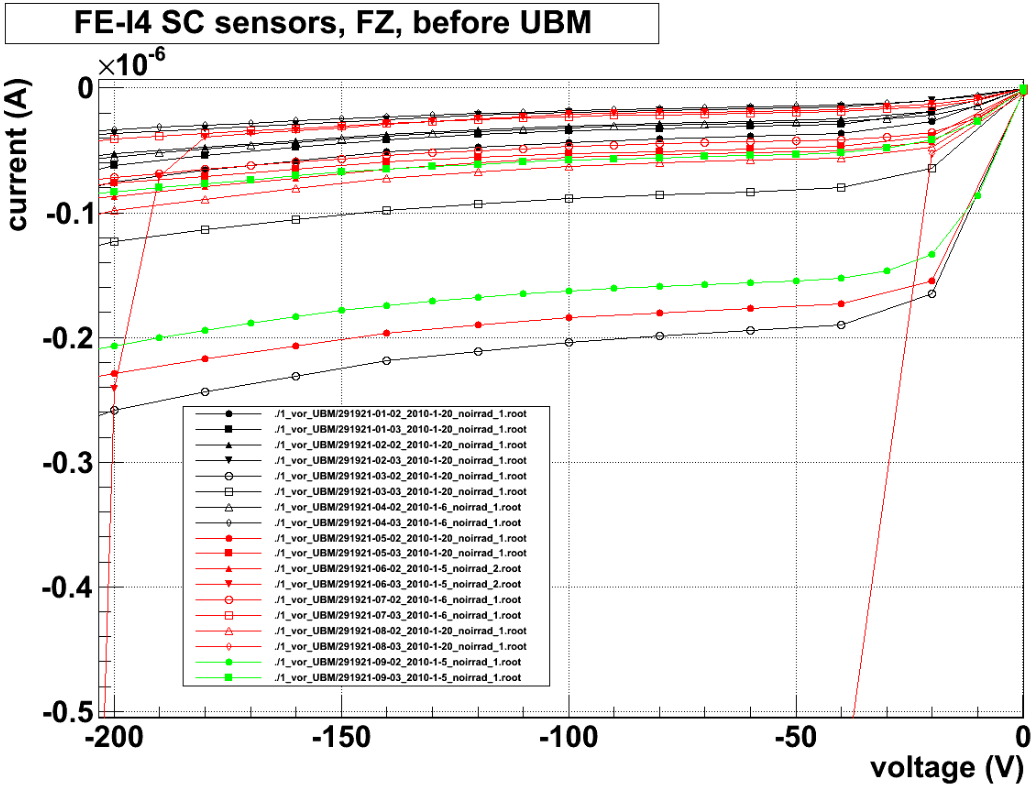
ATLAS quality assurance criteria

- $V_{breakdown} > V_{depletion} + 50V$
- leakage current must not reach
  - 100nA for FE-I3 SC
  - 500nA for FE-I4 SC
  - 2000nA for FE-I4 MCM
- $V_{depletion}$ determined by CV measurements
  - FZ: ~55V
  - MCz: ~400V → $V_{depletion}$ too high due to low bulk resistivity→ foreseen to be measured after irradiation



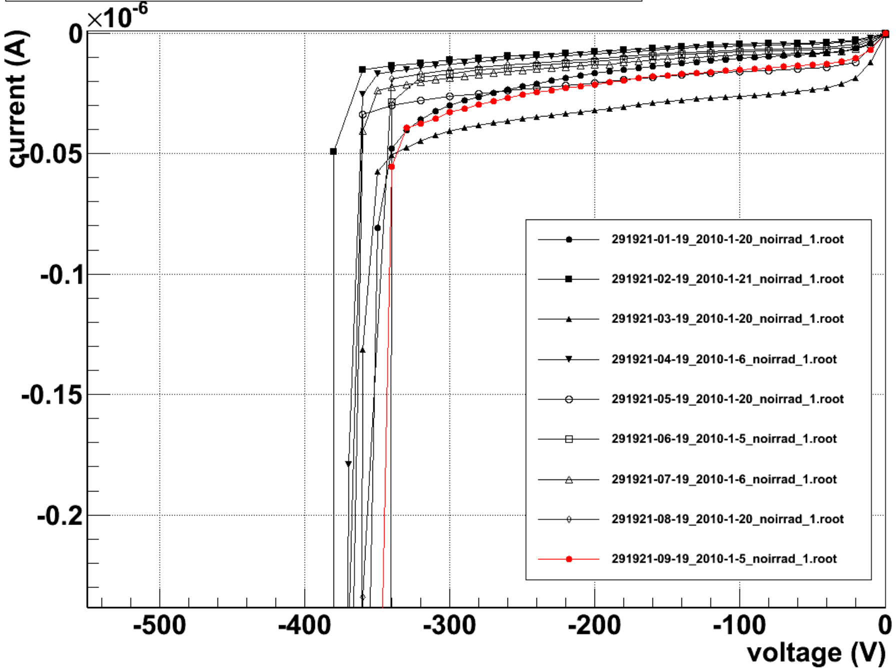
Yield before UBM

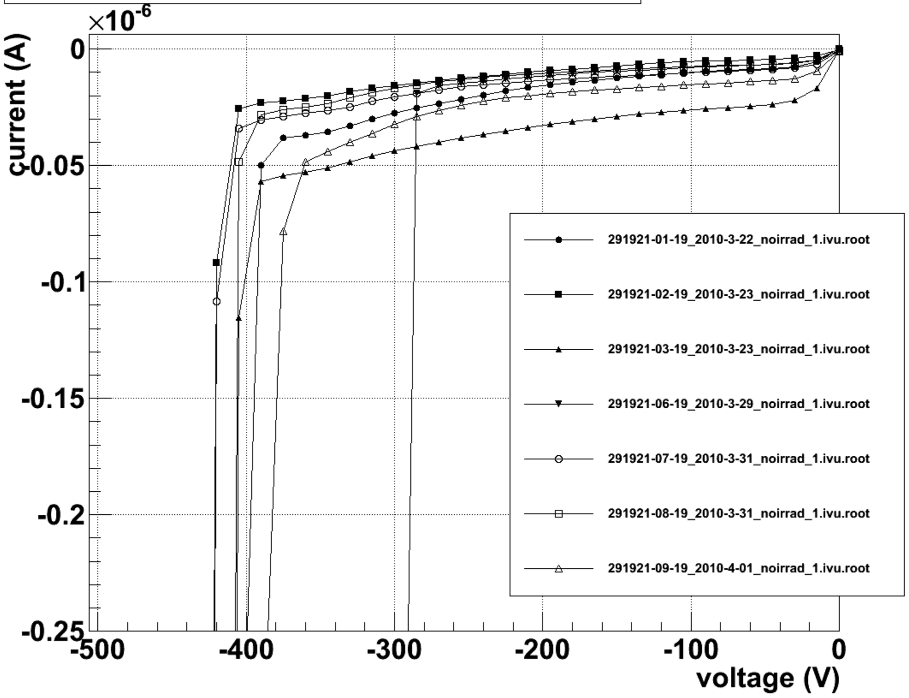
- yield after delivery from CiS was quite high
- good FZ sensors:
  - FE-I4 1x4 MCM: 6 of 9
  - FE-I4 SC: 17 of 18 →
  - FE-I3 SC: (conventional design) 9 of 9



Yield after UBM

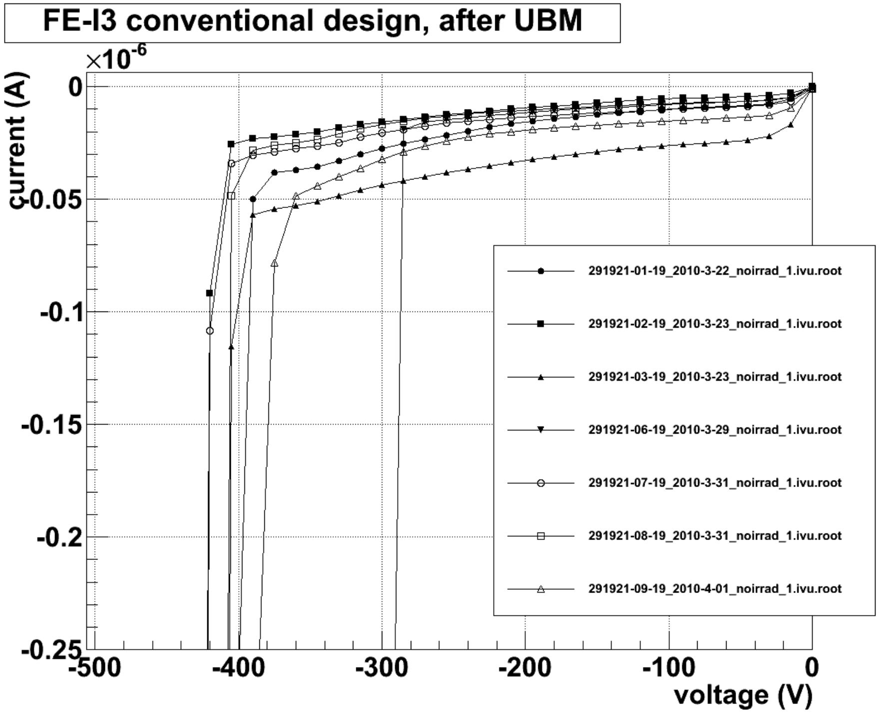
- UBM process didn't worsen the breakdown voltage significantly
- (for some sensors types the breakdown voltages increased, for other ones decreased)

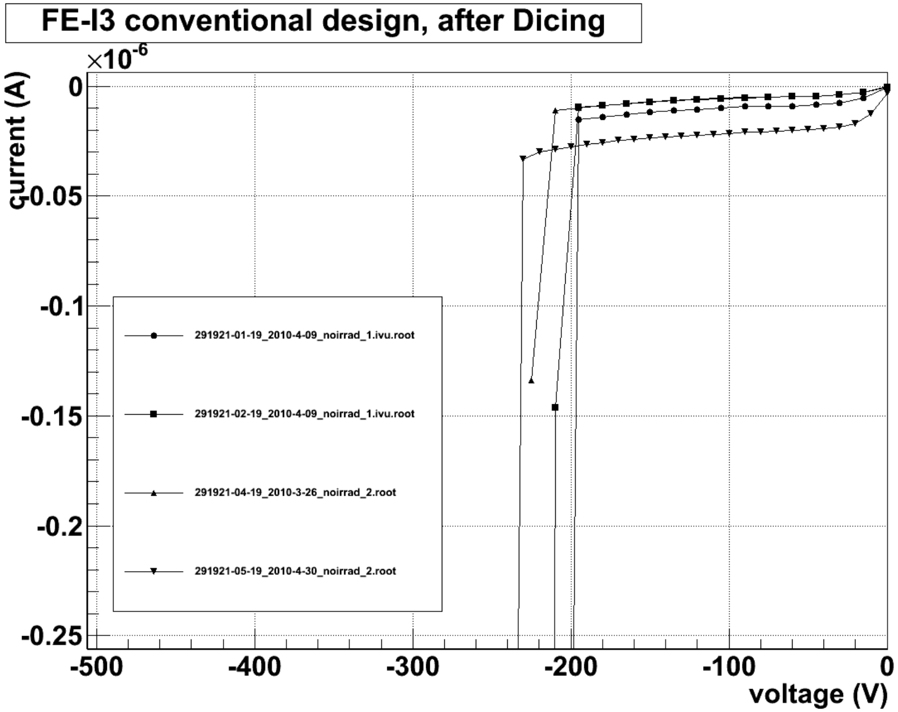

FE-I3 conventional design, before UBM


FE-I3 conventional design, after UBM

Standard dicing (along dicing street)

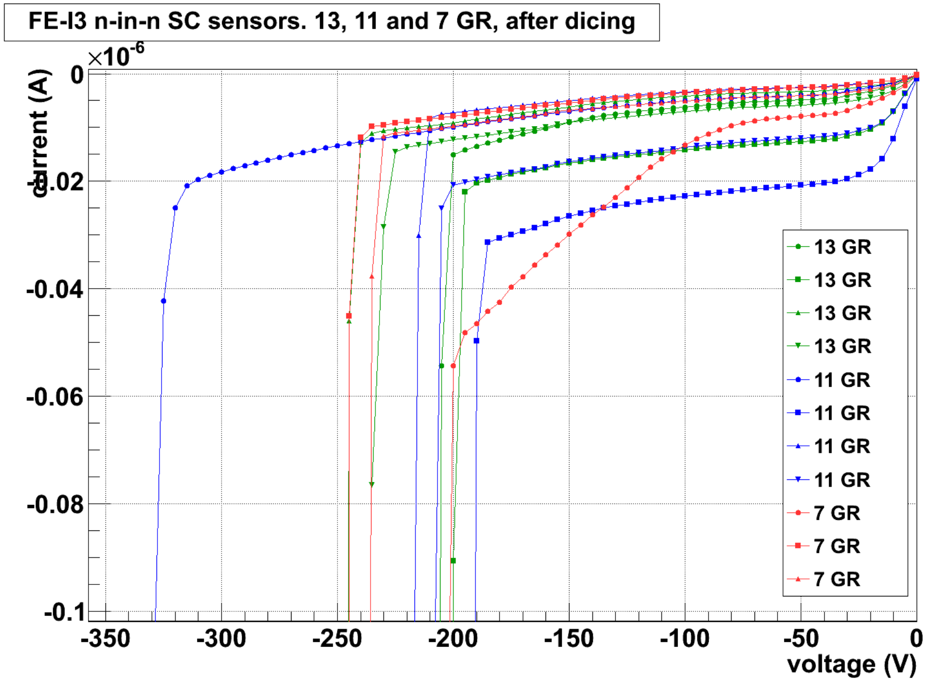
- Reduction of breakdown voltages occur after the dicing process which can be explained by contaminations caused by the diamond dicing saw
- The ATLAS quality assurance criteria (breakdown voltage >~105V) is still fulfilled

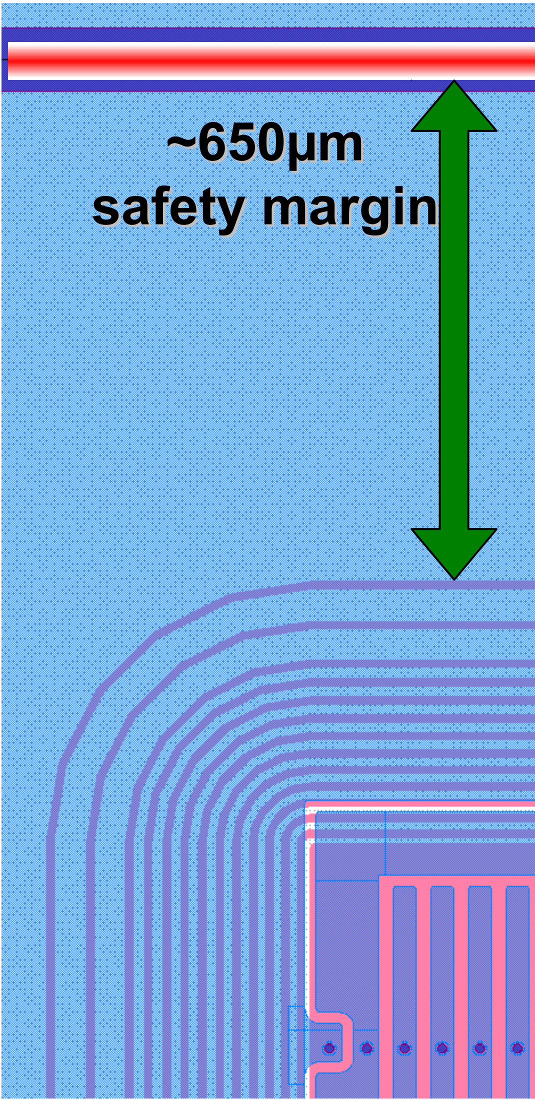




Reduced number of guard rings

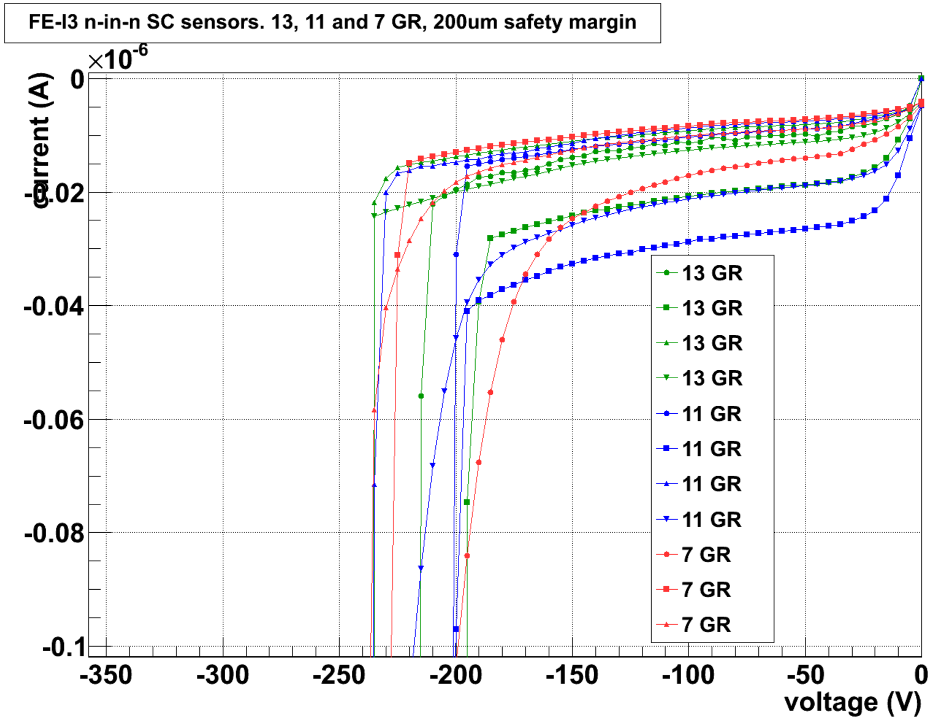
- Comparison of FE-I3 sensors with reduced number of guard rings (13, 11 and 7), diced at the dicing street (~650-850µm safety margin)
- no significant differences can be seen
- The breakdown voltage after dicing is still high enough to fulfill ATLAS quality assurance criteria ($V_{breakdown}$ >105V), even with 7 guard rings

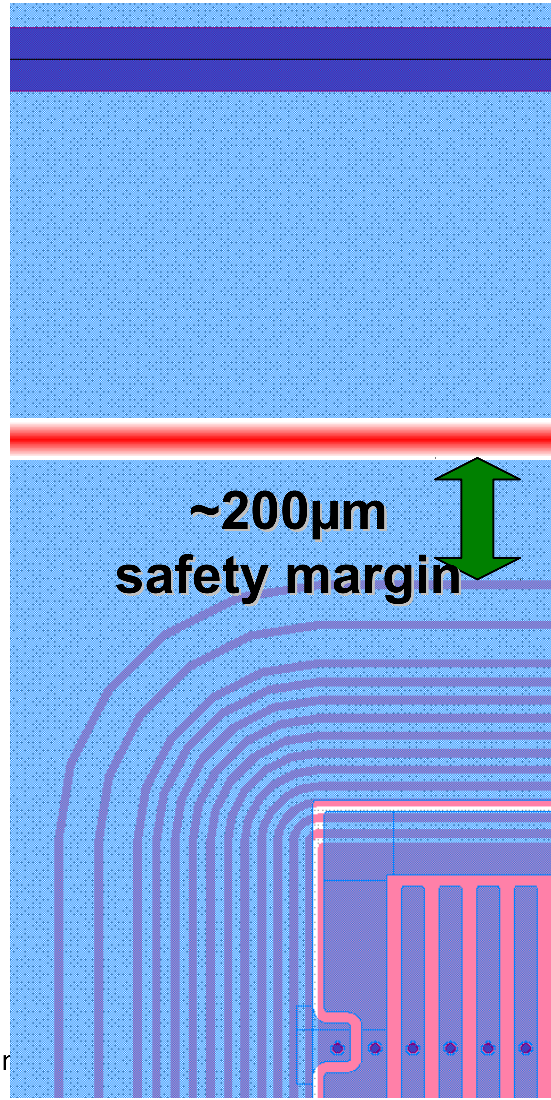




Results of slim edge dicing trials

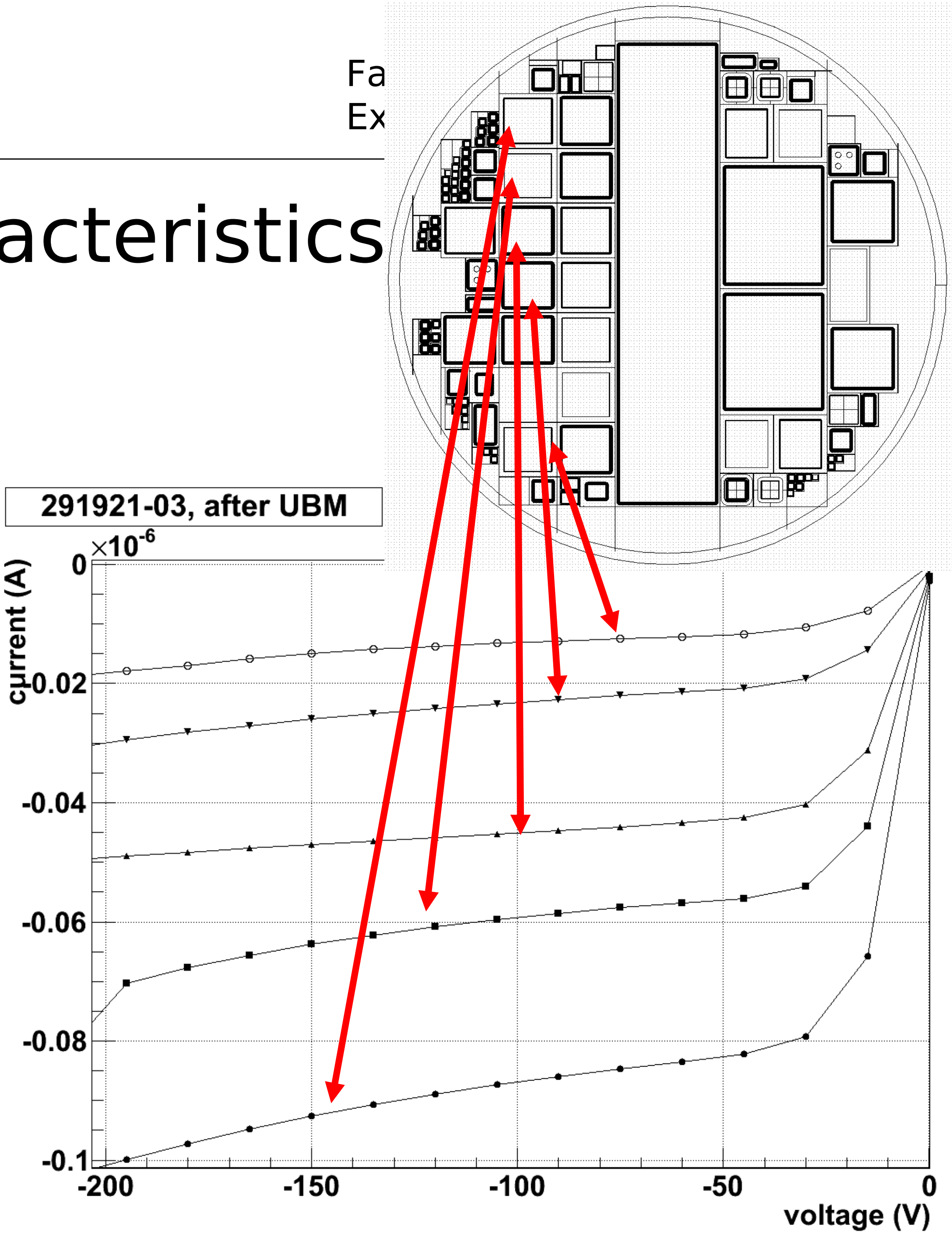
- FE-I3 sensors with reduced number of guard rings (13, 11 and 7) have been cut 200µm next to the last guard ring
- No significant changes in comparison to dicing along the dicing street despite large reduction of safety margin





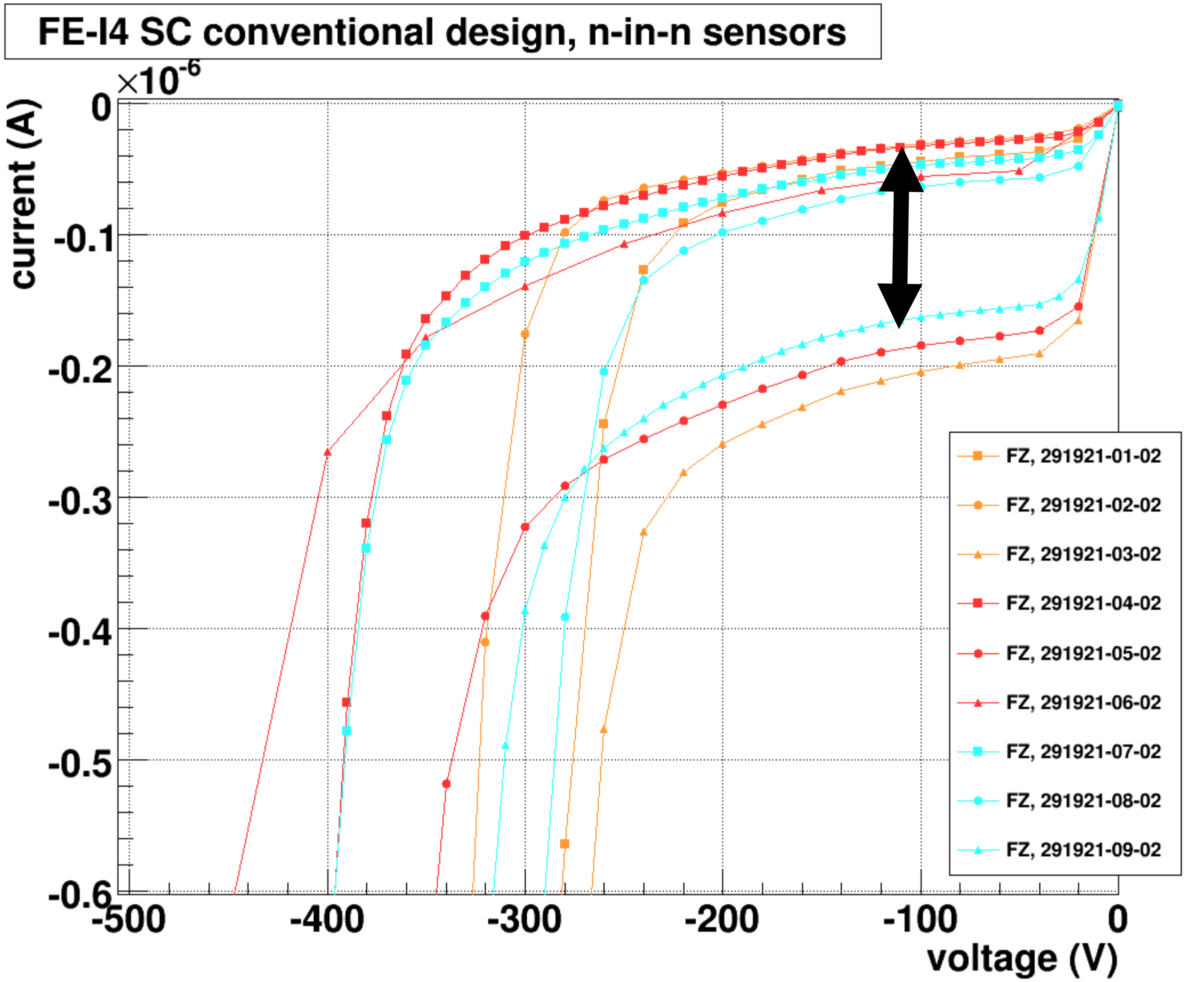
Global wafer characteristics

- Level of leakage current dependent of position on the wafer
    - at the top up to 5 times higher than at the bottom (before irradiation)
    - even the highest leakage currents are still acceptable



Global wafer characteristics

- Level of leakage current of three FZ wafers is a bit higher than the leakage current of the other six wafers
- even the highest observed leakage currents are fully acceptable



Irradiation plans (preliminary)

- FZ material
    - Slim Edge samples
        - Neutron irradiations with IBL fluences ($2 \cdot 10^{15}$ n_{eq}/cm² and $5 \cdot 10^{15}$ n_{eq}/cm²) as well as SLHC inner layer fluences for CCE measurements in test beam
    - Samples for investigations of charge amplification
        - Neutron irradiations up to SLHC fluences ($5 \cdot 10^{15}$ n_{eq}/cm², $10 \cdot 10^{15}$ n_{eq}/cm² and $20 \cdot 10^{15}$ n_{eq}/cm²)
- MCz material
    - mixed irradiations (protons and neutrons) to emulate SLHC outer layers
        - to investigate the effects of bulk damages compensation in this region
    - two whole wafers shall be irradiated to the minimum of N_{eff} to decrease $V_{depletion}$ (at the moment >400V, → often higher than the breakdown voltage)