Outlook on the 2010 n-in-n CiS pixel production on thinned silicon

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Within the framework of the ATLAS Upgrade Planar Pixel Sensor R&D Project (PPS) and with additional input from RD50 members, a new production of n-in-n sensors is currently under way at CiS. The production is carried out on n-bulk 4" DOFZ wafers with thicknesses ranging from $250\mu m$ down to $150\mu m$ in $25\mu m$ steps. The wafer layout contains sensors adapted to the future ATLAS readout chip FE-I4 suitable for the ATLAS insertable b-layer (IBL).

Further structures (mainly FE-I3 compatible pixel sensors and pad detectors) on the wafer are dedicated in large part to the investigation of charge amplification effects in pixel sensor geometries and their dependence on electric field distributions due to the different bulk thickness and implant boundary configuration.

Another principal focus of the test structures on this wafer are studies of the guard ring system in order to minimize the non-active sensor area.

The presentation will give an overview of the wafer layout, the production time schedule and a tentative irradiation plan.

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