Status and plans of the n-in-p CiS pixel production

Anna Macchiolo
Max-Planck-Institut für Physik, Munich

on behalf of the groups participating in the project

- Layout and results of the n-in-p pixel characterization
- Preparation of the sensors for the interconnection to the ATLAS pixel electronics
- Investigation of alternative dicing methods to achieve slim-edges
- Tuning of a TCAD simulation for planar devices with the present n-in-p production

16th RD50 Workshop, Barcelona, 1st June 2010

R&D for Planar Pixel Sensors for SLHC

- Common RD50 production with the contribution of:
  - ATLAS groups participating in the Planar Pixel Sensor Project (coordinator C. Gössling, TU Dortmund), established in view of the Insertable B-Layer upgrade and SLHC:
    - IFAE-Barcelona
    - ATLAS Pixel group CERN
    - TU Dortmund
    - MPI Munich
    - LAL-Orsay
    - LPNHE - Paris
    - Prague
  - CMS pixel group at PSI
- R&D areas to be covered by this project:
  - Comparison of performances between n- and p-bulk pixels: yeald, reliability, radiation hardness
  - Slim edges, increase of the fraction of active area
  - Cost reduction
  - Vertical integration

Production parameters

- Production with CiS (Erfurt, Germany) on 4” wafers
- Parallel production of n-in-p and n-in-n wafers with several common test devices to achieve a full comparison between the two technologies

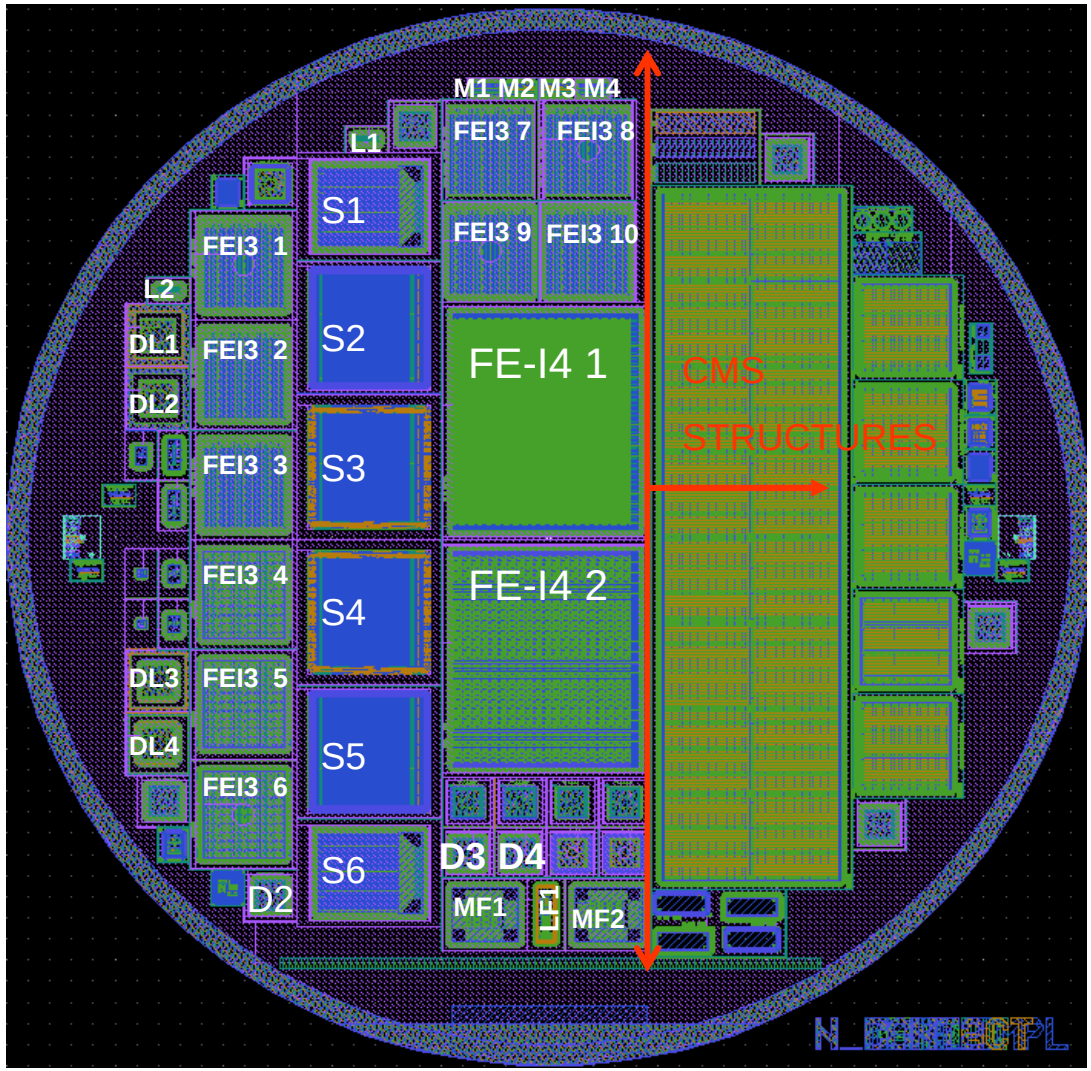
n-in-n batch	12 Fz wafers	12 MCz wafers	Double sided process
n-in-p batch	34 Fz wafers	6 MCz wafers	Single sided process

	Resistivity [KΩ.cm]	Thickness
FZ n-type	3.5-5.7	285
MCZ n-type	0.85-1	300
FZ p-type	> 10	285
MCZ p-type	> 2	300

- N-in-n and n-in-p batches delivered at the beginning of 2010

Layout of the CiS n-in-p pixel production

- FE-I3: present ATLAS pixel electronics
- FE-I4: new electronics for the ATLAS Insertable B-Layer



FEI3-1 to FEI3-3: Standard GR, homogeneous p-spray

FEI3-4 to FEI3-6: Standard GR, moderated p-spray

FEI3-7 – FEI3-8: 8 GRs, homogenous p-spray

FEI3-9 – FEI3-10: 15 GRs, homogeneous p-spray

FEI4-1 : standard GR, homogeneous p-spray

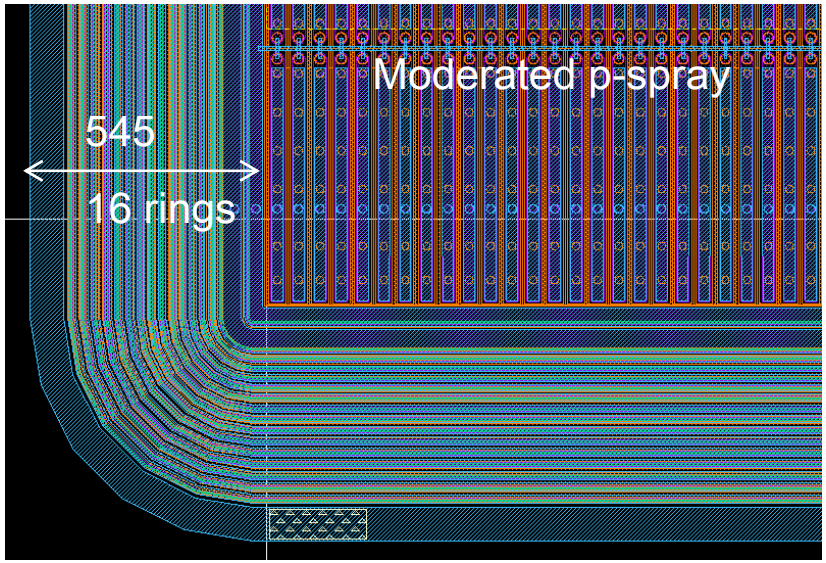
FEI4-2 : standard GR, moderated p-spray

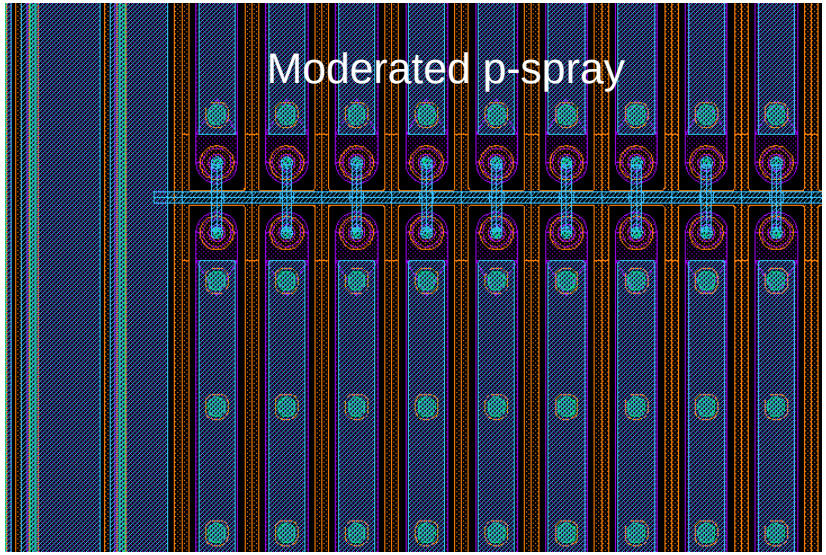
S1 and S6: 80 μm pitch strips, HLL design

S2 to S5: 80 μm pitch strips, RD50design

ATLAS pixels: Isolation schemes (I)

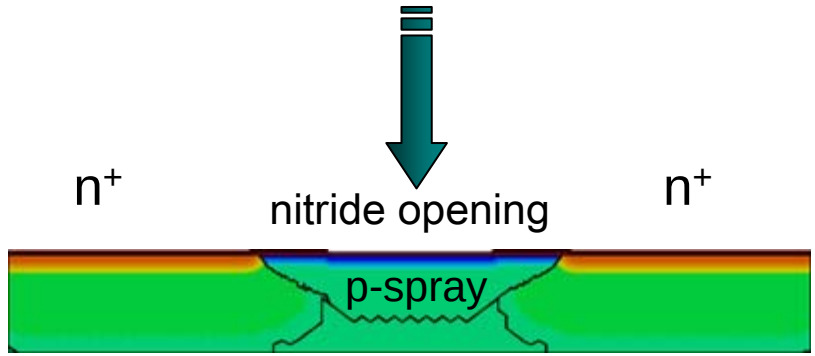
- Standard FE-I3 SCM dimensions , 1100 μm from cutting edge to guard rings



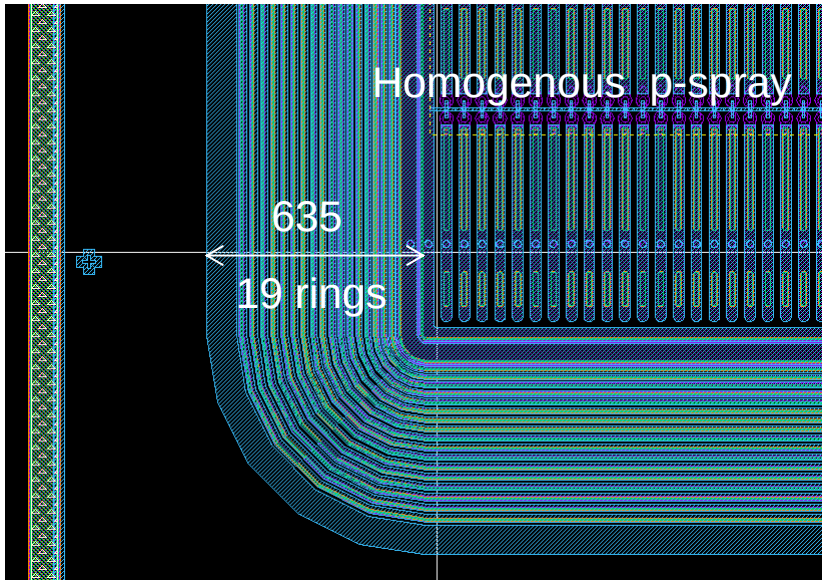


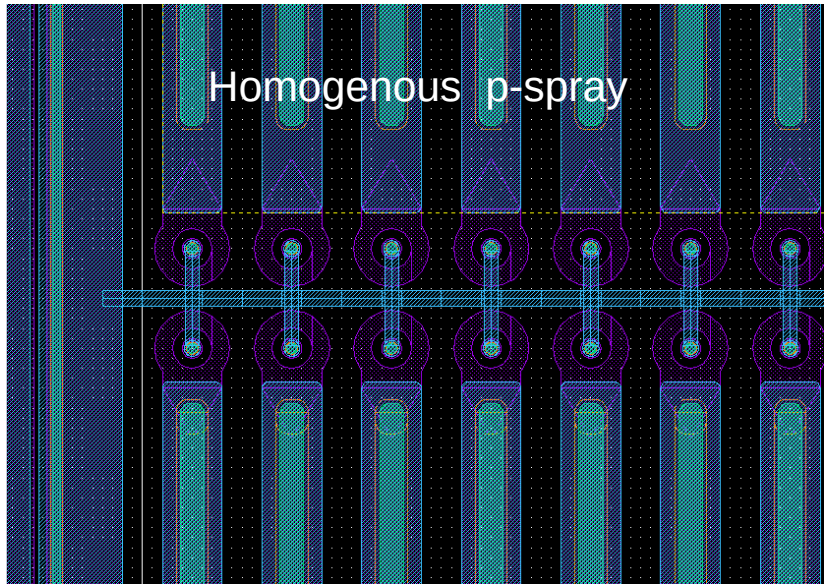
- Moderated p-spray: standard isolation scheme between pixels adopted by the present n-in-n ATLAS and CMS sensors.

- An opening in the nitride layer determines an increase of the boron implanted dose in the central region between the strips.



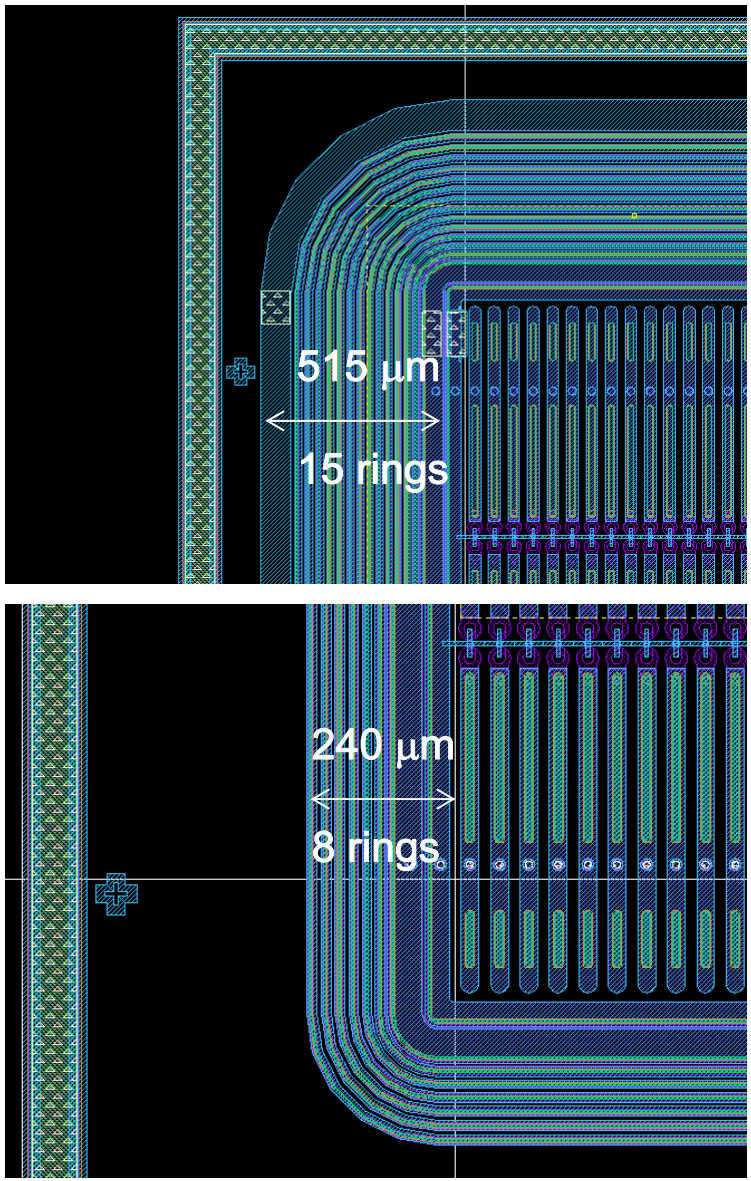
ATLAS pixels: Isolation schemes (II)





➢ Implementation in the pixel design of the isolation scheme with homogenous p-spray : good performances observed in pre- and after-irradiation characterization of the MPP-HLL thin pixel production where this isolation method has been implemented.

Slim Edges: reduced guard ring structures

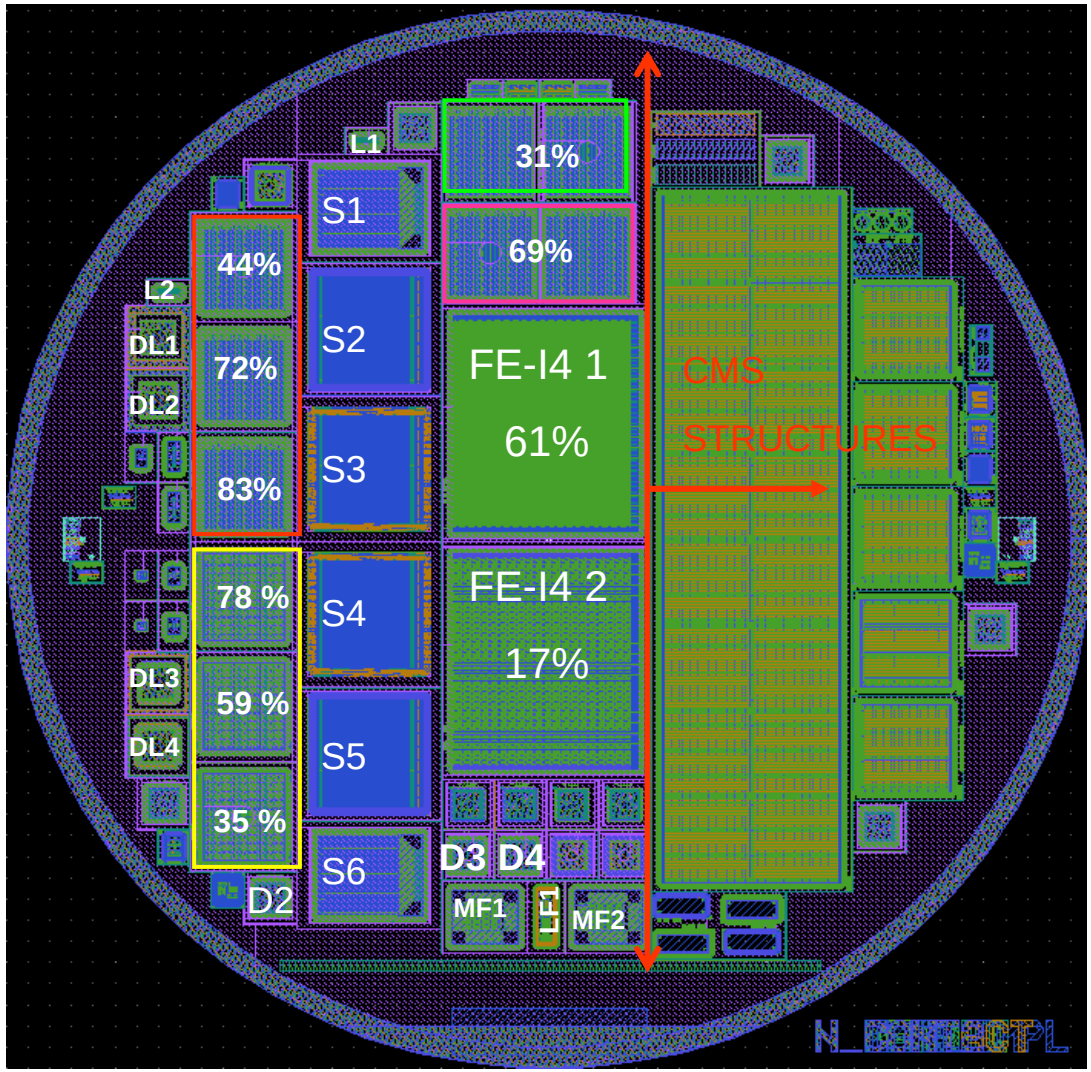


- For the modules of the ATLAS Insertable b-Layer no shingling is allowed: the sensors are required to have inactive edges < 450 μm.
- Design of slimmed guard-rings structures aided by simulation activities carried out by the ATLAS LAL-LAPNHE groups.
- Both in the n-in-n and n-in-p designs the slimmed edge versions have been implemented mostly in the FE-I3 sensors → more variations are possible due to the reduced size with respect to the FE-I4 sensors

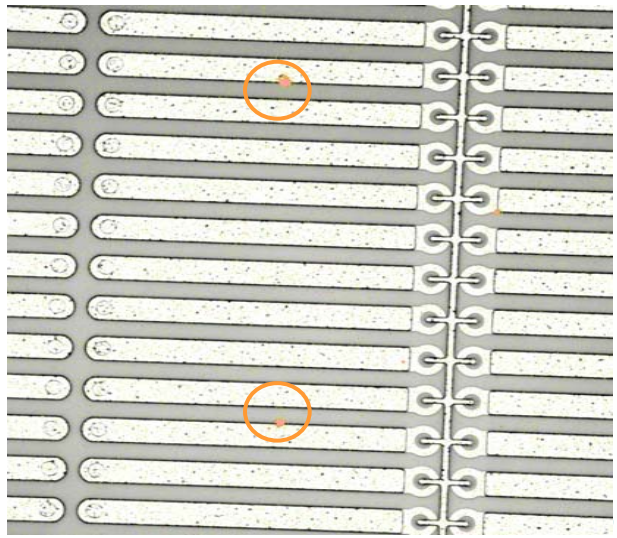
CiS n-in-p production yield

Efficiency definition for FE-I3: I_{leak} <700 nA @ 150 V (V_{depl}=60V)

FE-I4: I_{leak} <2 μA @ 150 V



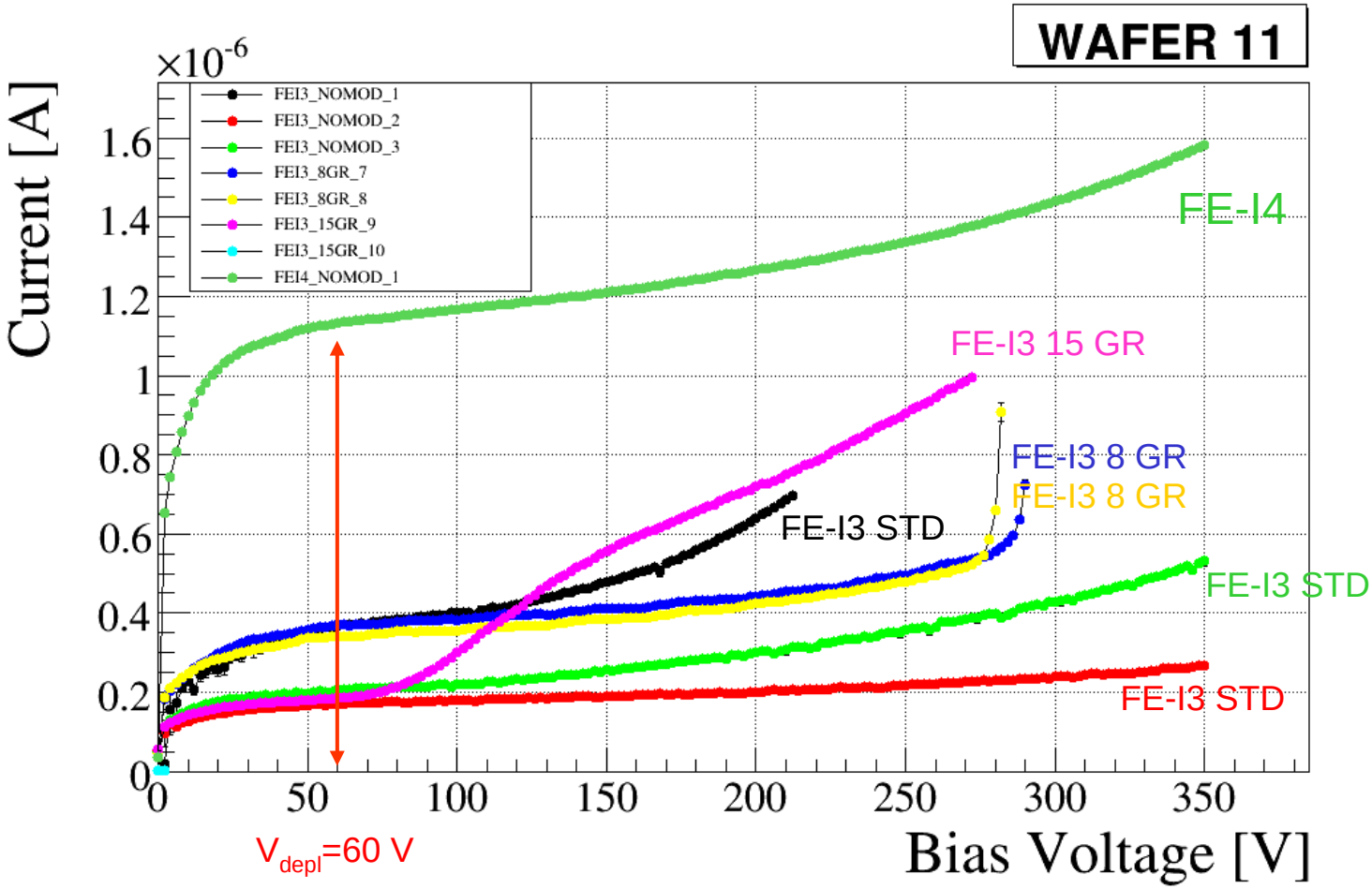
- The yield has a strong radial dependence, pointing to some process non-homogeneity.
- Pictures from the photon emission microscope show many hot spots but not correlated to any critical structure, as GR or punch-through.



Slim edges investigation

- Slim edges implemented in FE-I3 sensors:

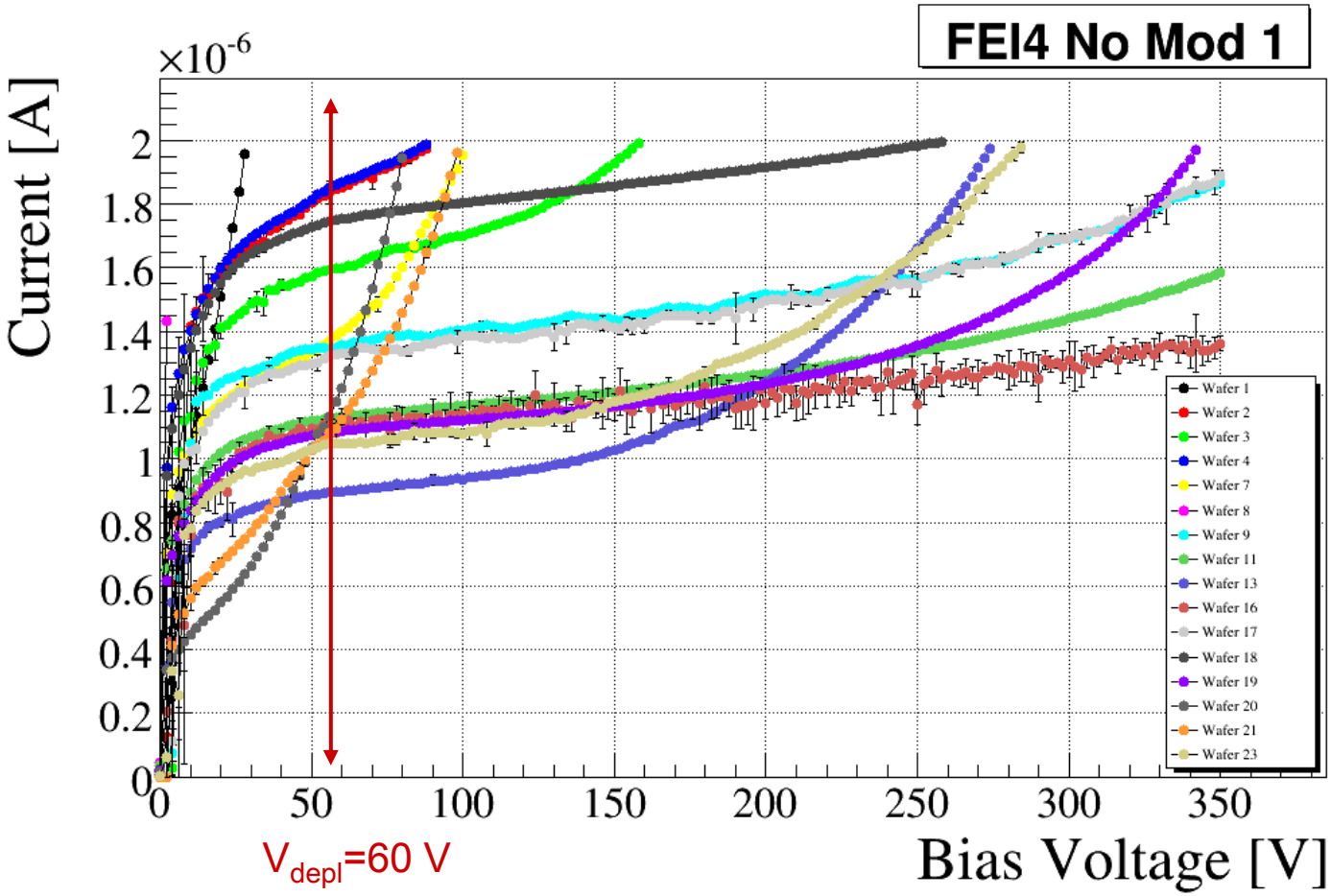
- performance of sensors with 15 GR is comparable to standard (19) GR
- difficult to disentangle for the 8GR version the effect of the external location on the wafer.



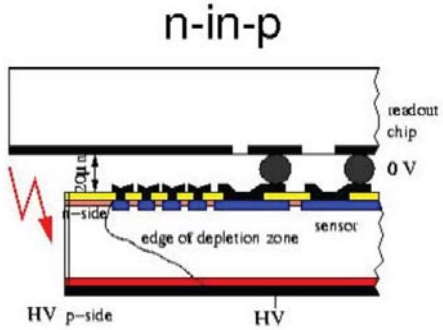
FE-I4 sensors

- FE-I4 sensors have been implemented with standard GR, homogeneous and moderated p-spray

- Among the 10 wafers with UBM, 11 good n-in-p FE-I4 available for flip-chipping.

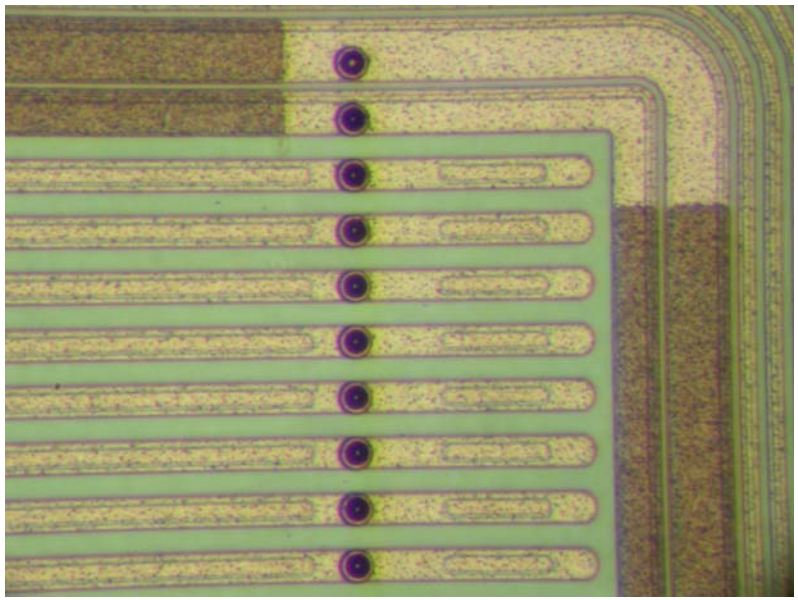


Post-processing at IZM-Berlin

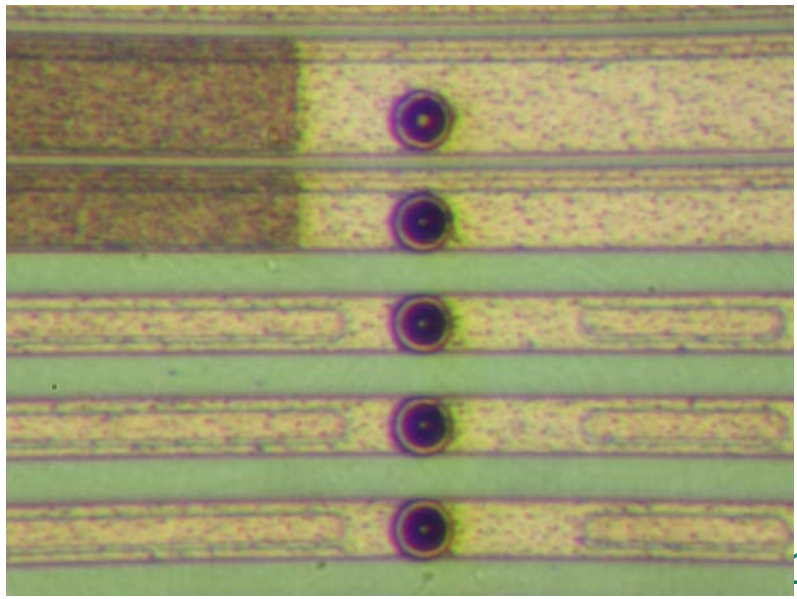


- 10 best wafers sent to IZM-Berlin for :
  - deposition of a 3 μm thick layer of BCB as additional passivation
  - UBM processing
- 2 wafers left undiced for plasma-etching trials by IFAE; the remaining 8 have been partially diced by IZM with only the large pixel structures singularized (FE-I3 and FE-I4).
- The first 7 FE-I3 chip-sensor assemblies have already been flip-chipped. 14 more assemblies will be produced after the test of the first devices.

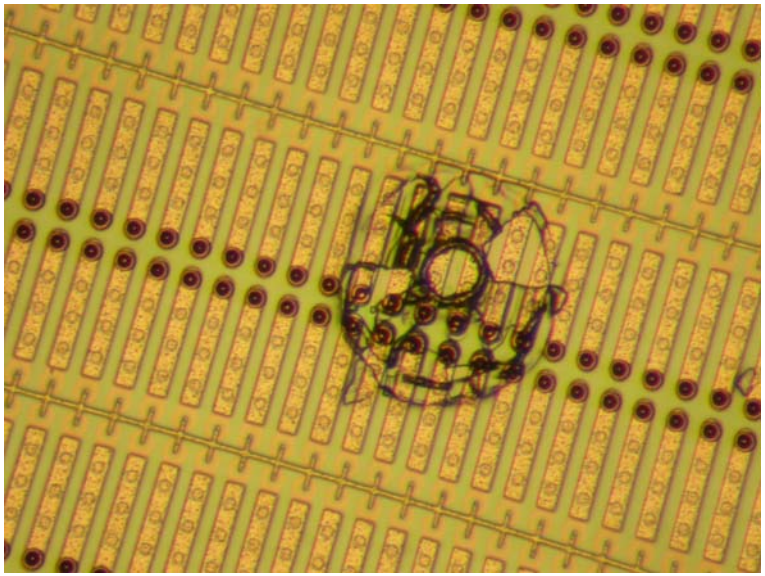
UBM on FE-I3 sensor

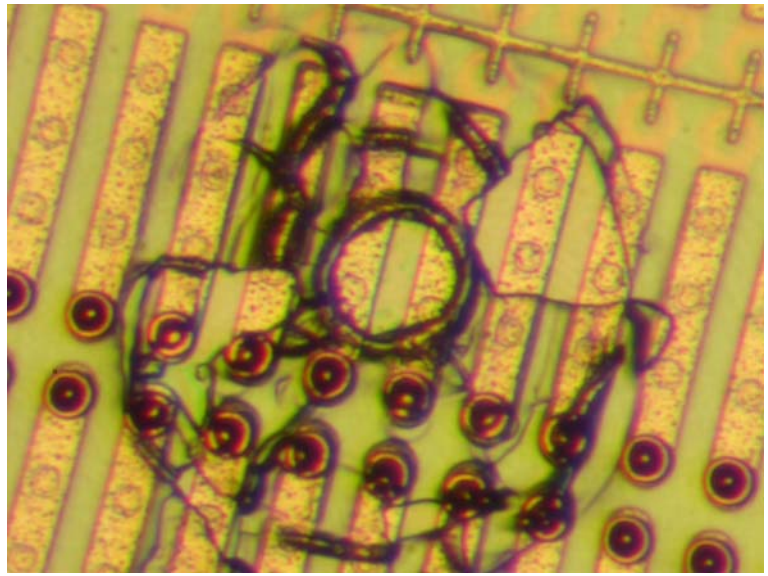


Close-up

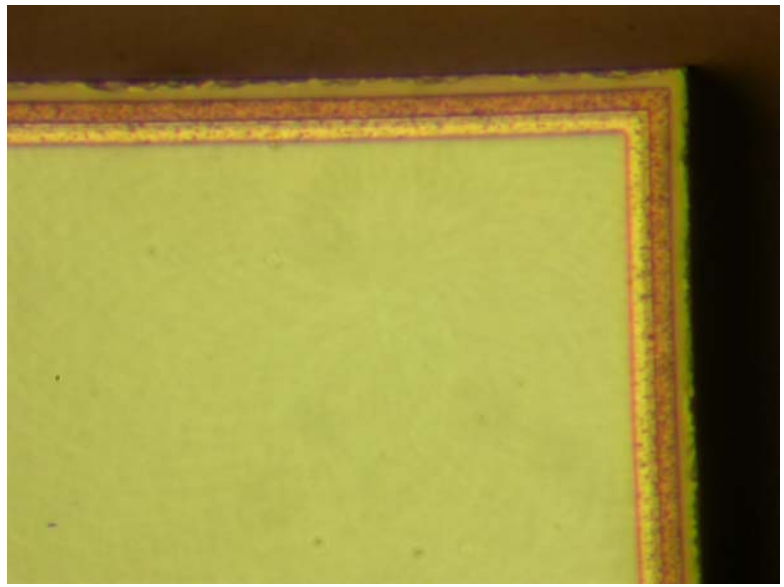


Post-processing at IZM – BCB quality

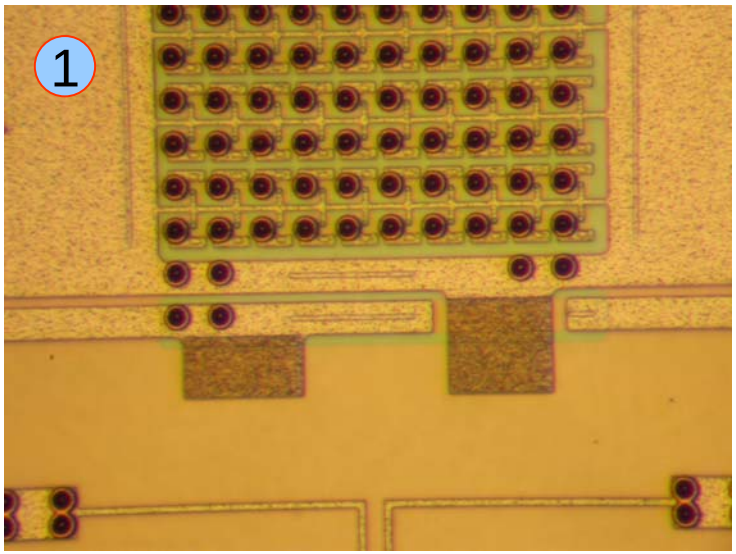


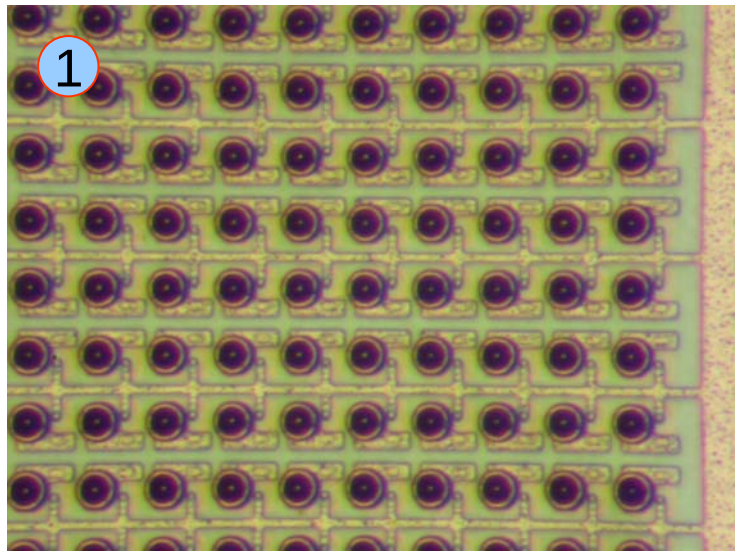


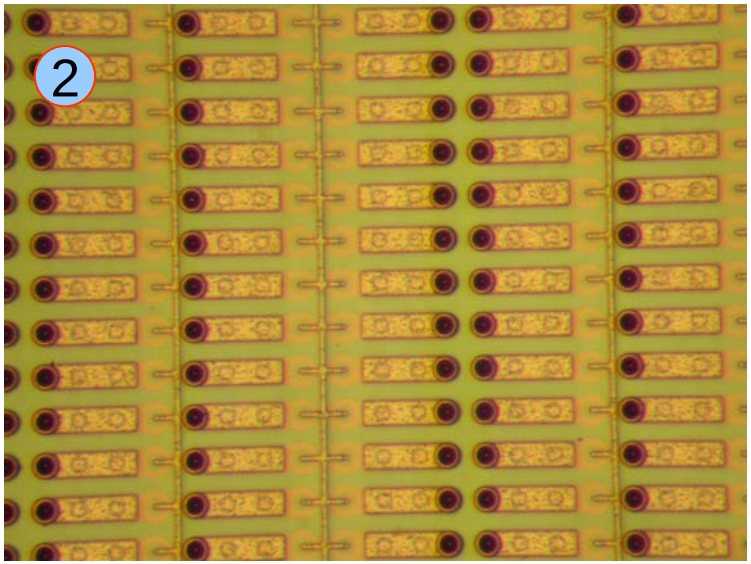
- The BCB layer has an overall good quality by visual inspection. Cracks have been seen only in two FE-I4 structures of the same wafers , over a total of 10 wafers.
- No problems observed in the FE-I3 structures.
- The BCB layer did not suffer from the dicing, no problems seen along the pixel edges.



UBM processing at IZM – small pixel pitches



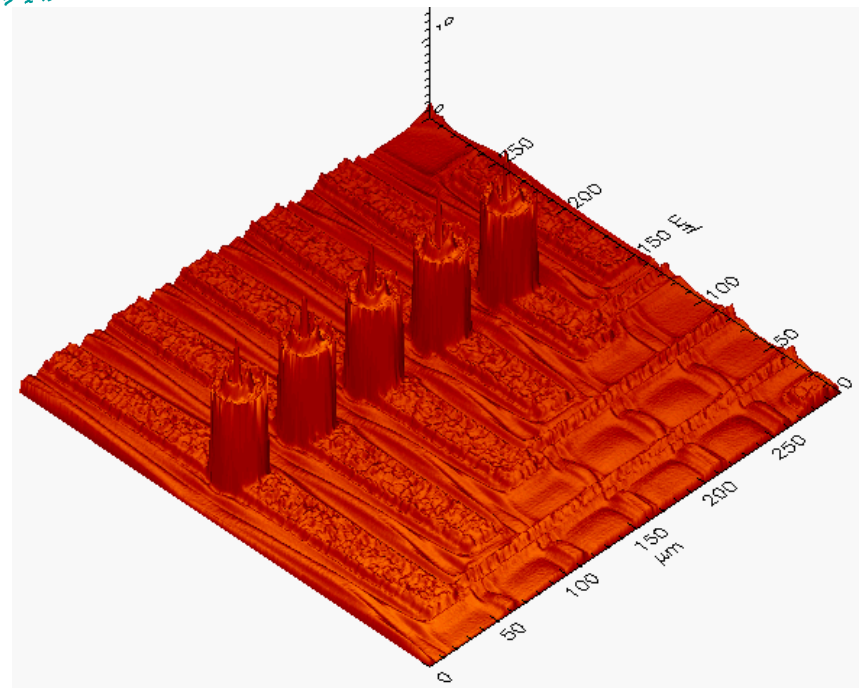




- Good UBM quality also with very fine pitches of small pixel matrices designed for 3D chips (Orsay and Marseille groups):

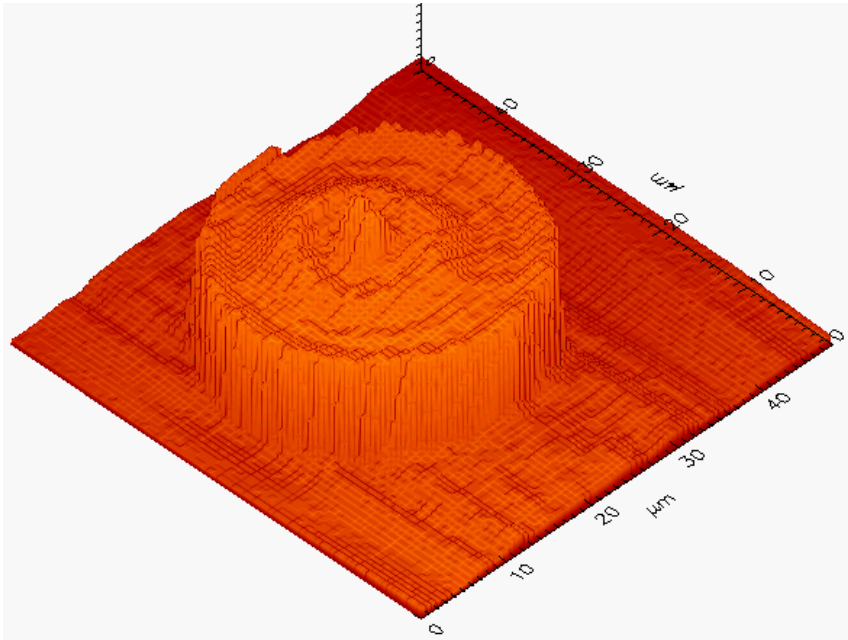
1) 50x50 μm^2
2) 50x166 μm^2

UBM at IZM



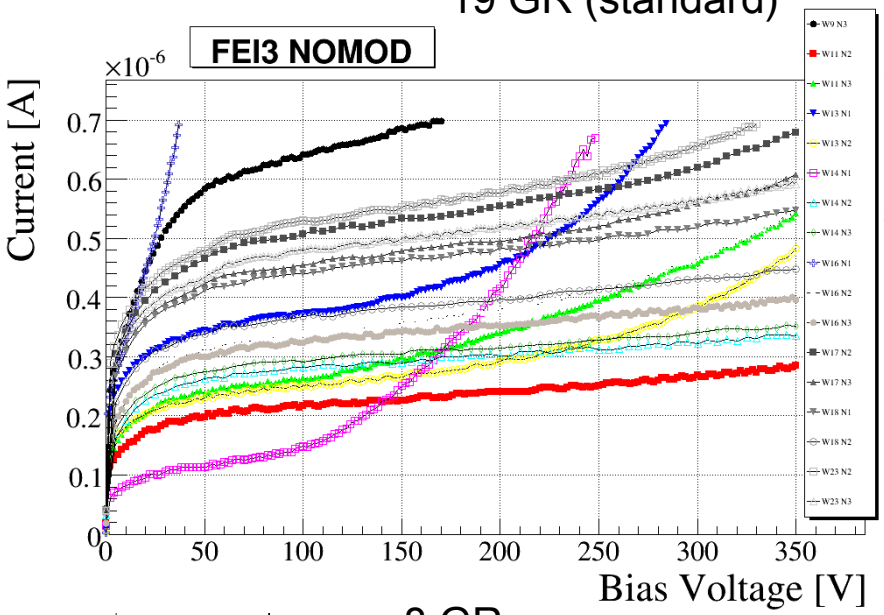
- UBM pads have been analyzed with a RTF profiler at HLL.
- In these pictures only the metal layers (UBM + Al of the pixels) and the bare silicon are visible.

- The BCB and the original SiO_2 passivation are transparent in this scan, but have been measured to be respectively 3 µm and 1 µm thick with the same RTF profiler in another configuration. UBM pads height is 6-7 µm, over the BCB layer.

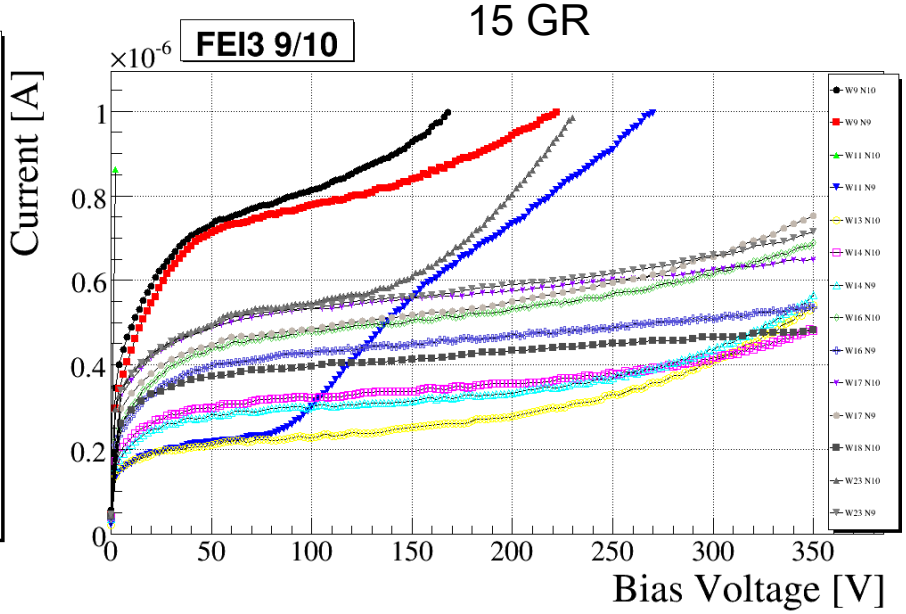


Pixel sensors performance after UBM and dicing

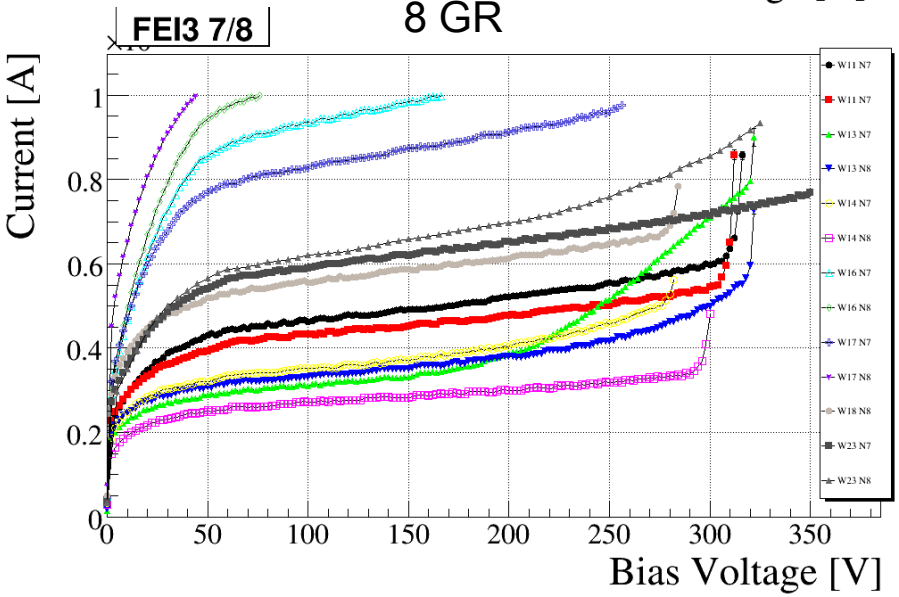
19 GR (standard)



15 GR



8 GR

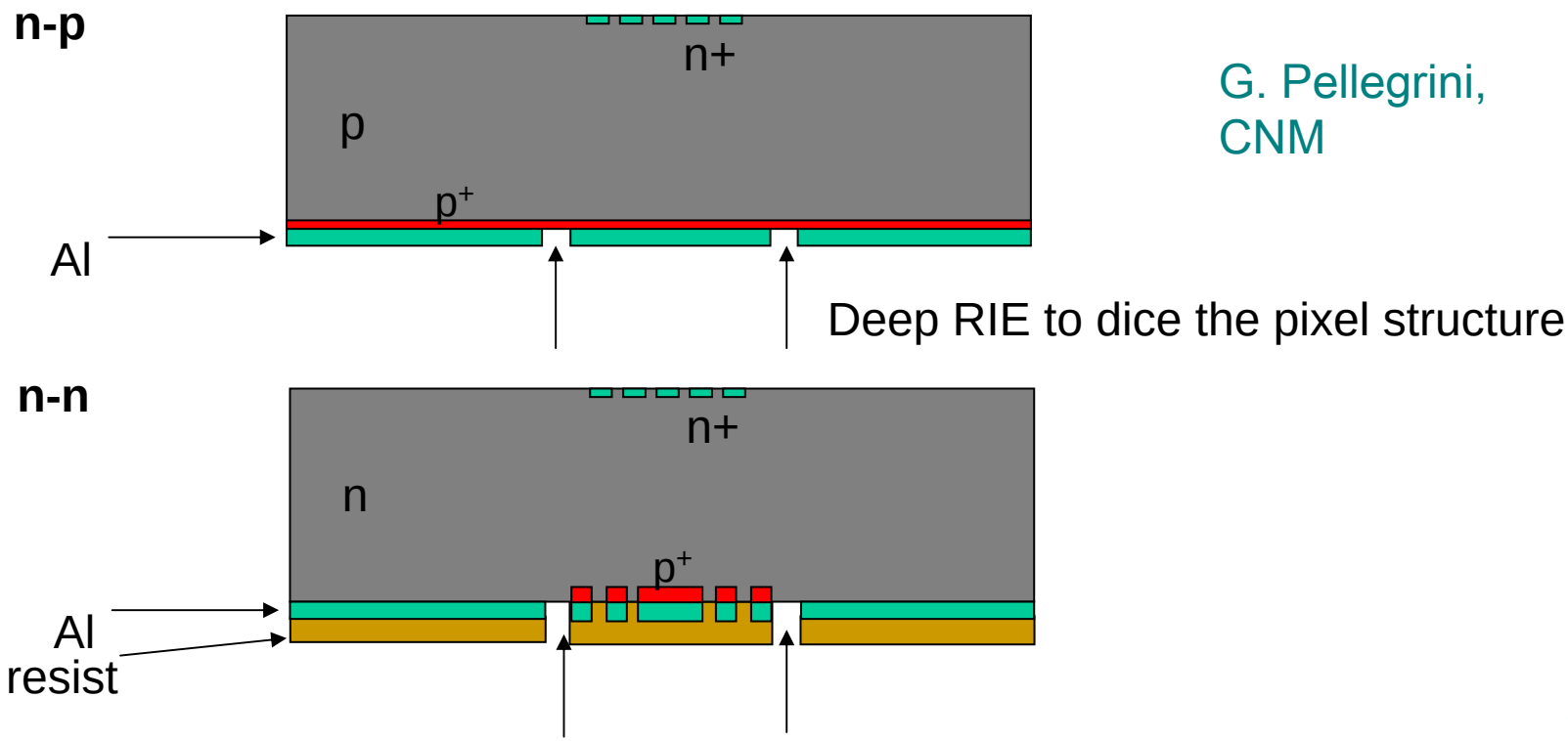


- Sensors have almost identical IVs before and after the UBM processing. Structures with a reduced GR maintained good performances after dicing.
- Many FE-I3 diced structures available for flip-chipping (+2 plasma diced wafers at IFAE):
  - 13 with standard GR
  - 9 with 15 GR
  - 9 with 8 GR

Slim Edges: dicing with DRIE

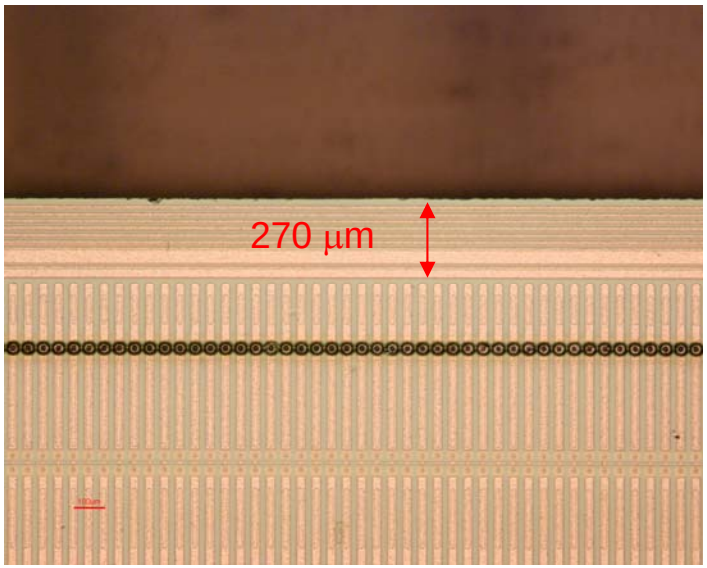
Deep RIE : Alternative dicing method to sawing with less surface damage, investigated by the IFAE-CNM group

- 2 n-in-p wafers with UBM have been dedicated to etching trials at CNM.
- Cutting lines implemented at a short distance from the end of the GR structure (30-40 μm).



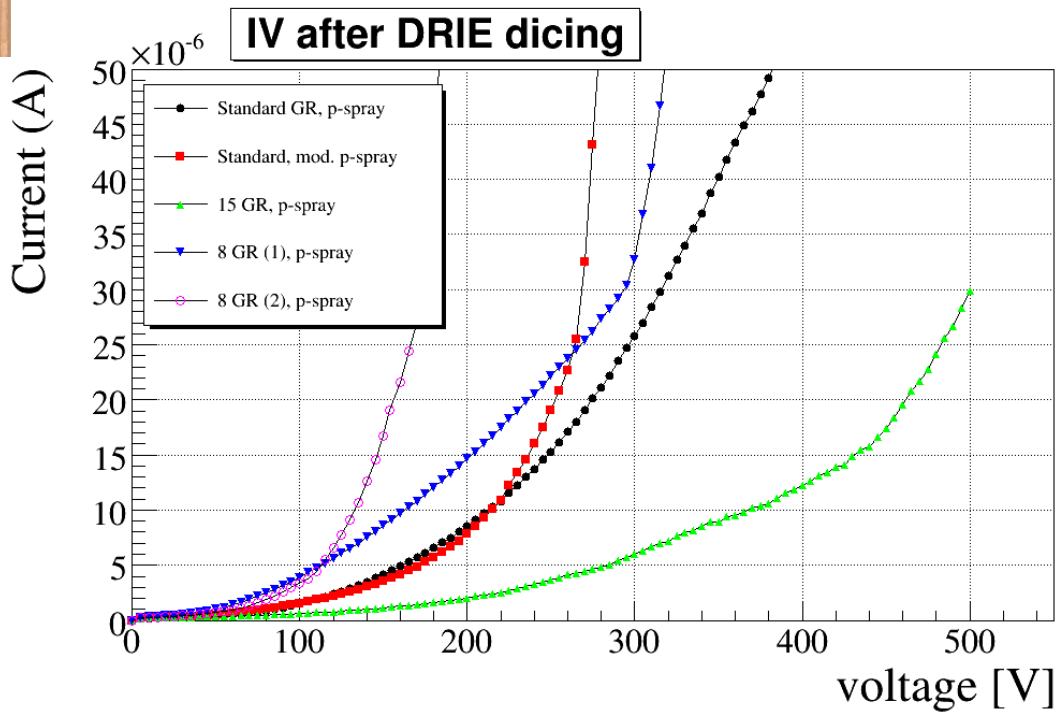
G. Pellegrini, CNM

Results after dicing with DRIE



One wafer with UBM has been diced with DRIE at CNM

- inactive edges down to 270 μm have been obtained.
- some cracks corresponding to the position of the silicon bridges left uncut in the middle of the dicing lines, to hold temporarily the structures to the remaining part of the wafer.



- One of the 8GR structures plus one standard pixel sensors from this DRIE diced wafer have been flip-chipped at IFAE and will be tested in the coming days (S. Grinstein).

Irradiation and test-beam plans

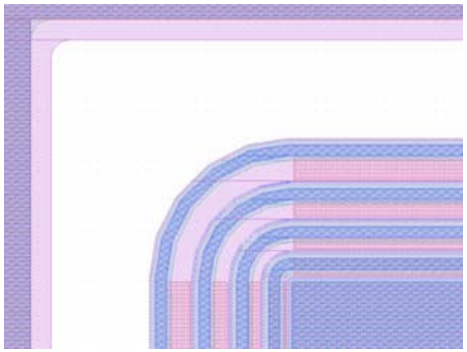
- Some bare n-in-p FE-I3 sensors already sent to CERN to be irradiated in the first irradiation at the end of April.

- FE-I3 assemblies attached to the read-out card should be available this week. Plan to characterize the assemblies with the ATLAS USB-Pix system and possibly study their performance before irradiation in a CERN test beam in July.

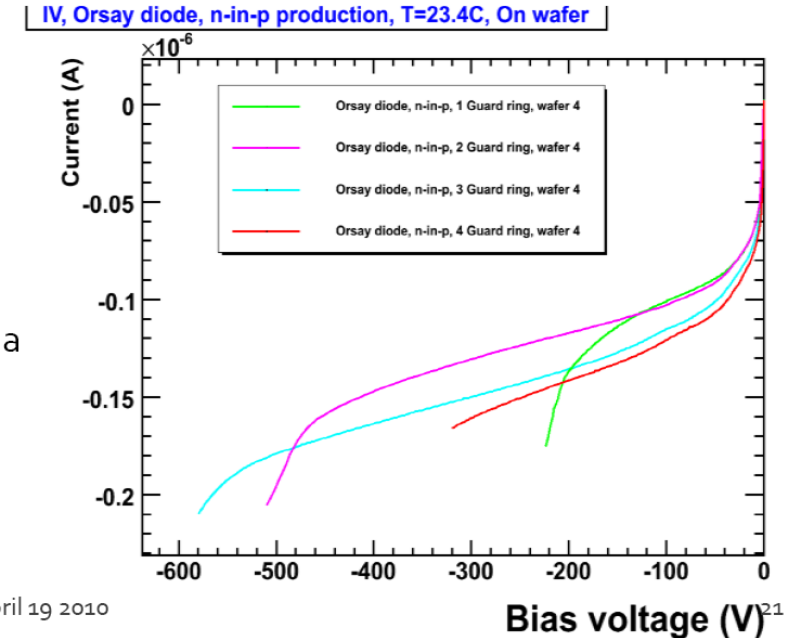
- Irradiation of sensor-chip assemblies in the August CERN irradiation run.

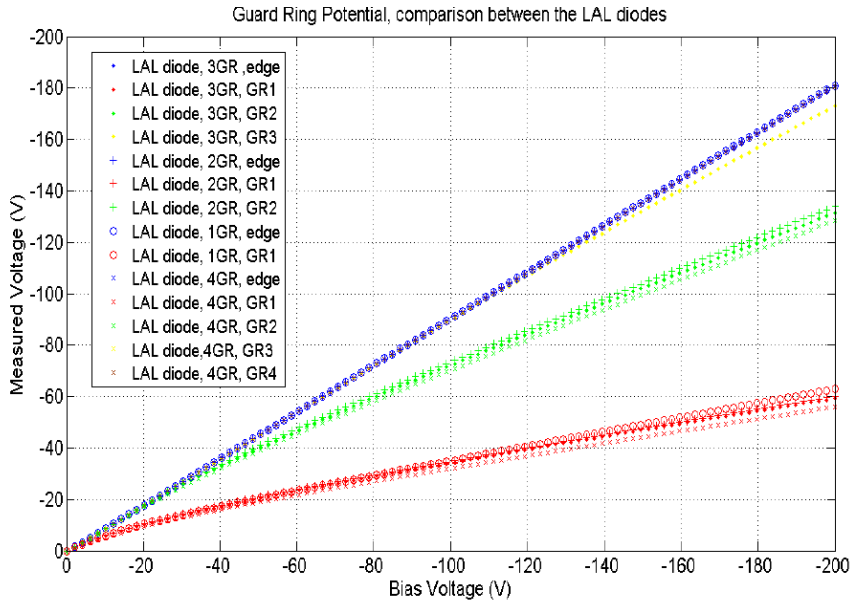
Tuning of the TCAD simulation at LAL

- The LAL group has developed a Silvaco TCAD simulation for planar structures (M. Benoit), used to simulate the n-in-n and n-in-p pixel structure implemented in the CiS production.
- Simple diodes, with an increasing number of GR (1-4), have been used to tune the simulation and extract the process parameters.

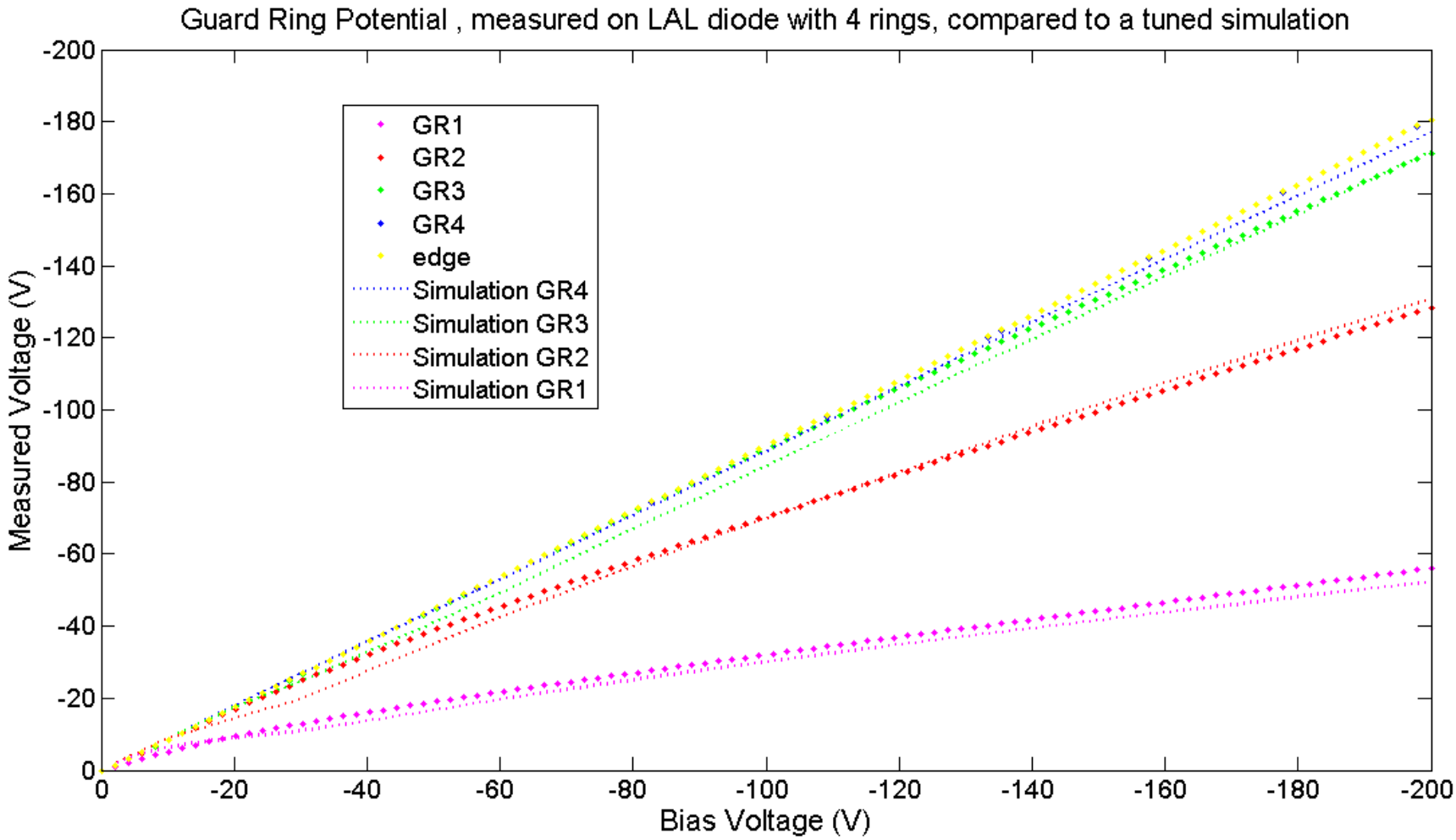


- The matching simulation corresponds to a p-spray concentration of O(10^{16} cm^{-3}) and a oxide charge of $0.5x10^{11}$ cm^{-2}.
- Measurements of the GR potential suggest that the potential of the inner rings is only slightly dependent on the presence of the more external ones.





Tuning of the TCAD simulation at LAL



Conclusions and Outlook

- CiS n-in-p pixel production characterized. Some yield issues at the edges of the wafer but many structures are available for interconnection to the FE-I3 and FE-I4 chips.

- BCB deposition and UBM processing at IZM-Berlin have been performed without visible problems (at least before flip-chipping).

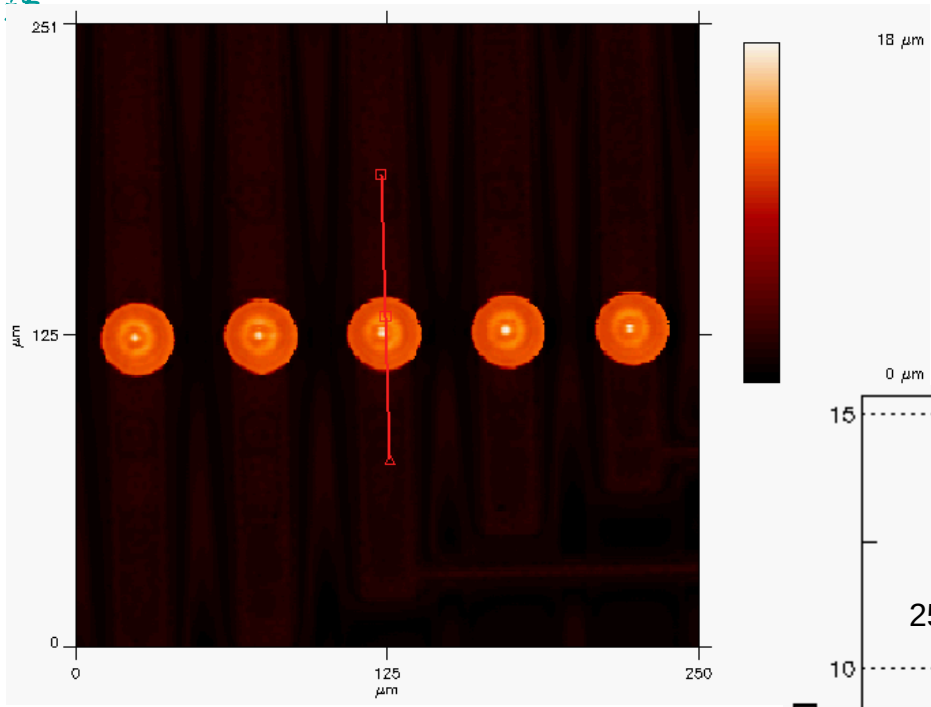
- Dicing performed with the standard diamond saw technique at IZM and at CNM flip plasma etching to achieve slimmer edges.

- Flip-chipping performed for the first 7 structures at IZM-Berlin. Two pixel sensors have been flip-chipped at IFAE.

- Plans to characterize the chip-sensor assemblies and irradiate them in the August CERN irradiation.

- Tuning of the TCAD-simulation developed at LAL-Orsay performed with the aid of measurements on diode of this production.

UBM at IZM (II)



- Height scan performed along the pixel direction