ALIBAVA system upgrade

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Instituto de Microelectrónica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain.
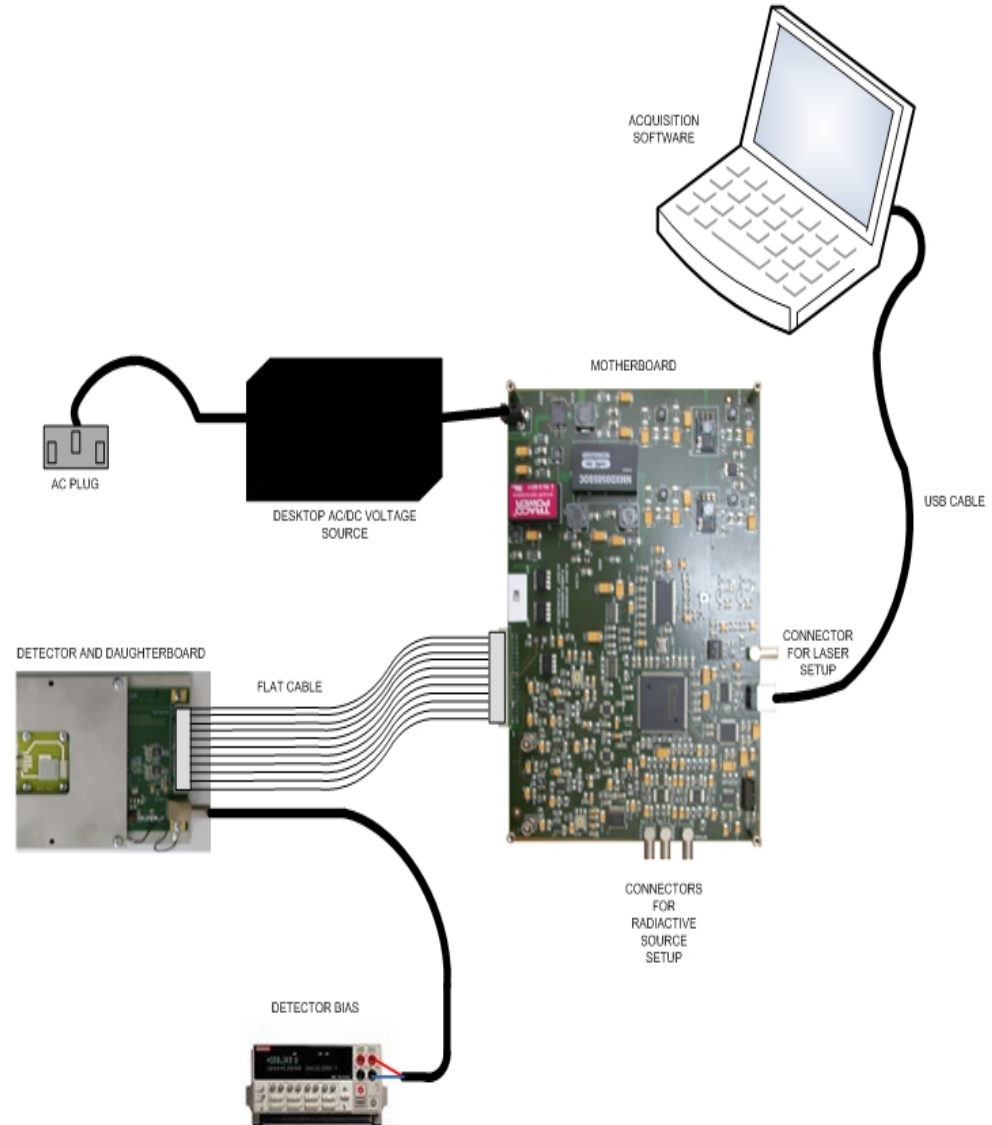*Instituto de Física Corpuscular (IFIC), Universidad de Valencia-CSIC,Valencia, Spain.*

Outline

- System architecture.
- Chip masking.
- Header sampling.
- Calibration delay scan.
- Software reset and hardware version.
- Summary.

System architecture

- Software part (PC) and hardware part connected by USB.
- **Hardware part**: a dual board based system connected by flat cable.
  - **Mother board** intended:
    - To process the analogue data that comes from the readout chips.
    - To process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used.
    - To control the hardware part.
    - To communicate with a PC via USB.
  - **Daughter board** :
    - It is a small board.
    - It contains two Beetle readout chips.
    - It has fan-ins and detector support to interface the sensors.
- **Software part**:
  - It controls the whole system (configuration, calibration and acquisition).
  - It generates an output file for further data processing.

ACQUISITION SOFTWARE

MOTHERBOARD

AC PLUG

DESKTOP AC/DC VOLTAGE SOURCE

USB CABLE

CONNECTOR FOR LASER SETUP

DETECTOR AND DAUGHTERBOARD

FLAT CABLE

CONNECTORS FOR RADIACTIVE SOURCE SETUP

DETECTOR BIAS

Chip masking

- The system had to work using both Beetle chips.

  - Continuously.

  - Even if you had just one detector connected.

- Each Beetle ASIC can be addressed independently.

  - For configuration, calibration and acquisition.

  - Time saved when configuring and reading data.

- FPGA logic modified.

  - Slow control block: chips addresable by CHIP (1:0) from Microblaze processor.

  - Arbitrer: added SC_CHIP (1:0).

- Microblaze processor firmware modified.

  - Chip masking configured at Beetle Configuration.

  - Beetle_mask [0...0 B1 B0].

 - Chip masking applied for reading data in calibration and acquisition.
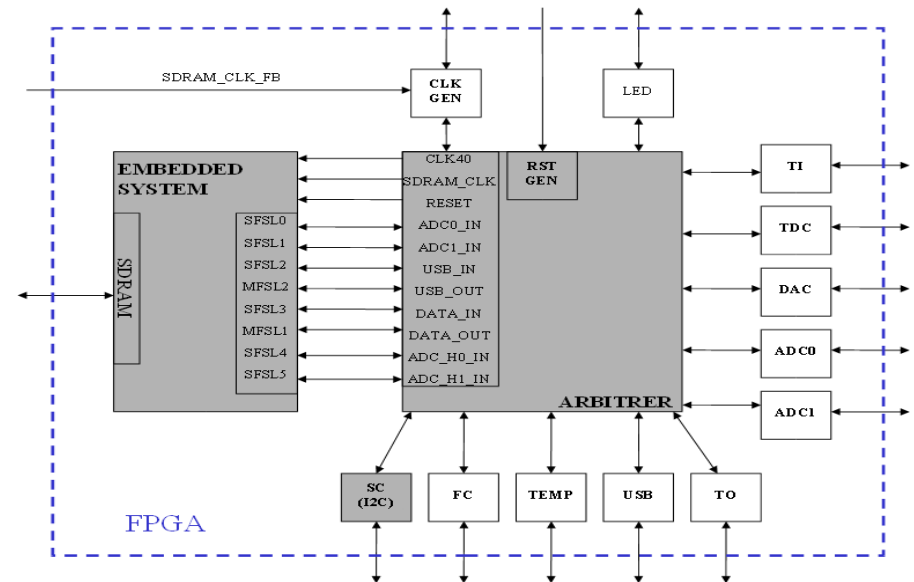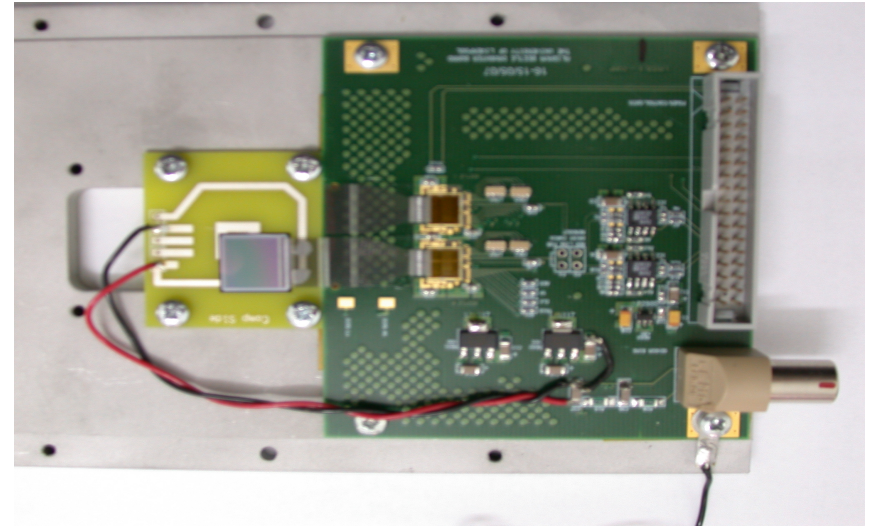
Header sampling

- The output data of each Beetle chip consists of a header and the analogue channels multiplexed.
  - Header of 16 'bits'.
  - 128 analogue channels.
  - Header bits and analogue channels are 25 ns wide.
- The system digitalized just the analogue channels while rejecting the header bits.
- The header bits offer 'real time' information about the Beetle chip status.
  - Parity of some configuration registers.
 - Pipeline column number of the data read.
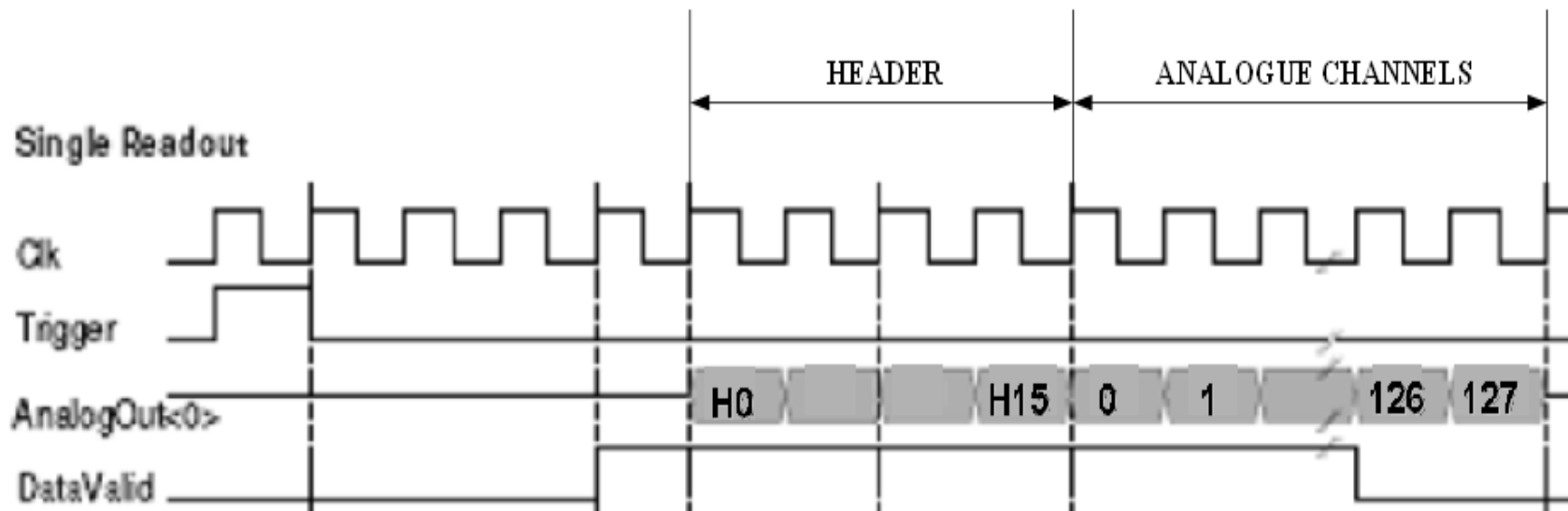
Header sampling

- The header is now digitalized together with the analogue channels to have all the 'real time' information.

- FPGA logic modified.

    - Two new FIFOS added to the Microblaze to store the header data.

    - ADC0 and ADC1 blocks generate SCLK for the header and control the header FIFOs.

    - Arbitrer connects the header FIFOs with ADC blocks.

- Microblaze processor firmware modified.

    - Header data read together with channels data.

    - Beetle data structures modified to handle the header data when moving data.
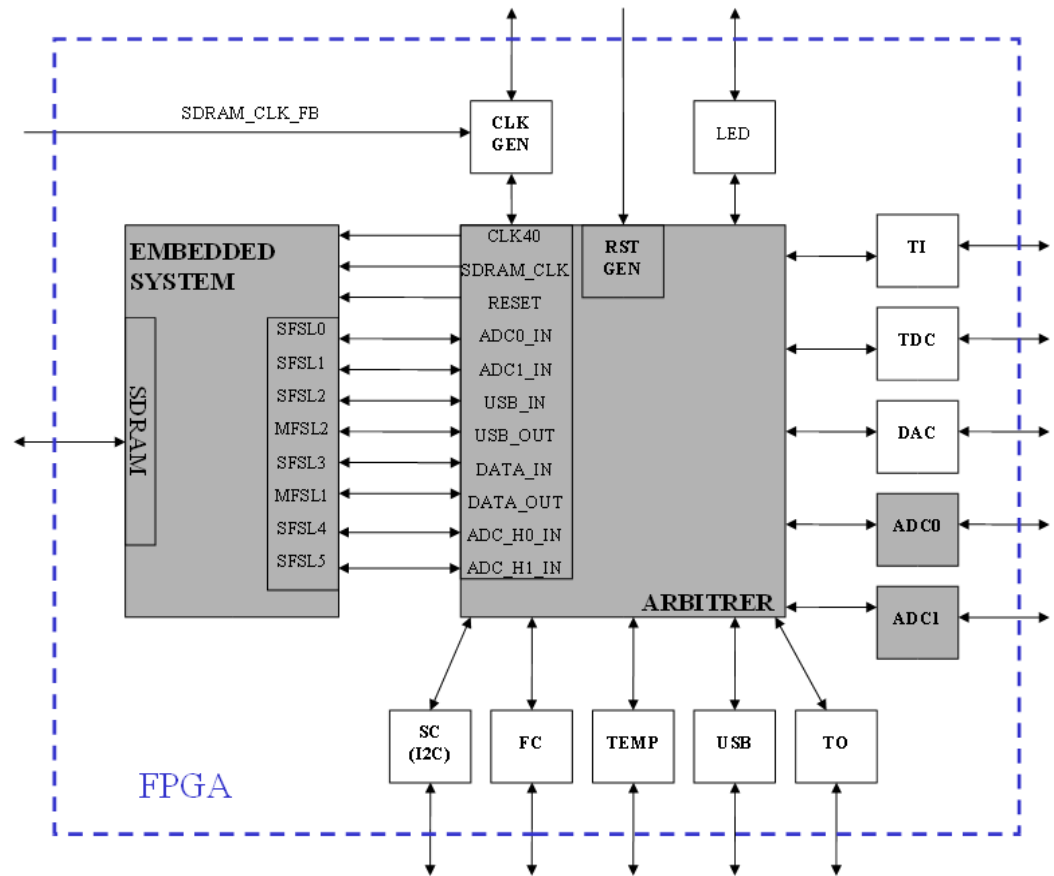
Calibration delay scan

- The system is calibrated by injecting pulses on the input channels of the Beetle ASICs.

  - Amplitude injected in electrons configured in the Beetle registers.

  - Sign of the injected pulse is changed every time a new pulse is injected. It also alternates with the channel number.

  - The pulse is injected when a TestPulse LVDS signal is activated.

  - The data is read when a Trigger LVDS signal is activated.

- The delay between TestPulse and Trigger signals was fixed.

- There is no possibility of reconstructing the analogue pulse in calibration stage.

- What if the calibration values do not correspond to the pulse peak?.
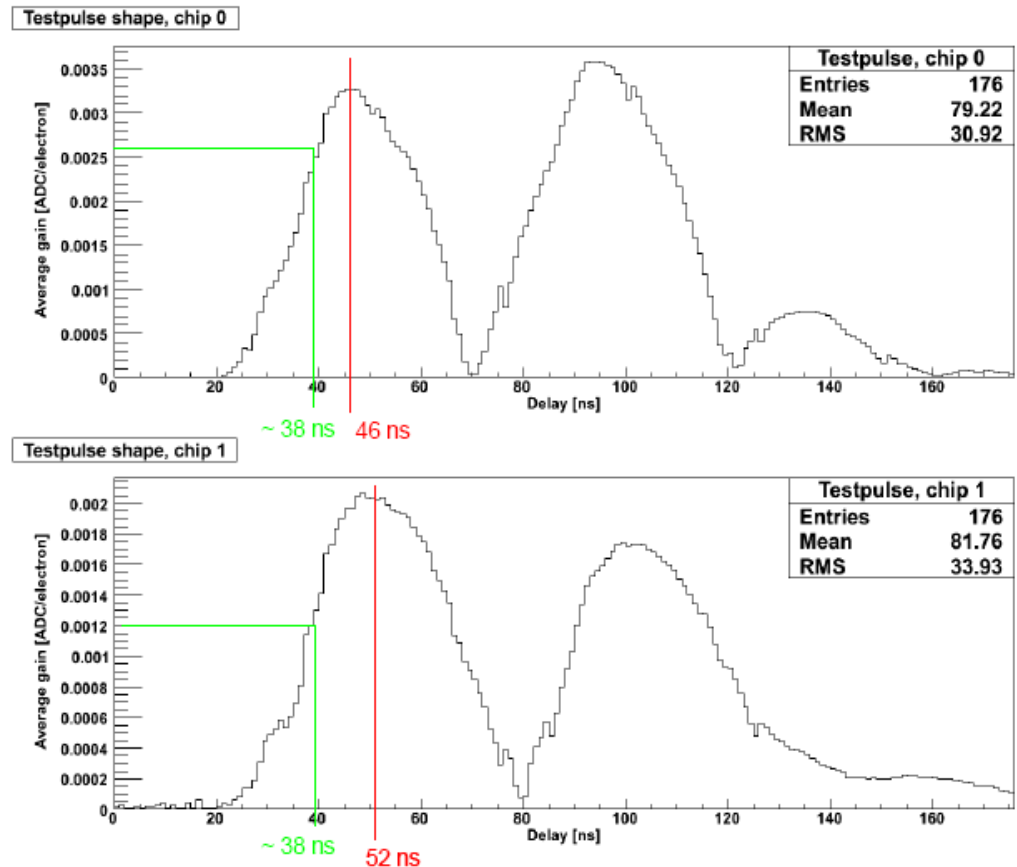
From Michel Walz (University of Freiburg)

Calibration delay scan

- The delay between TestPulse and Trigger is now configurable by the user.

  - Resolution of 1 ns.

  - 0-255 ns range.

  - TP is generated only once.

- FPGA logic modified.

  - Fast control block includes a new block for delaying TP w.r.t. Trigger.

  - Combining the carry-chain resources for fine delay (1 ns) and a 200 MHz clock for coarse delay.

  - For nominal zero delay there is a latency + 5 (133 clock cycles) between TP and Trigger: accounting for intrinsic delay.

  - Arbitrer: added DELAY_CAL, DELAY_COARSE(5:0) and DELAY_FINE(2:0).

- Microblaze processor firmware modified.

  - Delay is programmed as well as the charge to inject for each calibration TP.

Calibration scan Beetle 0 channel 2 (latency + 5 and TP 1)
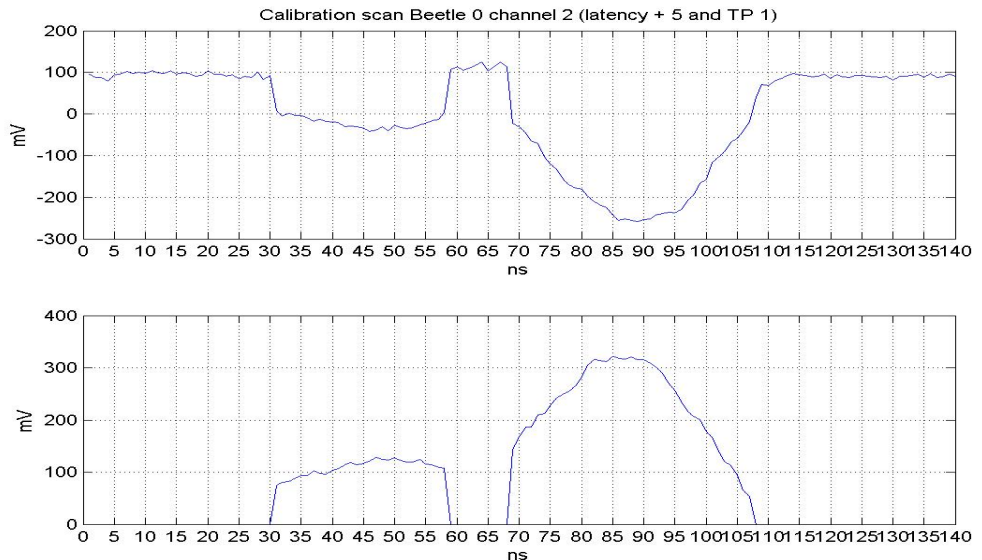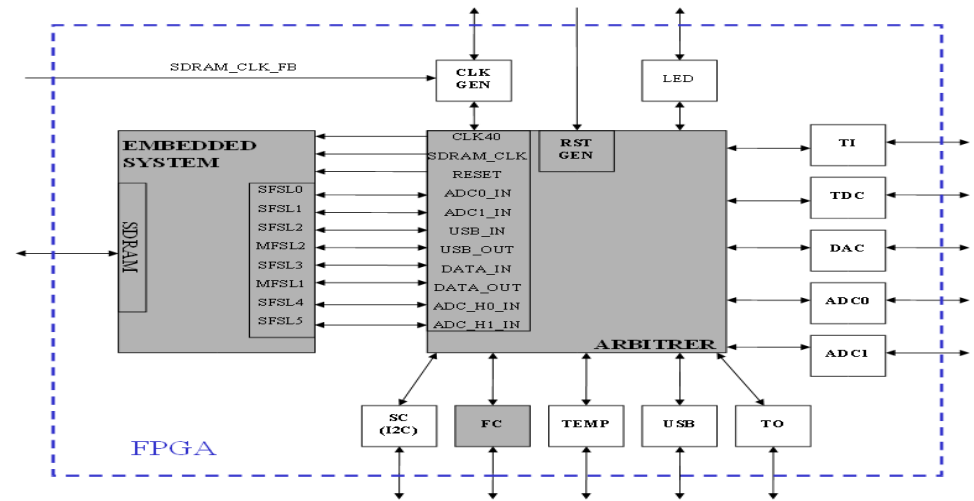
Software reset and hardware version

- We realized that the system needed an improved reset.

    - The reset by software did not work when the system was stuck: it was a firmware reset.

    - The reset button should be pushed before the software was launched.

- A real software reset have been implemented.

    - The USB block spies the data sent by the software and generates a reset query if a special code is detected.

    - The RST block generates a reset signal for all the hardware: he reset is done by hardware.

- The RST block have been improved so that the system is really reset automatically when the software is launched.

- The hardware version is now sent to the software in order to load the correct version of software.
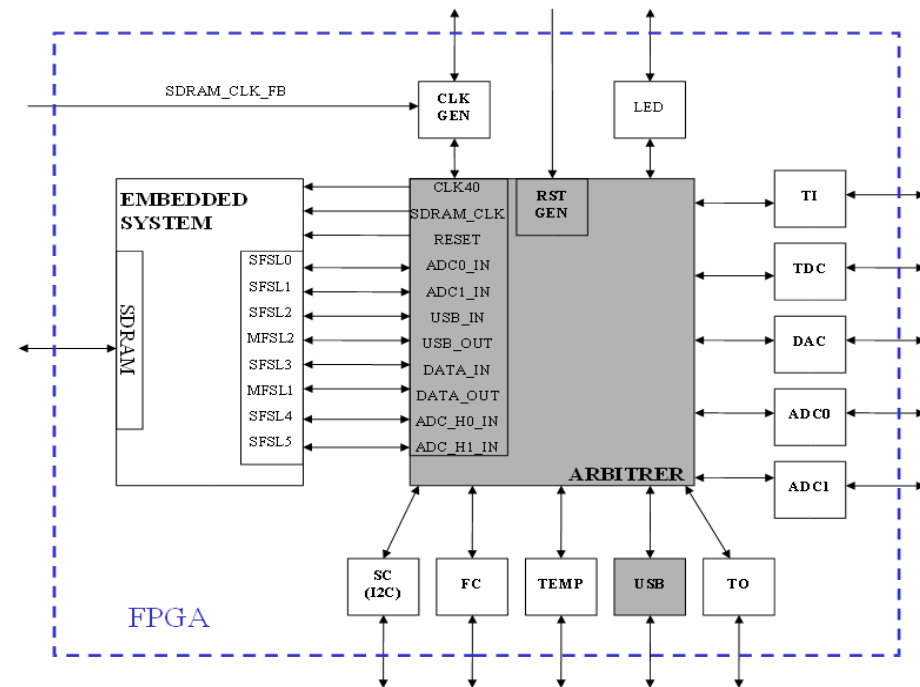
Summary

- A system upgrade have been carried out to include some new features.
    - Chip masking.
    - Header sampling.
    - Calibration delay scan.
    - Software reset/hardware reset improvement.
    - Hardware version identification.
- The upgrade have been accomplished by modifying the FPGA hardware/firmware and the software.
- Status:
    - The FPGA hardware/firmware changes are finished and already tested.
    - The software changes are finished but must be tested with the hardware.
    - All ALIBAVA users will be informed when the upgrade is ready to use.
- FPGA re-programming.
    - In the next RD50, or
    - by yourself (if you have a FPGA Xilinx programmer), or
    - by shipping the ALIBAVA MB to me.
- Software distribution: new software version will be released through the twiki.

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