Integration and performance of the HMPID in the ALICE O2 system

ALICE-HMPID plenary meeting CERN - 11/12/2019

CEADEN (CU)

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Overview

- HMPID commissioning - Equipment distribution/connection.

- HMPID performance at 100KHz of trigger rate.

- HMPID software integration to O2 framework.

- Conclusions.

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HMPID commissioning - Equipment distribution/connection

EQUIPMENT-#	CROC-#	PCI Addr	Channel	SIU (SN)	JTAG (IP)	LOCAL Host Name
0-LEFT	1	3b:00.0	0	03027	10.160.128.67	HMPID-P2-JTAG-0L.cern.ch
0-RIGHT	1	3b:00.0	1	03029	10.160.128.64	HMPID-P2-JTAG-0R.cern.ch
1-LEFT	1	3b:00.0	2	03038	10.160.128.63	HMPID-P2-JTAG-1L.cern.ch
1-RIGHT	1	3b:00.0	3	03039	10.160.128.62	HMPID-P2-JTAG-1R.cern.ch
2-LEFT	0	af:00.0	0	03028	10.160.128.57	HMPID-P2-JTAG-2L.cern.ch
2-RIGHT	0	af:00.0	1	03034	10.160.128.65	HMPID-P2-JTAG-2R.cern.ch
3-LEFT	0	af:00.0	2	03025	10.160.128.66	HMPID-P2-JTAG-3L.cern.ch
3-RIGHT	0	af:00.0	3	03033	10.160.128.61	HMPID-P2-JTAG-3R.cern.ch
4-LEFT	2	d8:00.0	0	03035	10.160.128.55	HMPID-P2-JTAG-4L.cern.ch
4-RIGHT	2	d8:00.0	1	03030	10.160.128.56	HMPID-P2-JTAG-4R.cern.ch
5-LEFT	2	d8:00.0	2	03036	10.160.128.68	HMPID-P2-JTAG-5L.cern.ch
5-RIGHT	2	d8:00.0	3	03037	10.160.128.58	HMPID-P2-JTAG-5R.cern.ch
6-LEFT	2	d8:00.0	4	03032	10.160.128.59	HMPID-P2-JTAG-6L.cern.ch
6-RIGHT	2	d8:00.0	5	03026	10.160.128.60	HMPID-P2-JTAG-6R.cern.ch

Using the JTAG :

- We need around 4 min to upload the firmware to all readout Cards.
- We need around 14 min to program the flash off all readout Cards

The programing operation is made in parallel !!!

After the Power On cycle the booting FPGA process need a few seconds.

Data acquisition :

- The communication with all the channel was tested successfully.
- The data taking and local store was tested using LTU trigger.

The HMPID electronic is working in the RUN3 environment !!!

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HMPID performance at 100KHz of trigger rate, P2.

One year ago the theoretical expectations of doubling the readout frequency was proved at Lab581. HMPID electronics work stable at 100 kHz trigger rates throughout different percentages of occupancy.

ALICE-HMPID plenary meeting CERN − 14/12/2018
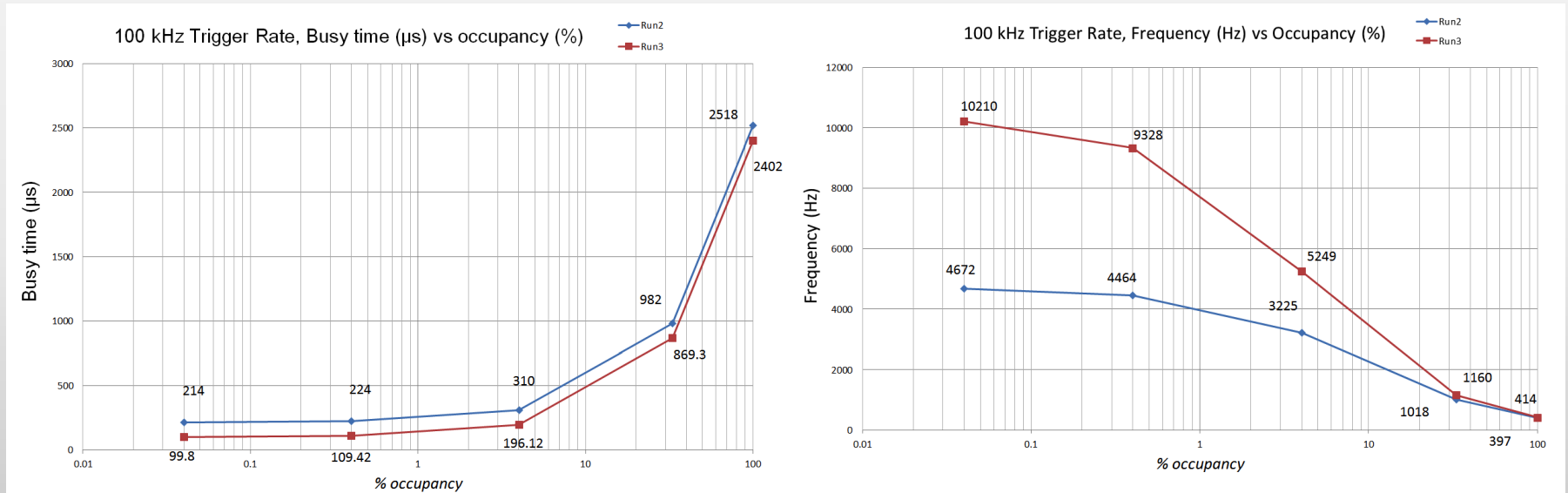
100 kHz Trigger Rate, Busy vs Occupancy, Run2 vs Run3

100 kHz Trigger Rate, Frequency vs Occupancy, Run2 vs Run3

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HMPID performance at 100KHz of trigger rate, P2.

BUSY TIME (us) vs OCCUPANCY (%)

	100%	40%	10%	4.00%	0.40%	0.20%	0.01%
0L	1843.20	614.40	281.60	140.80	76.80	65.83	64.00
0R	1848.83	769.83	281.60	140.80	76.80	67.66	64.00
1L	1843.20	832.00	281.60	135.31	76.80	67.66	64.00
1R	1935.77	832.00	281.60	135.31	76.80	76.80	64.00
2L	1843.20	832.00	266.97	140.80	76.80	67.66	76.80
2R	1871.37	800.91	281.60	140.80	76.80	76.80	64.00
3L	1843.76	832.00	281.60	135.31	76.80	71.31	64.00
3R	1843.20	832.00	281.60	140.80	76.80	71.31	65.83
4L	2969.60	1139.20	577.83	448.00	376.69	371.20	371.20
4R	1843.20	832.00	281.60	140.80	76.80	67.66	67.66
5L	1880.36	738.74	266.97	140.80	76.80	71.31	64.00
5R	1843.20	832.00	281.60	129.83	76.80	73.14	64.00
6L	1847.98	713.14	237.71	128.00	76.80	64.00	64.00
6R	1843.20	832.00	281.60	140.80	76.80	71.31	64.00

Legend: 0L, 0R, 1L, 1R, 2L, 2R, 3L, 3R, 4L, 4R, 5L, 5R, 6l, 6R

busy time (us) vs occupancy %

The current firmware is a full VHDL version, with internal busy time counter.

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HMPID performance at 100KHz of trigger rate, P2.

Module 4 Left
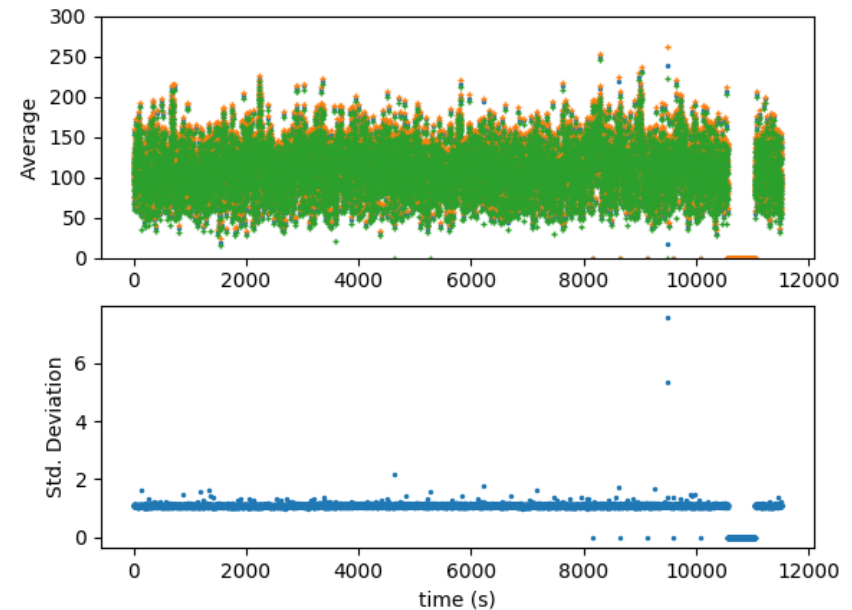
The controller of the column 23 is not working. The firmware wait for the arrive of the start column marker, then if after a fixed numbers of clock it not arrive the firmware send an error and continue to the next column.

This loop increase the busy time for the module. We need to fix the column controller or mark the column as bad in order to skip the waiting loop.

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HMPID software integration to O2 framework.

GitLab repository: https://gitlab.cern.ch/rarteche/hmpid-readout-software

HMPID software integration to O2 framework.

ReadoutCard (RoC) module, Python integration.

GUI Python App for readout local data taking
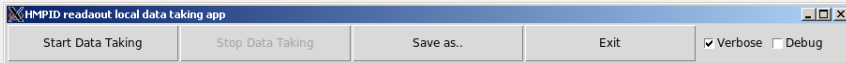
GUI Python App for Write and Read Pedestals and thresholds.
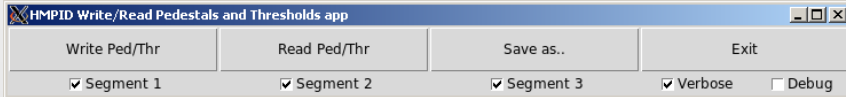
- L0Delay.py, L0Delay0ns.py, L0Delay100ns.py, L0Delay200ns.py are used to set L0 delay at different time.
  L0Delay.py --id=3b:00.0 --channel=0 --verbose
- L1Latency.py is used to set L1 Latency.
  L1Latency.py --id=3b:00.0 --channel=0 --verbose
- WritePedThr.py is used to send to the FEE the pedestals and thresholds.
  WritePedThr.py --id=3b:00.0 --channel=0 --verbose
- ReadPedThr.py is used to get the pedestals and thresholds from the FEE.
  ReadPedThr.py --id=3b:00.0 --channel=0 --verbose
- RstBusy.py is used to reset the busy line.
  RstBusy.py --id=3b:00.0 --channel=0 --verbose
- RstFSM.py and RstMainFSM.py are used to reset the FSMs in the firmware.
  RstFSM.py --id=3b:00.0 --channel=0 --verbose
- RstTTCRx.py and RstTTCRxLong.py are used to reset the TTCRx module.
  RstTTCRx.py --id=3b:00.0 --channel=0 --verbose
- DataRead.py is used to start a local data taking.
  DataRead.py --id=3b:00.0 --channel=0 –verbose

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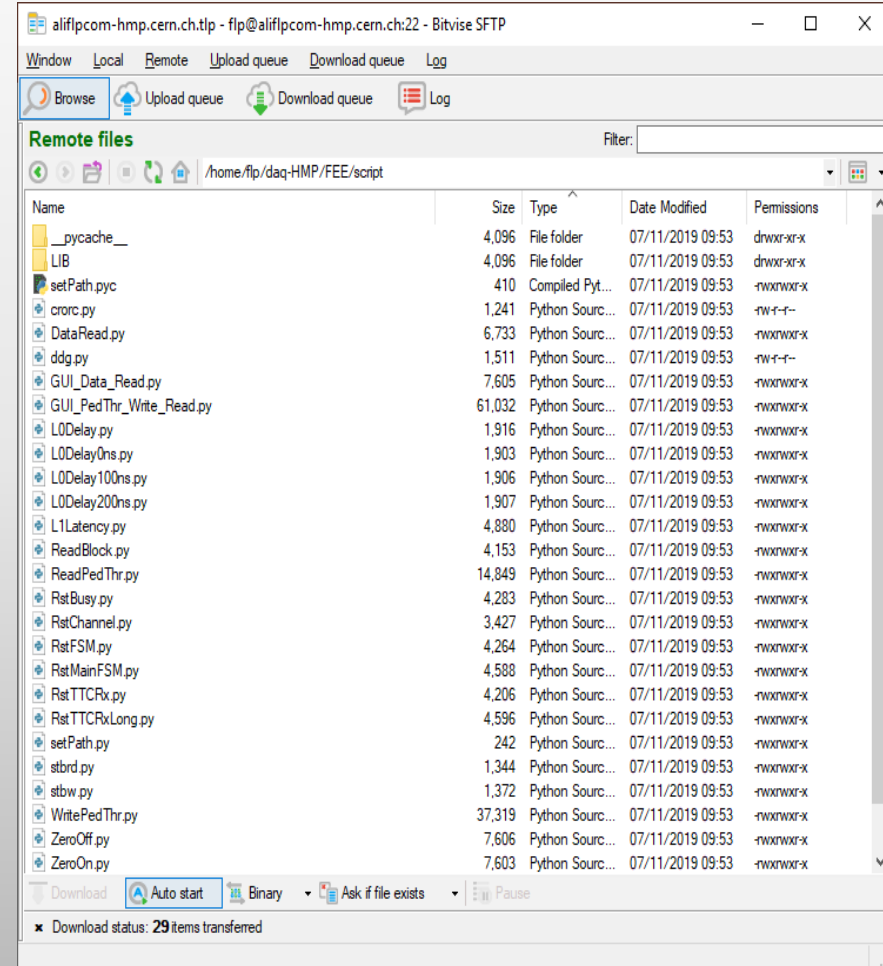
HMPID software integration to O2 framework.

ReadoutCard (RoC) module, C++ integration.

Commands line utilities developed in C++ using O2 framework. The programs call directly the functions of the ReadoutCard library, also is possible to compile directly in the FLP machine. Source include the instructions of how to compile it.
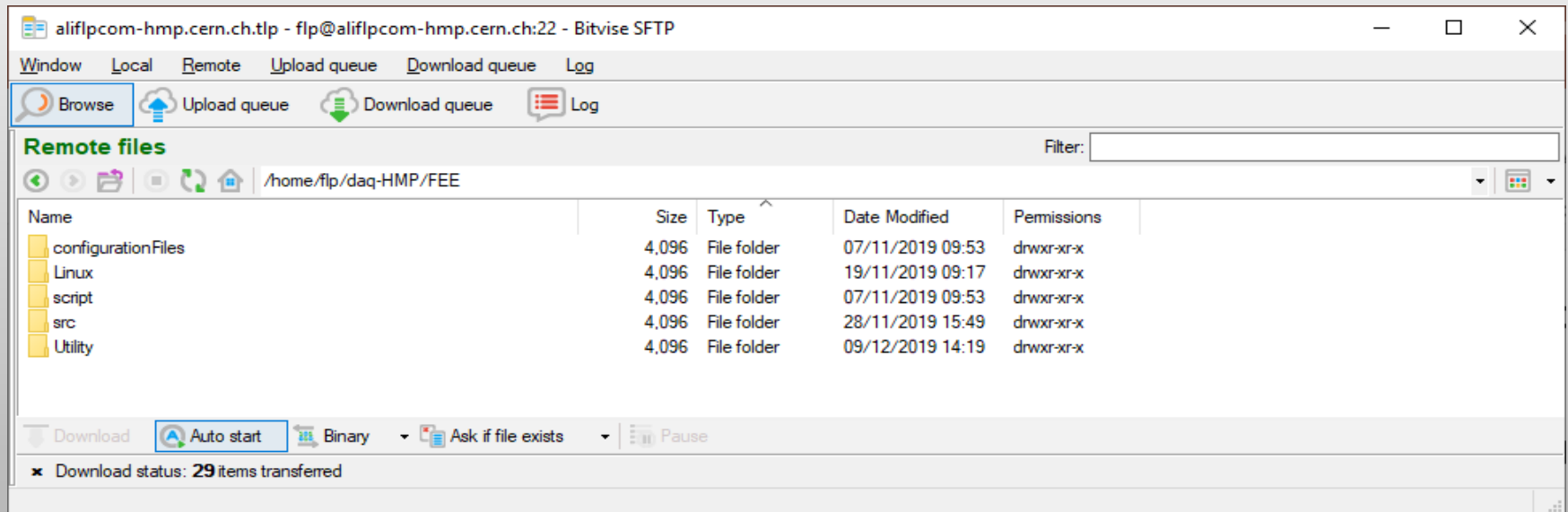
HMPID software integration to O2 framework.

Software used during the detector commissioning.

Basically, three command line utilities are used in this phase.

- hmpid-Write-PedThr-v14 --verbose --id=3b:00.0 --channel=0

- hmpid-Zero-On-v14 --verbose --id=3b:00.0 --channel=0

- hmpid-roc-bench-dma-v14 --verbose --id=3b:00.0 --dma-channel=0 --no-errorcheck --data-source=FEE
  --to-file-bin=/tmp/data_on_0L.raw --bytes=100M

Ansible role was prepare at *aliflpcom-hmp.cern.ch*

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# HMPID ReadOut tools

HMPID ReadOut tools

- hmpReadRawFile3-3.py : program to read raw files, check errors and display the file contents

    - hmpReadRawFile3-3.py <inputRawFile> <verbosity>

    - <verbosity> := -1..9

- hmpConvertRawFile3-3.py : program to extract from raw files the values of PAD charges in ASCII format

    - hmpConvertRawFile3-3.py <sourceRawFile> <destinationFile> <verbosity>

    - <verbosity> := 0,1

    - Example of output:

    - # HMPID RUN3 Event dump : v.1.1 - A.Franco 6/11/2019

    - # Column Dilogic Channel Charge [Column == -1 -> Start of Event]

    - -1 2017 34546 34546 0 4294967295

    - 1 1 0 100

    - 1 1 1 109

- hmpDisplayMapRun3-3.py : program to generate a PAD map

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The VHDL firmware

- The old RCB FPGA firmware was written in AHDL (Altera Hardware Description Language). The current firmware is written in VHDL but conserving the same architecture.
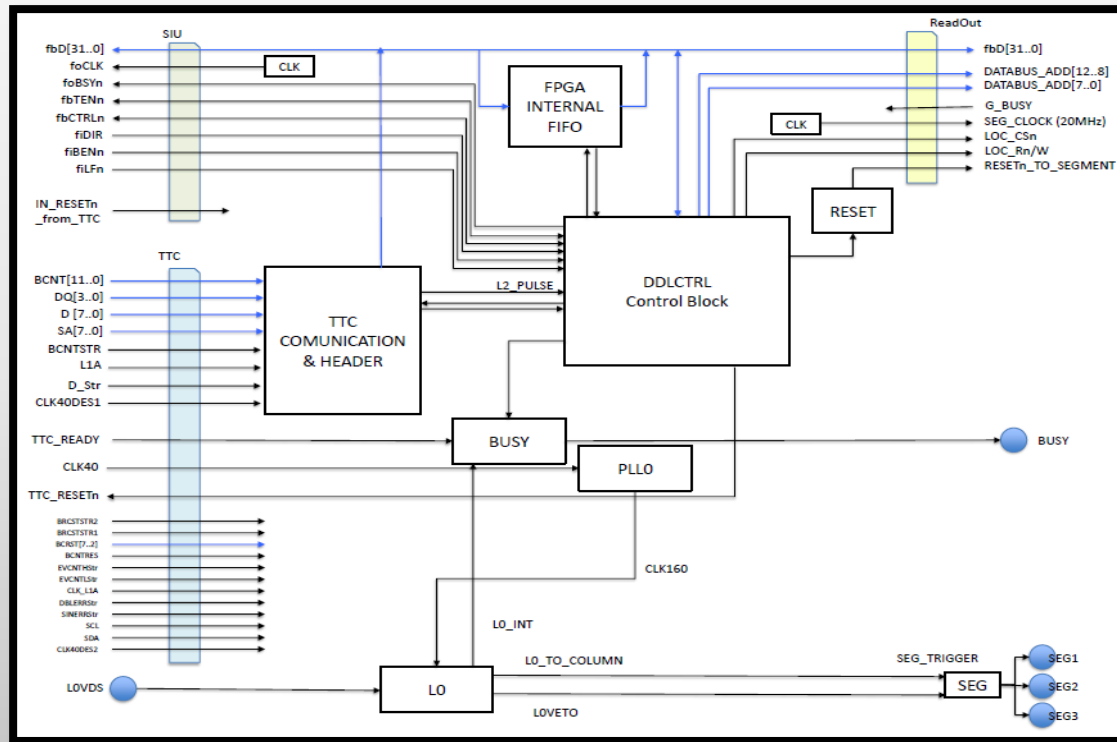
- The DDL controller is finish, some new requirement could be include if is needed.

- The final version of the TTC communication module is going to be finish in the first month of 2020.

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Conclusions

- The HMPID is working in the RUN3 environment with very good performance.

- We have the necessary software tools, to continue it integration to the rest of the O2 framework.

- More analysis need to be done in the acquired data in order to know better the status of the electronic and plan any intervention if is needed.

- More job is coming!!!.

Thank you

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