Radiation effects in the LHC experiments and impact on operation and performance.

Contact: Ian.Dawson@cern.ch
Editors: M. Bindi, M. Bomben, E. Butz, A. de Cosa, I. Dawson, S. Mallows, M. Moll, B. Nachman, J. Sonneveld

Abstract
This report documents the knowledge and experience gained by the LHC experiments in running detector systems in harsh radiation environments, with focus on inner detector systems. Run 2 finished in December 2018 with unprecedented integrated luminosity delivered to the experiments. The deleterious effects of radiation is increasingly impacting detector operation and performance and measurements have been made across the LHC experiments. It is timely to review the situation and establish if the detector systems are operating and performing as expected. We would like to know how well the radiation damage is being modelled and monitored? And how accurate are the radiation background simulations? Have there been unexpected effects? What mitigation strategies have been developed? The goal of this report is to provide a major reference for future upgrades and for future collider studies, summarising the experiences and challenges of designing complex detector systems for operation in harsh radiation environments.

Keywords
Radiation, damage, simulation, LHC, experiments
## Contents

1. Introduction .................................................. 3
2. Overview of radiation effects on detector systems ............... 4
   2.1 Sensors .................................................. 4
   2.2 Electronics ............................................. 4
   2.3 Optoelectronics ......................................... 4
   2.4 Services ................................................. 4
3. Simulation of radiation environments .............................. 5
   3.1 Event generation ........................................ 5
   3.2 Particle transport codes ................................ 5
   3.3 Simulation frameworks ................................... 5
   3.4 Fluence and dose predictions .............................. 5
4. Measurements of radiation damage on sensors ..................... 6
   4.1 ATLAS .................................................. 6
   4.2 CMS ..................................................... 6
   4.3 LHCb ..................................................... 6
   4.4 ALICE .................................................. 6
   4.5 Inter-experiment comparisons .............................. 6
   4.6 Extracting fluence from measurements ...................... 6
   4.7 Discussion .............................................. 6
5. Impact of radiation on electronics & optoelectronics (30pp) .... 7
   5.1 ATLAS .................................................. 7
   5.2 CMS ..................................................... 16
   5.3 ALICE and LHCb ......................................... 16
   5.4 Inter-experiment comparisons .............................. 16
   5.5 Discussion and future strategies ........................... 16
6. Simulating radiation effects in silicon sensors and modelling charge response .... 20
   6.1 ATLAS .................................................. 20
   6.2 CMS ..................................................... 20
   6.3 LHCb ..................................................... 20
   6.4 ALICE .................................................. 20
   6.5 Inter-experiment comparisons .............................. 20
   6.6 Discussion .............................................. 20
7. Conclusions .................................................. 21
1 Introduction

This report documents the knowledge and experience gained by the LHC experiments in running detector systems in harsh radiation environments, with a focus on inner detector systems. The deleterious effects of radiation is increasingly impacting detector operation and performance and measurements and observations have been made across the LHC experiments. It is timely to review the experiences of the LHC experiments and ask if the detector systems are operating and performing as expected? How accurate are the radiation damage models and predictions? Have there been unexpected effects? What mitigation strategies have been developed? Our understanding and modelling of radiation effects was originally tested in irradiation facilities, so strong motivation to cross check in-situ in the complex radiation fields of the LHC?

The goal of this report is to provide a major reference for future upgrades and for future collider studies, summarising the experiences and challenges of designing complex detector systems for operation in harsh radiation environments. In section 2 we discuss the current knowledge on the effects of radiation on detector systems. In section 3 we describe how the radiation environments ...
2 Overview of radiation effects on detector systems

Editors: M. Moll, I. Dawson, A. Nother?

A general introduction/overview on effects of radiation – we could possibly merge this section into the other sections, but my view is it’s better to separate the theory from the measurements as much as possible? We could also briefly describe in this section how radiation challenges in our field differ to other industries?

2.1 Sensors
Leakage currents, depletion voltage, CCE, etc.

2.2 Electronics
SEUs etc.

2.3 Optoelectronics
Section on relevant opto/photonic (fibres, LEDs and lasers, etc.)

2.4 Services
Anything to say here apart from scattering and activation?

References
3 Simulation of radiation environments

Editors: I. Dawson, S. Mallows

Write introduction discussing:

– The need of simulation for radiation background studies, starting with event generation followed by transport of particles in detector material.
– During design phase rely on radiation simulation predictions – extrapolating from lower centre of mass collision energies. Challenge in determining uncertainties on the predictions. Safety factors?
– Typical requirements of the experiments: 1 MeV neq fluence; ionising dose; hadrons > 20 MeV; residual dose rates

3.1 Event generation

General discussion on event generator codes available for describing minimum bias \( pp \) collisions. ATLAS uses PYTHIA8, CMS and LHCb use FLUKA embedded DPMJET. (Say something about ALICE, TOTEM, LHCf ?)

3.1.1 PYTHIA
3.1.2 DPMJET

3.2 Particle transport codes

General discussion on on particle transport codes used in the LHC experiments. ATLAS uses both FLUKA and GEANT4, CMS and LHCb use FLUKA.

3.2.1 FLUKA & FLUGG
3.2.2 MARS
3.2.3 GEANT3/CALOR
3.2.4 GEANT4

3.3 Simulation frameworks

For example, ATLAS uses Git repository for shared geometry development – shared with RP. Web tools. TWikis?

3.4 Fluence and dose predictions

3.4.1 ATLAS
3.4.2 CMS
3.4.3 LHCb
3.4.4 ALICE

References
4 Measurements of radiation damage on sensors

Editors: A. De Cosa, B. Nachman

General introduction on the effects of radiation on sensors, though I propose details should go in section 2. Here we should focus on the experiment measurements, and how they compare to the predictions from simulation and modelling.
For presenting results I think easiest to summarise studies and conclusions for each experiment first, as we did in the workshops, then try to extract combined conclusions? A crude outline given below ...

4.1 ATLAS
4.1.1 Sensor leakage current measurements and comparison with predictions
4.1.2 Sensor depletion voltage measurements
4.1.3 Ionising dose monitoring
4.2 CMS
4.3 LHCb
4.4 ALICE
4.5 Inter-experiment comparisons
4.6 Extracting fluence from measurements
4.7 Discussion
Drawing conclusions from across the experiments.

References
In this chapter we will present the results of the impact of radiation on electronics and opto-electronics for the four LHC experiments during Run1 and Run2. ATLAS results are presented in section 5.1; CMS in section 5.2 whilst LHCb and ALICE observations are described in section 5.3. In section 5.4 we will present the comparison between the various experiments; finally, in section 5.5, some guidelines and suggestions for building and operating electronics and opto-electronics in future LHC experiments will be given.

5.1 ATLAS

Contributing author: M. Bindi;

The ATLAS Inner Detector (ID) has been designed to provide hermetic and robust pattern recognition, excellent momentum resolution and both primary and secondary vertex measurements for charged tracks within the pseudorapidity range $|\eta| < 2.5$.

The ID layout, described in [1], reflects the performance requirements: the ID is contained within a cylindrical envelope of length $3512 \text{ mm}$ and of radius $1150 \text{ mm}$, within a solenoidal magnetic field of $2 \text{ T}$. The ID consists of three independent but complementary sub-detectors: at inner radii, high-resolution pattern recognition capabilities are available using discrete space-points from the silicon Pixel detector ($r \leq 122.5 \text{ mm}$) and stereo pairs of silicon microstrip from the Semiconductor Tracker (SCT) ($299 \geq r \leq 514 \text{ mm}$); at larger radii ($563 \geq r \leq 1066 \text{ mm}$), the transition radiation tracker (TRT) comprises several layers of gaseous straw tube elements interleaved with transition radiation material.

The performance of the ATLAS experiment depends critically on the innermost layer (B-layer) of the Pixel detector. For this reason, at the beginning of 2013 the detector underwent the first of three long shutdown (LS) phases planned by the LHC machine. During this period (LS1), a fourth pixel layer based on new technology, the Insertable B-Layer (IBL) [2], was added to the pixel detector between a new, narrower Beryllium beam-pipe and the pre-existing B-Layer.

Fig. 1 shows the r-z layout of the upgraded ID during Run-2.

At the same time, during LS1, pixel services were replaced by new ones (new Service Quarter Panel, or nSQP).

After resuming data-taking in 2015, ATLAS has successfully operated the ID during Run-2 at $\sqrt{s} = 13 \text{ TeV}$ and instantaneous luminosities surpassing the design value of $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The total integrated luminosity collected till 2019 by Pixel, SCT and TRT detectors is $\sim 190 fb^{-1}$ whilst the IBL detector, operating only during Run 2, collected a luminosity of $\sim 159 fb^{-1}$.

Radiation effects from TID on the IBL front-end electronics will be described in section 5.1.1; SEU/SET effects from highly ionizing particles in IBL and SCT detector will be shown in section 5.1.2 whilst impact on opto-electronics from SCT will be described in section 5.1.3. Finally, results from TRT electronics will be presented in section 5.1.4.

5.1.1 TID effects in the IBL front-end chip (4 pp)

Contributing authors: M. Backhaus; A. LaRosa;

The IBL consists of 14 carbon fibre staves instrumented along 64 cm, 2 cm wide, and tilted in $\phi$ by $14^\circ$ surrounding the beam-pipe at a mean radius of 33 mm from the beam axis and providing a pseudo-rapidity coverage of $\pm 3$. Each stave, with integrated CO$_2$ cooling, is equipped with 32 front-end chips bump bonded to silicon sensors.
The IBL detector was designed to be operational until the end of the LHC Run 3, where the total integrated luminosity was expected to reach $300 \text{ fb}^{-1}$. The detector components are qualified to work up to 250 Mrad of total ionising dose (TID). The IBL front-end chip, namely FE-I4 [3], was designed in 130 nm CMOS technology which features an array of 80 x 336 pixels with a pixel size of $50 \times 250 \mu\text{m}^2$. Each pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The FE-I4 keeps track of the time-over-threshold (ToT) of each discriminator with 4-bit resolution, in counts of an external supplied clock of 40 MHz frequency. The FE-I4 operates by feeding the common power supply to analog signal amplifiers and digital signal-process circuits, referred to as the low-voltage (LV) power supply and the clock input.

### 5.1.1.1 Observations during 2015 data taking

During the first year of the IBL operation in 2015, a significant increase of the LV current of the front-end chip and the detuning of its parameters (threshold and time-over-threshold) have been observed in relation to the received TID.

The LV current of the FE-I4 chip was stable at a value of 1.6–1.7 A (for a four-chip unit) until the middle of September 2015. Then, the current started to rise up significantly (see Figure 2), and the change of the current during September to November 2015 was more than 0.2 A even within a single LHC fill, depending on the luminosity and the duration of the fill.

With the increase of the LV current, the temperature of IBL modules also changes (Figure 3).
Fig. 2: Mean low voltage (LV) current in IBL FE-I4 chips during stable beam as a function of integrated luminosity and total ionising dose (TID). In the period from September to November 2015 the IBL detector was switched off during one LHC fill (due to safety concerns in early October 2015). The mean LV currents are averaged for all modules across 100 luminosity blocks and there is no obvious dependence of LV current on module group position. The TID is calculated from integrated luminosity [4].

In addition, as shown for example in Figure 4, the calibration of the FE-I4 chips for the analog discriminator threshold and the target ToT were observed to drift rapidly despite frequent updating of the calibration.

The increase of the LV current of the FE-I4 chip and the drifting of its tuning parameters were traced back to the generation of a leakage current in NMOS transistors induced by radiation higher than usual. The radiation induces positive charges that are quickly trapped into the shallow-trench-insolation (STI) oxide at the edge of the transistor. Their accumulation builds up an electric field sufficient to open a source-drain channel where the leakage current flows. If the accumulation of positive charges is relatively fast, the formation of interface states is a slower process. The negative charges trapped into interface states start to compete with the oxide-trapped charges with a delay. This is what gives origin to the so called rebound effect [5].
Fig. 4: The time-over-threshold (ToT) and its RMS as a function of the integrated luminosity or total ionising dose (TID) [4]. The detector was regularly retuned, and each marker type corresponds to a single tuning of the detector.

5.1.1.2 Irradiation test-results

Dedicated laboratory measurements [6] of irradiated single transistors in 130 nm CMOS commercial technologies showed that the increase of the leakage current reaches its peak value between 1 Mrad and 3 Mrad. For higher TID the current decreases to a value close to the pre-irradiated one.

To reproduce and analyse the effects described above during the FE-I4 chip operation, several irradiations and electrical tests were performed [4]. Since the current increase in NMOS transistors depends on dose rate and temperature, measurements under different temperature and dose rate conditions have been carried out to qualify this dependency.

The first irradiation test aimed at measuring the boundary current (at a given temperature and dose rate) that the chip always approaches after annealing periods and re-irradiation. Figure 5 shows the increase of the current consumption of a single FE-I4 chip in data taking condition as a function of the TID. The temperature of the chip was 38 °C and the dose rate 120 krad h$^{-1}$. After reaching the maximum of each peak the chip was annealed for several hours resulting in the observed partial recovery. Then, to study

Fig. 5: Current consumption of a single FE-I4 chip in data taking condition as a function of the total ionising dose (TID). The temperature of the chip was 38 °C and the dose rate 120 krad h$^{-1}$. After reaching the maximum of each peak the chip was annealed several hours resulting in the observed partial recovery [4]. The fit performed on the first set of data (first peak) has been carried out by using the current parametrisation described in Ref. [7].
the dependence of the LV current increase on temperature and dose rate several irradiation tests were performed by setting one of those variables and changing the other. Figure 6 shows the results of three different measurements, performed with three different and previously not irradiated chips. The dose rate was 120 krad h$^{-1}$ and the temperatures were 38°C, 15°C and −38°C. Before irradiation the LV current of the three chips was 400 mA (38°C), 360 mA (15°C) and 380 mA (−38°C). For comparison Figure 7 shows the result of two different measurements where the temperature was kept fix at 15°C, while the dose rate set to 120 krad h$^{-1}$ or 420 krad h$^{-1}$. Also in this case the tests were performed with different and previously not irradiated chips. The measurements described above revealed two facts:

**Fig. 6:** Increase of the LV current of three single FE-I4 chips in data taking condition as a function of the total ionising dose (TID) in logarithmic x-axis scale. Test measurements were carried out at 38°C (blue points), at 15°C (black points) and at −15°C (red points) with a dose rate of 120 krad h$^{-1}$. A dose rate up to 10 krad h$^{-1}$ is expected in the experiment. The LV current of the single FE-I4 chips before irradiation were 400 mA (38°C), 360 mA (15°C) and 380 mA (−38°C) [4].

**Fig. 7:** Increase of the LV current of two single FE-I4 chips in data taking condition as a function of the total ionising dose (TID) in logarithmic x-axis scale. Test measurements were carried out at 15°C with a dose rate of 120 krad h$^{-1}$ (red points) and 420 krad h$^{-1}$ (black points). A dose rate up to 10 krad h$^{-1}$ is expected in the experiment. The LV current of the single FE-I4 chips before irradiation were 380 mA (420 krad h$^{-1}$) and 360 mA (120 krad h$^{-1}$) [4].
at a given dose rate the LV current increase is stronger at lower temperatures;
- at a given temperature, the LV current increase is stronger at higher dose rates.

To simulate the dose rate conditions of the 2015 and 2016 data taking, a first irradiation was performed at $-15^\circ$C and 120 krad h$^{-1}$. This was followed by several hours of annealing and a second irradiation this time performed at $5^\circ$C and 420 krad h$^{-1}$. As shown in Figure 8 the second LV current peak is lower than the first one, i.e. by increasing the operational temperature of the chip it was possible to keep the increase of the LV current below the boundary current given by the first irradiation. To verify that a temperature of $5^\circ$C is safe for the IBL detector operation, a measurement at 10 krad h$^{-1}$ was performed. The maximum LV current increase was of the order of 250 mA, which gives a LV current increase of 1 A for a four-chip unit, which would not exceed the safety limit of the LV current originally set to 2.8 A. In principle, lower operational temperatures are favourable for the sensor performance and properties after irradiation and therefore preferred. Consequently, irradiation and electrical tests were also performed at a temperature of $0^\circ$C to investigate the feasibility for a colder operation. In addition it was investigated the evolution of the maximum of the LV current peak under several irradiation steps followed, interleaved with periods of annealing. In this case the first two consecutive peaks of the LV current increase exceeded the maximum current allowed for a safe detector operation. Therefore, it was decided to set $5^\circ$C as minimum temperature for a safe and successful data taking.

**5.1.1.3 Detector operation guidelines**

Based on the observations during the first year of data-taking in 2015 with the IBL detector, it was decided to raise the safety limit for the IBL LV currents from 2.8 A to 3 A for module groups of four chips, which means a current consumption of 750 mA per chip. Since the average current consumption for a single FE-I4 chip is about 400 mA before irradiation, the increase of the current due to the TID effects can not be higher than 350 mA per chip.

Given the above results it was decided to increase the IBL operation temperature from $-10^\circ$C to $15^\circ$C. In addition, the digital supply voltage ($V_D$) was lowered from 1.2 V to 1 V to decrease the LV current. Thanks to dedicated measurements at $5^\circ$C and at a dose rate comparable to the LHC in 2016 (10 krad h$^{-1}$), it is proven that the current increase is of the order of 250 mA. With this a module group
of four chips does not exceed the safety limit of 3 A. Therefore operating the IBL detector at 5 °C is safe with respect to the expected luminosity in 2016. The temperature of the IBL cooling system was lowered to a set point of 5 °C. The digital supply voltage (\(V_D\)) was raised from 1 V to 1.2 V, after an accumulated dose of ∼5 Mrad which, as the measurements show, is well beyond the high peak region for the current consumption.

An overview of the mean LV current of the IBL FE-I4 chips as a function of integrated luminosity and total ionising dose (TID) during stable beam is shown in Figure 9. The LV currents are averaged for all modules across 100 luminosity blocks (∼100 minutes), and the changes in digital supply voltage (\(V_D\)) and the temperature (\(T_{\text{Set}}\)) are highlighted. In addition, since the shift of the tuning parameters can be seen even at low dose rates and warmer temperatures, a retuning on a regular basis was performed.

### 5.1.1.4 Summary

During the first year of data taking in 2015, a peculiar increase of the LV current of the FE-I4 chip and the detuning of its parameters (threshold and time-over-threshold) have been observed in relation to received total ionising dose. It was tracked back to the generation of a leakage current in NMOS transistors induced by radiation. Dedicated irradiation and electrical tests of FE-I4 chips showed that the leakage current reaches its peak value when the total ionising dose is in the range of 1 Mrad – 3 Mrad, and above this the current decreases to a value close to the pre-irradiation one. This effect was shown to be temperature and dose rate dependent.

Thanks to intensive studies it was possible to apply special detector settings to still guarantee a successful data-taking.

### 5.1.2 SEU/SET studies on IBL and SCT detectors (4 pp)

Contributing authors: M. Bindi; A. Rozanov; D. Robinson.

An overall theoretical description of SEU/SET effects in electronics was given already in Sec. 2.2. In this section we will present the experimental observations on the ATLAS IBL and SCT detectors, giving the results of detail studies performed during the LHC Run 1 and Run 2 periods, including the adopted mitigation strategies and the plans for the future operation in Run 3.
5.1.2.1 SEU and SET measurement in IBL front-end chips

The readout integrated circuits in the ATLAS IBL detector are custom designed with SEU-hardened memory cells \[8\] (Dual Interlocked CElls or DICE latches \[9\] and triple redundancy). These reduce the SEU rate, but do not completely eliminate it. The effects of SEUs were indeed visible in the behaviour of the FEs during 2017, when the LHC peak instantaneous luminosity increased further respect to 2016 and was constantly above $1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Under these conditions, more frequent front end chip reconfigurations were needed to preserve good data quality and data taking efficiency.

![Graph showing effects of SEU on FE-I4 global registers](image)

**Fig. 10:** Effects of SEU on FE-I4 global registers can be seen during a typical LHC fill; in this case (fill 6046), the peak luminosity reached is $1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, and $490 \text{ pb}^{-1}$ were delivered over the entire fill. During the data taking, at luminosity block (LB) $\sim 268$, a drop in the LV current consumption can be observed. At the same time, a drop in occupancy is observed in one of the two DAQ modules that share the same LV power supply. At LB $\sim 277$, the critical DAQ module was manually reconfigured, bringing the LV current consumption and hit occupancy back to their values before the SEU.

Impacted FEs can stop sending hits, become very noisy, or experience large drops/increases (up to $\pm 100 \text{ mA}$) of the low voltage (LV) current consumption monitored from the Detector Control System (DCS) (see Fig. 10). Starting from 2016, part of the SEU/SET effects was treated by occasional manual or automatic reconfiguration of the problematic modules. However, to minimize the impact of SEUs on ATLAS data taking, it was decided to regularly reconfigure the global registers of the FE-I4 chips in the entire IBL.

Thanks to a joint effort of online software and firmware, it was possible to introduce this procedure without any additional dead time in ATLAS. Starting in August 2017, the global registers of the IBL FE-I4 chips were reconfigured every $\sim 5 \text{ s}$, improving the overall Data Acquisition (DAQ) efficiency and eliminating the low voltage current drops that were previously observed.

Unfortunately it was not possible to regularly reconfigure also the single pixel DICE latches in the FE-I4 since the needed software modifications were impacting the overall stability of the DAQ system. However, a test run was performed in July 2018 and can be used as proof of concept for future implementations.

The Global Configuration Memory of the FE-I4, located at the end of the column area outside of the pixel matrix region, is implemented as a memory block of 32 words of 16 bits (512 bits in total). The design used for this global memory is based on the triplication of the DICE latch to further suppress SEU.
Such triplication is not possible inside the pixel due to space constraints. An example of a fundamental parameter, vital for a proper chip functionality, is given by the global threshold, generated by a coarse and a fine DAC.

A 13 bit register is available to configure each single pixel, comprising a 1-bit enable flag, a 5-bit threshold tuning DAC (TDAC), a 4-bit time-over-threshold (ToT) tuning DAC (FDAC), a 1-bit HitBus (input to logical OR of all pixel discriminators outputs in the matrix), and 2 bits for the selection of the charge injection capacitor. The ToT represents the time of a single pixel discriminator being over threshold and has a 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz, that corresponds to the LHC bunch crossing (BC) time of 25 ns.

In data-taking configuration, the output enable bit mostly stores ones, as most of the pixels are enabled. However, there is a small fraction consisting of tenths of a percent of noisy pixels, which are disabled during calibration. The TDAC value is typically centered around fifteen, and the FDAC value is around seven. The capacitor selection bits are both set to one and the HitBus flag set to one (meaning HitOr disabled).

The occurrence of SEUs during data taking modifies both single pixel and global configurations, producing quiet pixels, noisy pixels introducing a general detuning of the FE-I4 and lowering the global thresholds or other parameters that impact severely on the correct chip functionality.

Fig. 11: Fraction of noisy pixels as a function of pixel TDAC during empty bunches of LHC fill 6343. TDAC values for each pixel are taken from the initial pixel configuration. The pixels with more than 200 hits in this fill are treated as noisy.

Fig. 11 shows the fraction of noisy pixels as a function of pixel TDAC during empty bunches of a typical LHC fill (6343 in 2017). TDAC values for each pixel are taken from the initial pixel configuration. The pixels with more than 200 hits in this fill are defined as noisy. Low values of TDAC correspond to high thresholds. The increase in the fraction of noisy pixels with initial TDAC < 15 indicates that some pixels become noisy due to the SEU flip 0 → 1 of the most significant bit (MSB) of TDAC, which lowers the pixel threshold by \( \sim 1850 \) e (with 2500 e being the typical discrimination threshold). No correlation of the noise with FDAC values was observed.

5.1.2.2 SEU in SCT front-end chips (4 pp)

- SCT (2 pp):
  - SEU expected rate vs observed rate. Highlight the discrepancy. References to Test beam studies.
  - Bit flip effects on de-synchronization
  - Explanation of mitigation strategies also for SCT.
Fig. 12: Average fraction of quiet pixels in each IBL chip ring after \(\sim 480 \text{ pb}^{-1}\) of data taking in LHC fill 7018 of 2018, compared with PYTHIA/FLUKA simulations. Four points are missing due to the reconfiguration tests happening during that fill in four specific front-end rings.

5.1.3 Optical links studies in SCT (2 pp)

Contributing authors: T. Weidberg, D. Robinson,

A description of radiation effects on VCSEL behaviour should go in the general part? Section 2.3?

– P-i-N diode: trends of the current consumption and depletion voltage estimate (test beam vs in-situ)
– VSEL: trends of current consumption from the Off detector electronics (test beam vs in-situ)

5.1.4 Irradiation effects in TRT electronics (2 pp)

Contributing author: S. Chen

5.2 CMS

5.3 ALICE and LHCb

5.4 Inter-experiment comparisons

5.5 Discussion and future strategies

Drawing conclusions from across the experiments.

References

Fig. 13: In figure (a), the Shift Register (SR) was set to 1, and \(0 \rightarrow 1\) flips dominate due to the SET on the LOAD line, while low rate \(1 \rightarrow 0\) flips are due to real memory SEU. In figure (b), the Shift Register was set to 0, and \(1 \rightarrow 0\) flips dominate. The values of the Shift Register are refreshed several times during the fill. The extrapolation of the measurement of SEU rate with 24 GeV protons on CERN PS is shown with blue line on the figure (b). During CERN PS measurement the value of SR was not refreshed which may explain higher rate of bit flips due to SET contribution.

Fig. 14: Average rate of SEU/SET bit flips in pixel memory of FE-I4 per fb$^{-1}$ in LHC fill 7334, as a function of bit number (0-12). In figure (a), the Shift Register was set to 1, and 0 → 1 flips dominate due to the glitches on the LOAD line, while low rate 1 → 0 flips are due to real memory SEU. In figure (b), the Shift Register was set to 0, and 1 → 0 flips dominate. The extrapolation of the measurement of the SEU rate with 24 GeV protons at CERN PS is shown with a blue line. During the CERN PS measurement, the value of the SR was not refreshed, which may explain higher rate of bit flips due to SET contributions.

Fig. 15: Cumulative fraction of SEU/SET bit flips in the Global Configuration Memory (GCM) of FE-I4 as a function of integrated luminosity in LHC fill 7333.
Fig. 16: The noise occupancy in IBL 3D modules as a function of integrated luminosity with and without the mechanism of pixel register reconfiguration at ECR.

Fig. 17: Fraction of quiet (a) or noisy (b) pixels versus integrated luminosity in fill 7018 from 2018, shown in the eight 3D IBL $\eta$ rings.

Fig. 18: Fraction of broken primary clusters versus integrated luminosity in fill 7018 from 2018, shown in the eight rings of 3D modules.
Simulating radiation effects in silicon sensors and modelling charge response

Editors: M. Bomben, J. Sonneveld
Contributing authors: M. Benoit, M. Bomben, E. Chabert, J. Merino, B. Nachman, L. Rossini, P. Sabatini, J. Sonneveld, C. Suarez, S. Swartz, T. Szumlak, A. Wang

Introduction ... TCAD etc.

6.1 ATLAS
6.2 CMS
6.3 LHCb
6.4 ALICE?
6.5 Inter-experiment comparisons
6.6 Discussion
Drawing conclusions from across the experiments.

References
7 Conclusions
References