Upgrade of the CMS Cathode Strip Chambers for the HL-LHC

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On behalf of the CMS Collaboration

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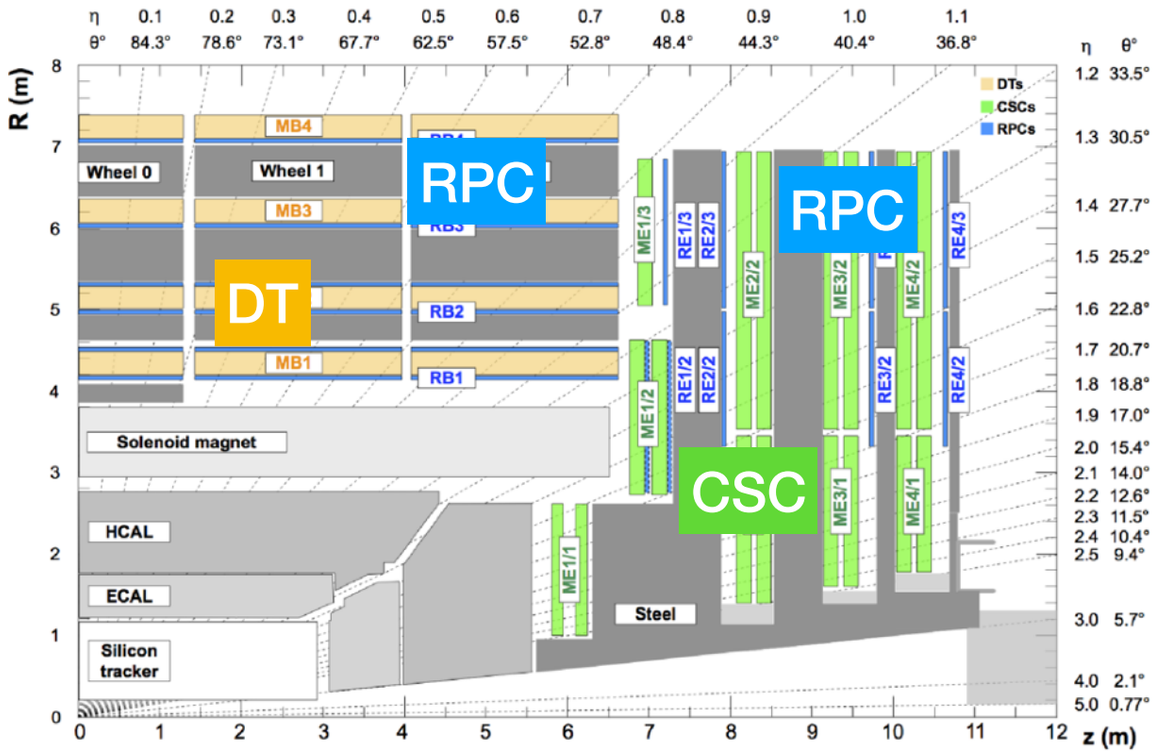
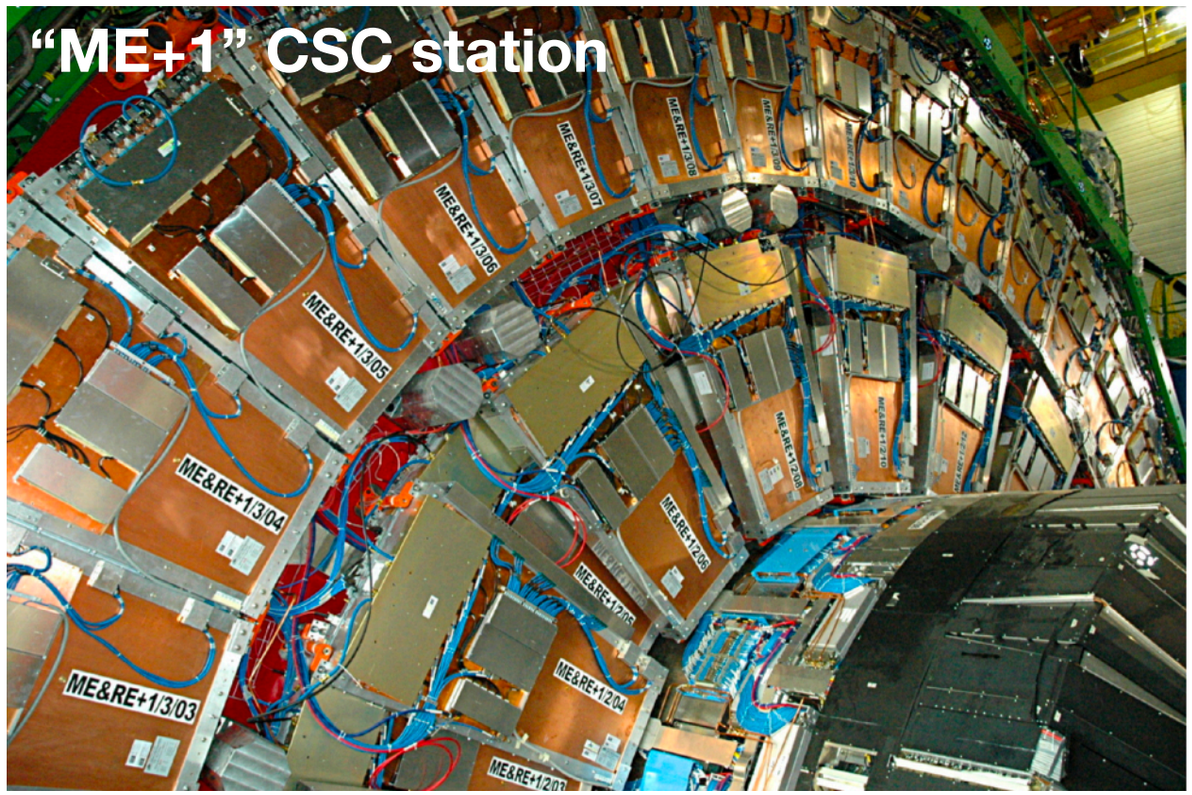
The CMS Muon System

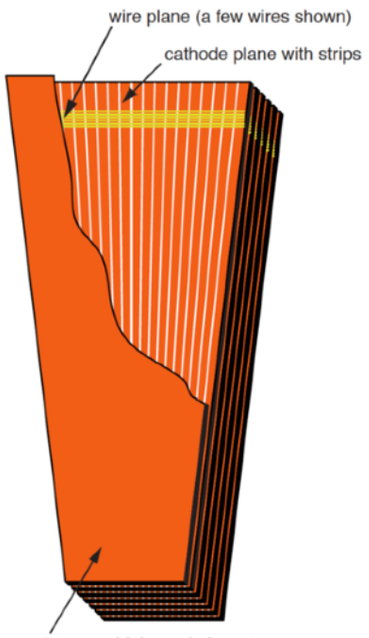
- The CMS detector uses three complementary systems to detect muons
  - ✓ Drift Tubes (DT) in the barrel region ($0.9 < |\eta| < 2.4$)
  - ✓ Cathode Strip Chambers (CSC) in the endcap ($0.9 < |\eta| < 2.4$)
  - ✓ Resistive Plate Chambers (RPC) in barrel and endcap ($0 < |\eta| < 1.8$)
- Gas Electron Multiplier (GEM) chambers to be installed in the forward region ($1.6<|\eta|<2.8$)



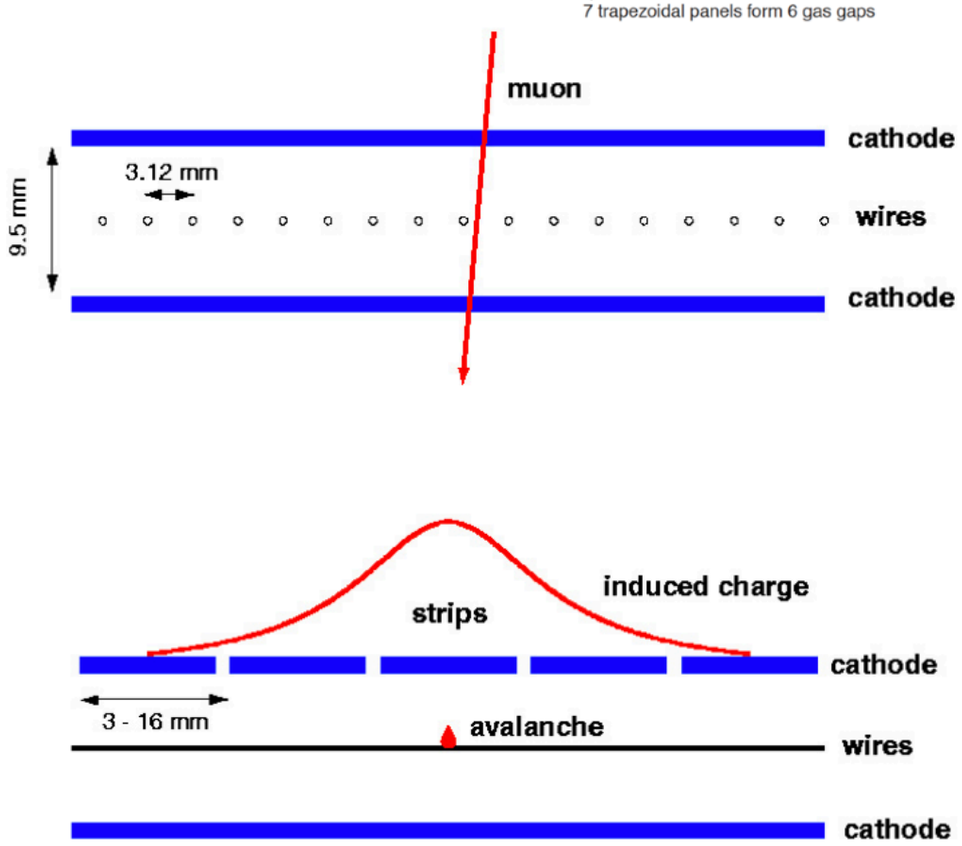


Cathode Strip Chambers

- Chamber design
  - ✓ Trapezoidal multi-wire proportional detectors (6 gas gaps each)
  - ✓ 270 CSCs installed in 4 stations in each endcap (540 total)
  - ✓ Finely segmented cathode strip and anode wire readout
  - ✓ Time resolution ~3.4 ns; position resolution ~50–145 μm



- Chamber Operation
  - ✓ Passing charged particle ionizes $Ar/CO_2/CF_4$ gas mixture
  - ✓ Electron amplification in strong electric field
    - ◉ Electrons captured by anode wires; induced image charge of anode signal captured by cathode strips
  - ✓ Coincidences of signals in multiple layers indicate passage of charged particle



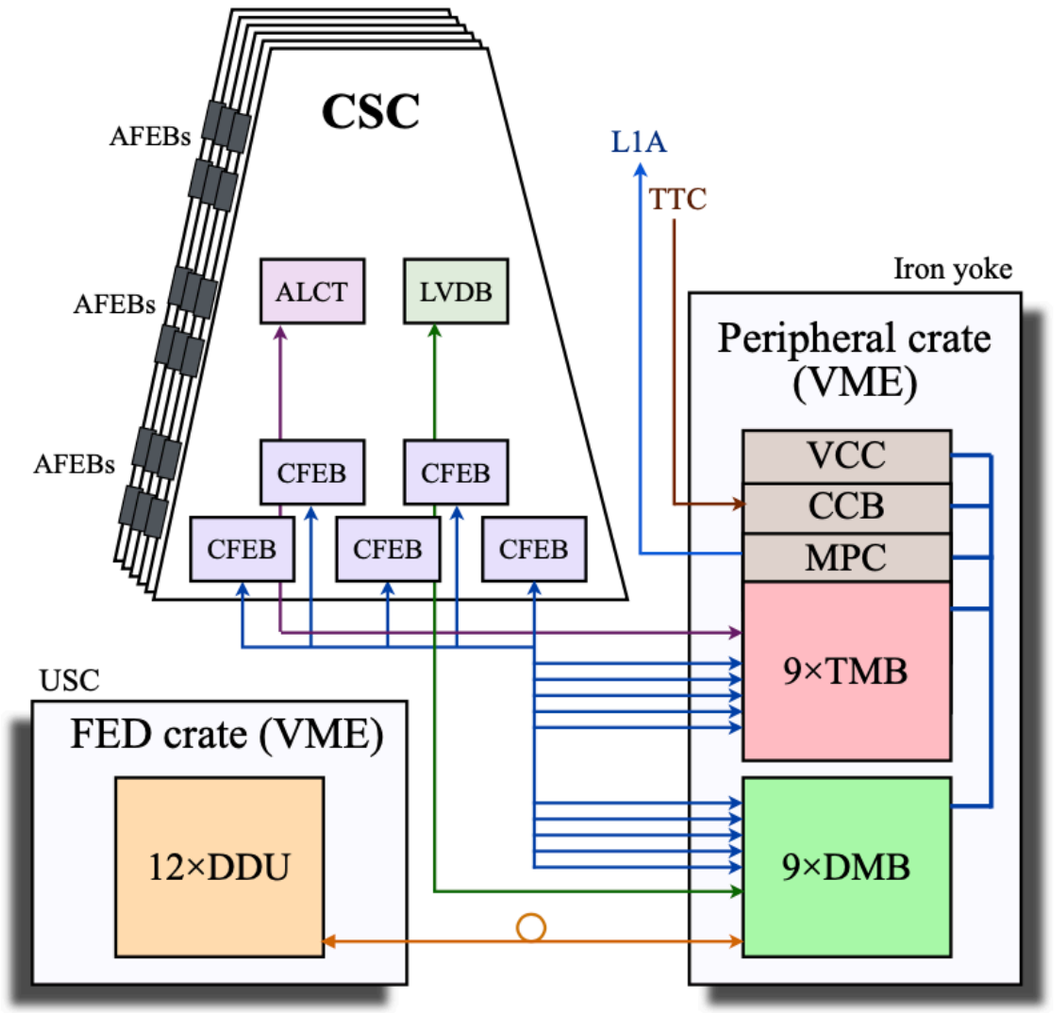
Electronics Design

Wire hits read out by Anode Front End Board

Processing anode hits into multi-layer coincidence in Anode Local Charged Track board

Strip hits read out by Cathode Front End Board

DDU: interface between CSC and CMS data acquisition system within Front End Driver crate



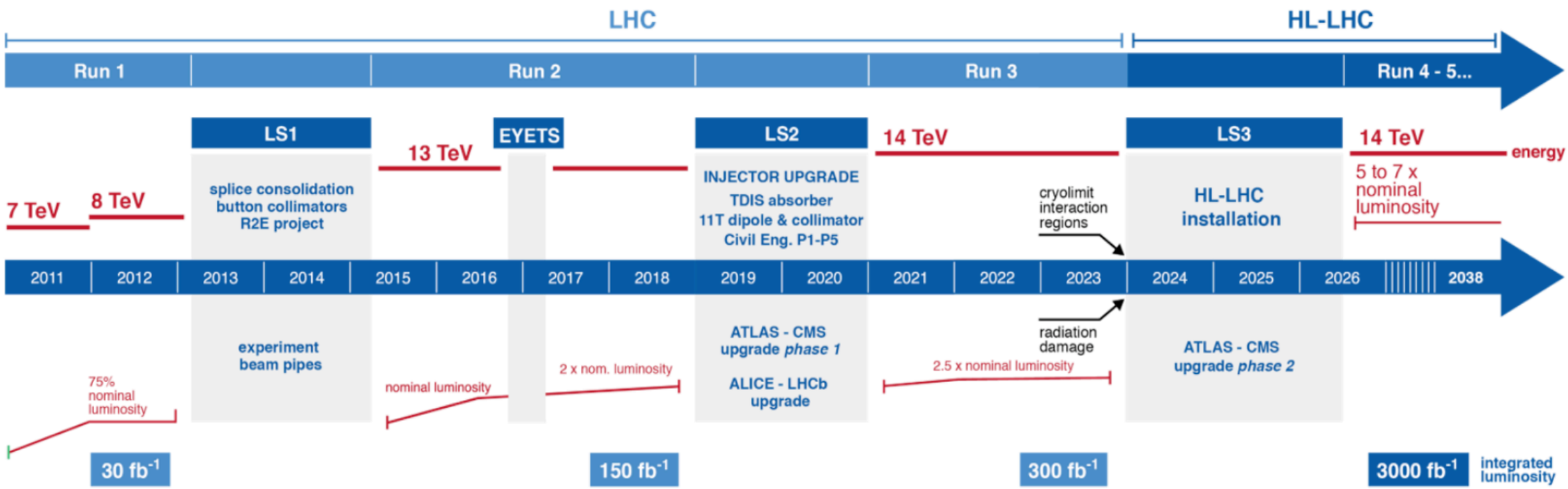
Low Voltage Distribution Board provides power

Clocking, data concentration and other services (VCC, CCB, MPC)

Processing multi-layer coincidences from cathode hits and ALCTs in (Optical) Trigger Motherboard

Data collection by Data Mother Board

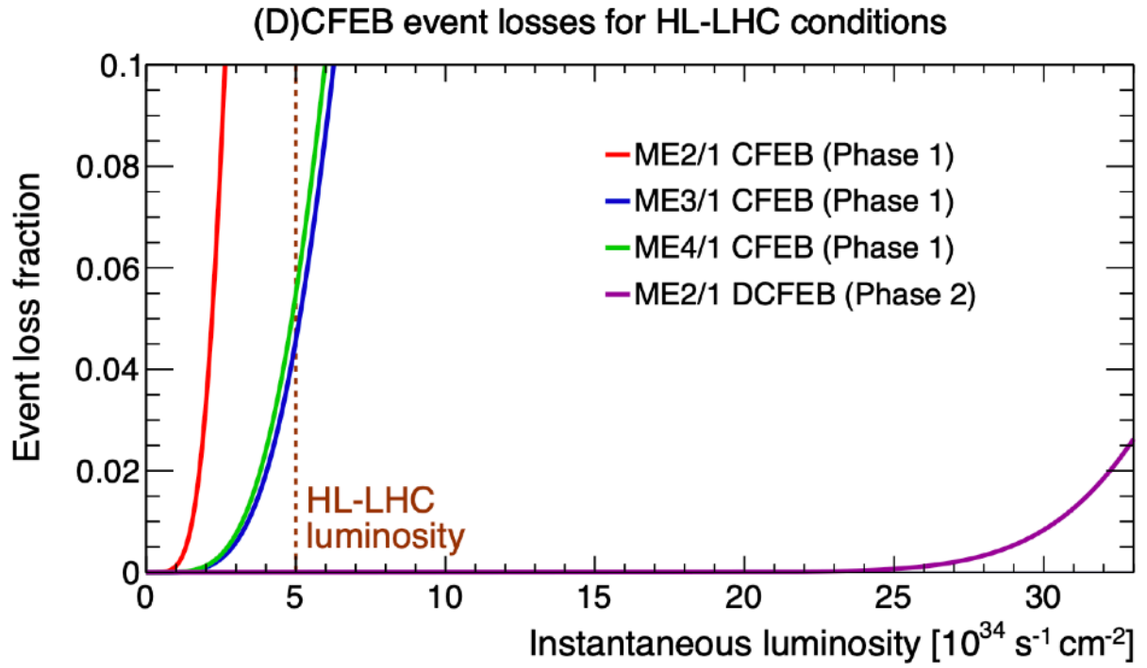
High-Luminosity LHC



- LHC will be upgraded to High-Luminosity LHC during LS3
  - ✓ 3000-4000 fb^{-1} of 14 TeV pp collision data over 10 years
  - ✓ Instantaneous luminosity increases to x5 -x7.5 design
- New trigger and DAQ systems to handle increasing data in harsh radiation environment
  - ✓ Able to handle 750 kHz of L1-trigger rate with a latency of 12.5 μs

Upgrade of the CSC System

- Motivated by upgrade of the LHC:
  - ✓ Buffer overflows in CFEBs in forward region cause large inefficiencies
  - ✓ Memory limitations in ALCT FPGAs
  - ✓ Insufficient bandwidth in DMBs
  - ✓ Certain components not radiation-tolerant



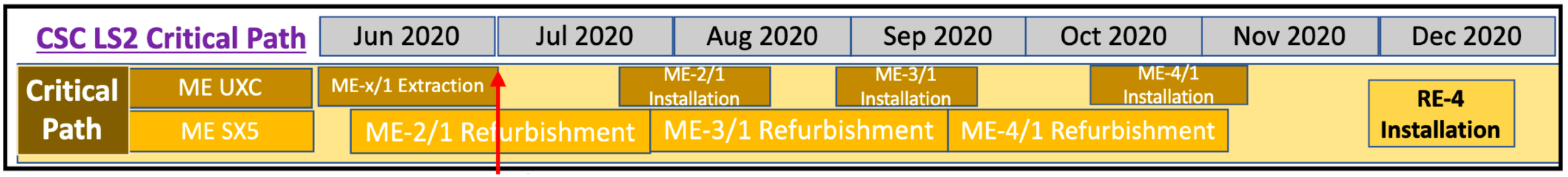
100% DCFEB loss in ME2/1 without upgrade

- CSC detectors will be upgraded during LS2 and LS3 to maintain excellent muon detection capabilities for CMS physics
  - ✓ Nearly 1400 new electronics boards
  - ✓ Trigger data will be sent from GEMs to CSCs via optical links
  - ✓ Environmentally friendly gas mixture

Upgrade timeline

- LS2 (2019-2021): necessary on-detector refurbishments
  - ✓ On-chamber electronics (DCFEB, ALCT, LVDB)
  - ✓ Trigger Motherboard (OTMB), Services (LV, HV), GEM-CSC link
- LS3 (2024-2027): only access to peripheral racks needed
  - ✓ Data Motherboard (ODMB), backend boards (ATCA)

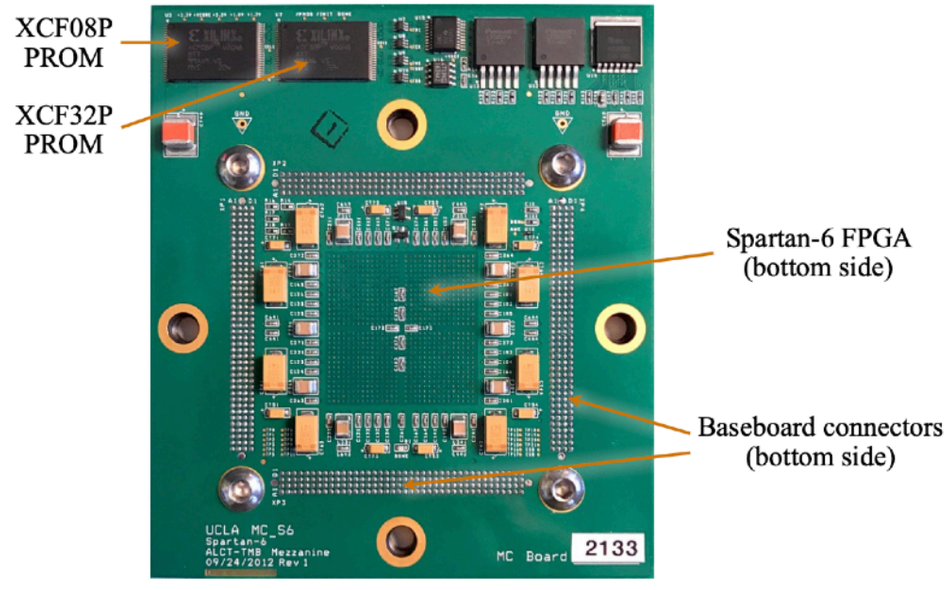
- Four work-streams spanning 2019-2020 during LS2



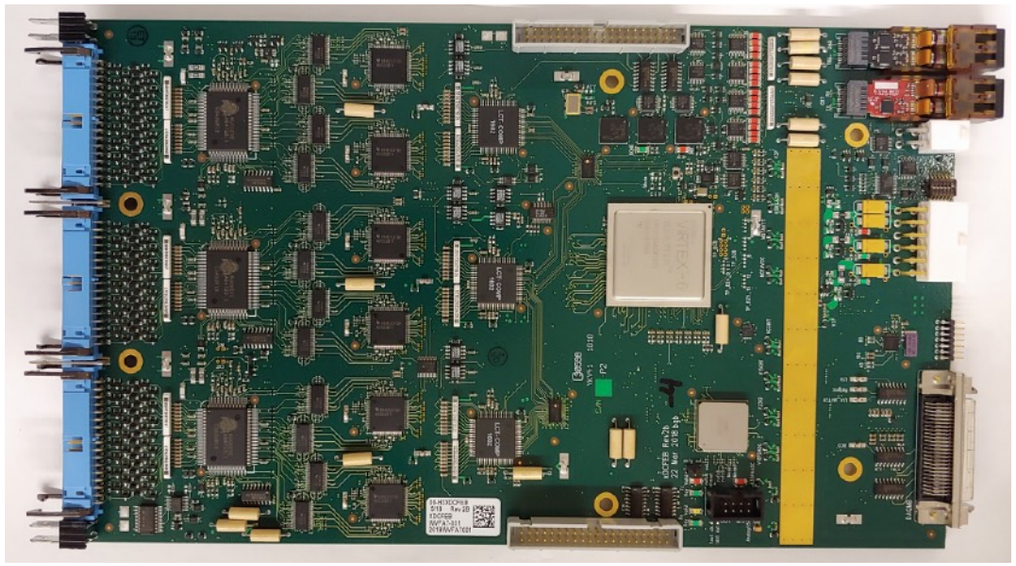
Post COVID-19 schedule for second half 2020

LS2 Electronics Upgrade

- **Anode Local Charged Track board (ALCT)**
  - ✓ Current Virtex-E ALCTs do not have sufficient FPGA memory resources and output bandwidth
  - ✓ Replaced with Spartan-6: 9-12x memory, 3-5 more logic, 2x faster
- **Cathode Front End Board (CFEB)**
  - ✓ Original ME1/1 DCFEBs to be replaced with the radiation-tolerant xDCFEBs (~30 kRad = 3x HL-LHC)
  - ✓ ME2/1, ME3/1 and ME4/1 chambers will have CFEBs replaced with digital versions (ME1/1 DCFEB)
  - ✓ Larger buffers, fast 20 MHz flash ADCs, Virtex-6 FPGAs
- **Low Voltage Distribution Board (LVDB)**
  - ✓ New LVDBs for ME1/1 provide more current for new xDCFEBs
  - ✓ New LVDBs for ME2/1, ME3/1, ME4/1 provide power for DCFEBs



ALCT mezzanine board

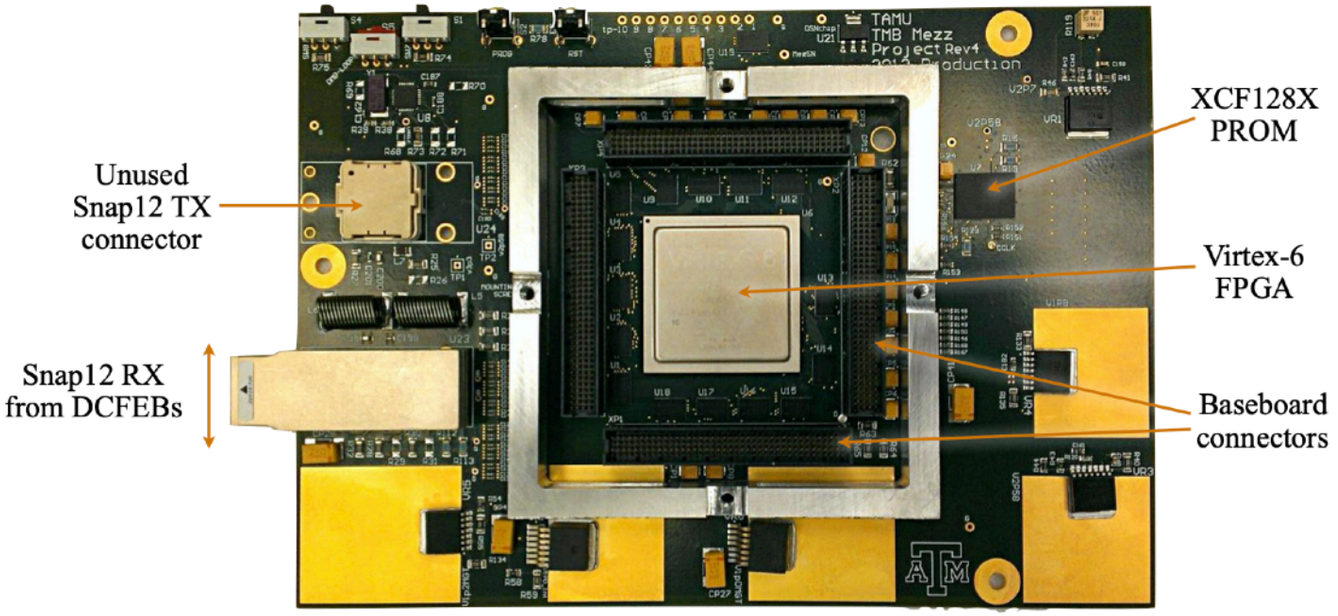


(x)DCFEB

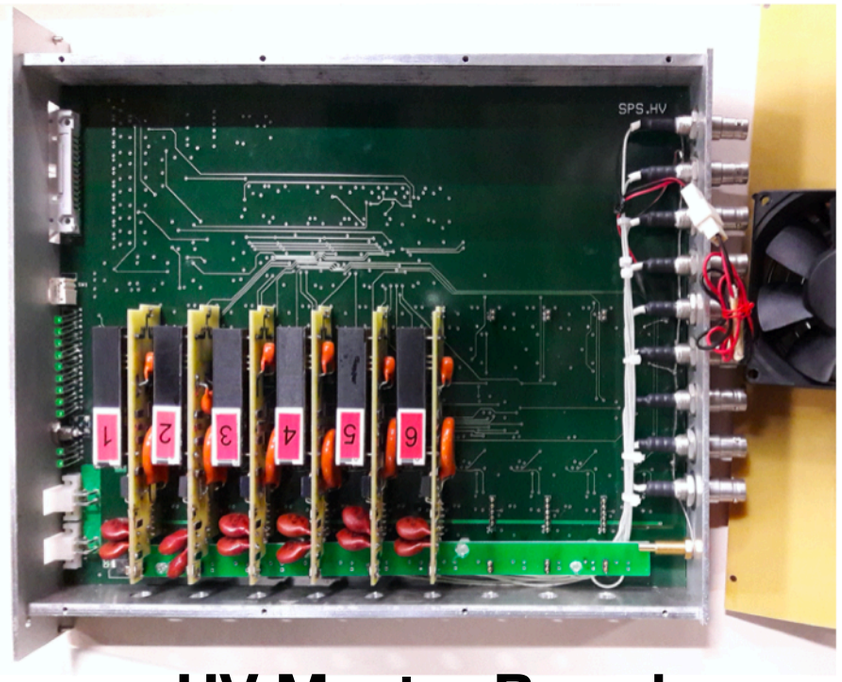
LS2 Electronics Upgrade

- **Trigger Motherboard (TMB)**
  - ✓ ME1/1 OTMBs will be replaced with faster optical versions and will be connected to GE1/1 boards
  - ✓ ME2/1, ME3/1 and ME4/1 will be instrumented with faster optical versions (old ME1/1 OTMB) based on Virtex-6 FPGAs

- New HV 9-channel Master boards
  - ✓ Original CAEN HV system for ME1/1 has already been absorbed in new HV system



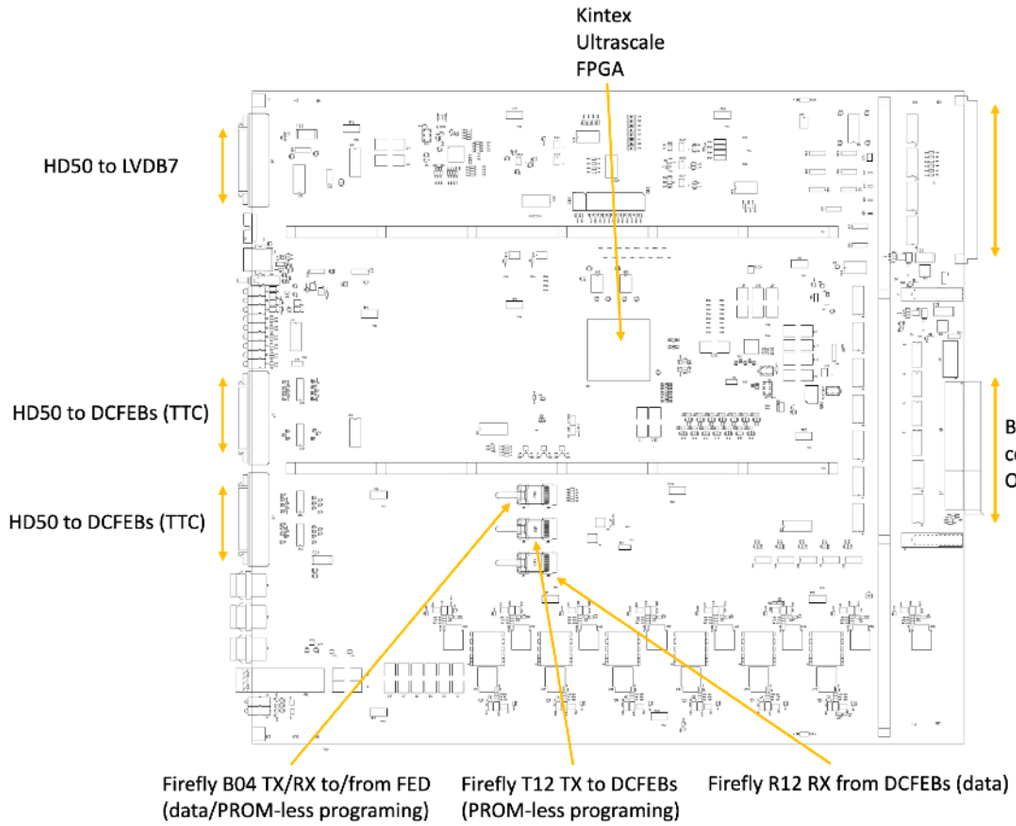
ME1/1 OTMB mezzanine



HV Master Board

LS3 Electronics Upgrade

- **Data Motherboards (DMB) to be replaced with optical data motherboards (ODMB)**
  - ✓ Upgrade of ME1/1 ODMBs to “ODMB7"
  - ✓ Upgrade of ME2/1, ME3/1, ME4/1 DMBs to “ODMB5”
  - ✓ Both boards based on Xilinx Kintex Ultrascale FPGA
  - ✓ Output bandwidths are up to 30 Gb/s.

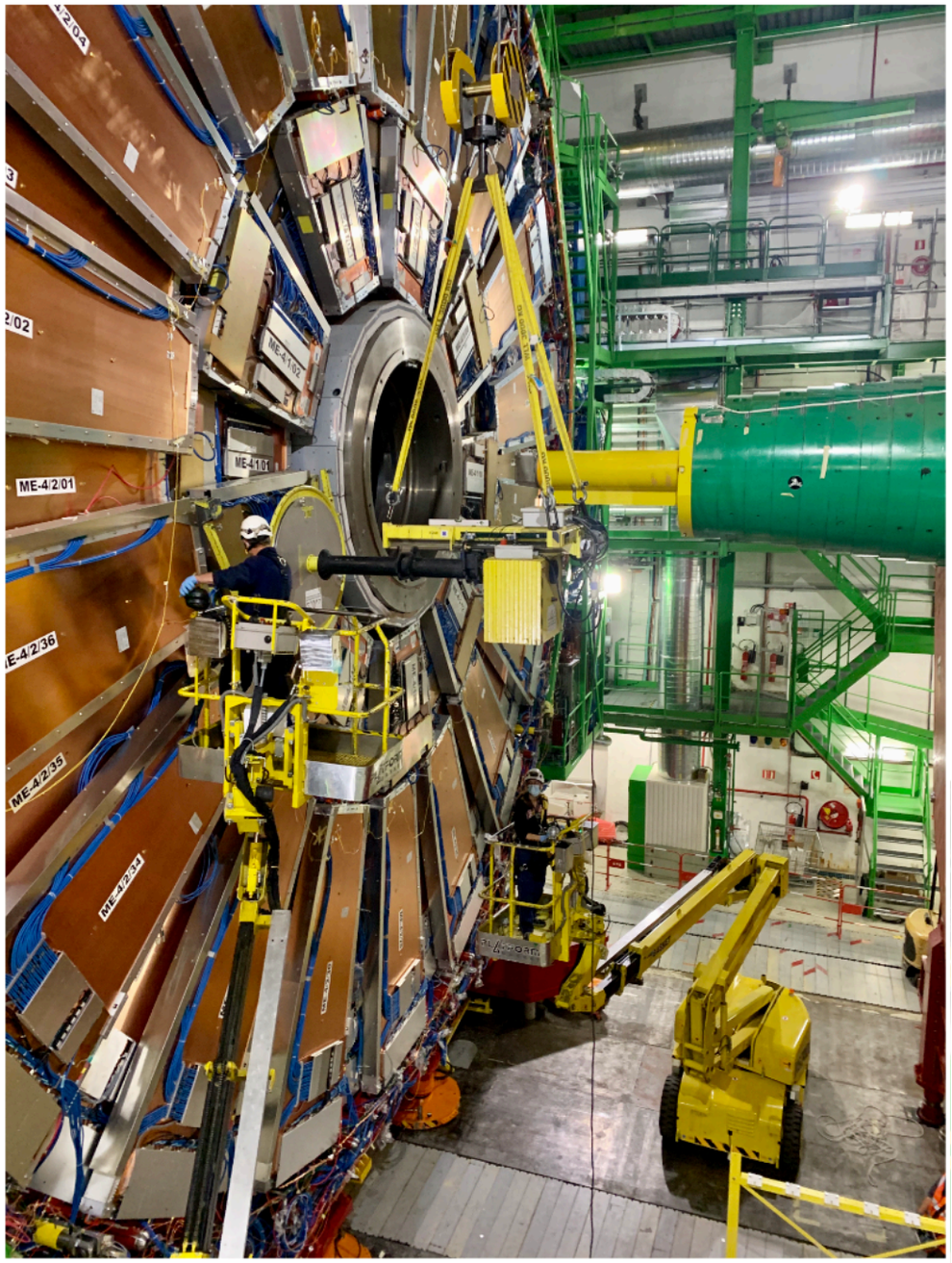


ME1/1 ODMB7

- **CSC Front-End Driver (FED)**
  - ✓ New ATCA-based boards will deliver a total of up to 598 Gb/s of data to CSC DAQ

Electronics Refurbishment

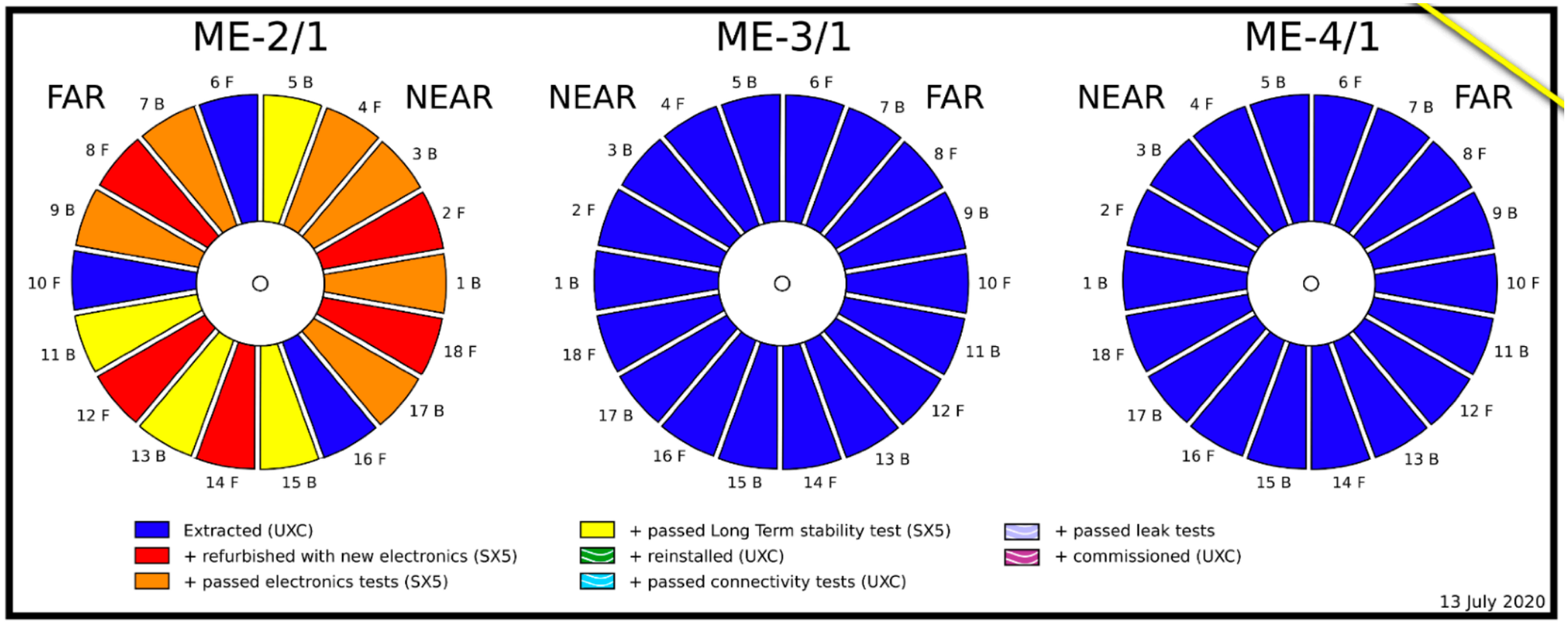
- Chambers are extracted from the cavern to CSC lab at SX5 (surface)



- On-chamber electronics boards are replaced and tested in CSC lab at SX5
- Crew of ~20 people involved in refurbishment

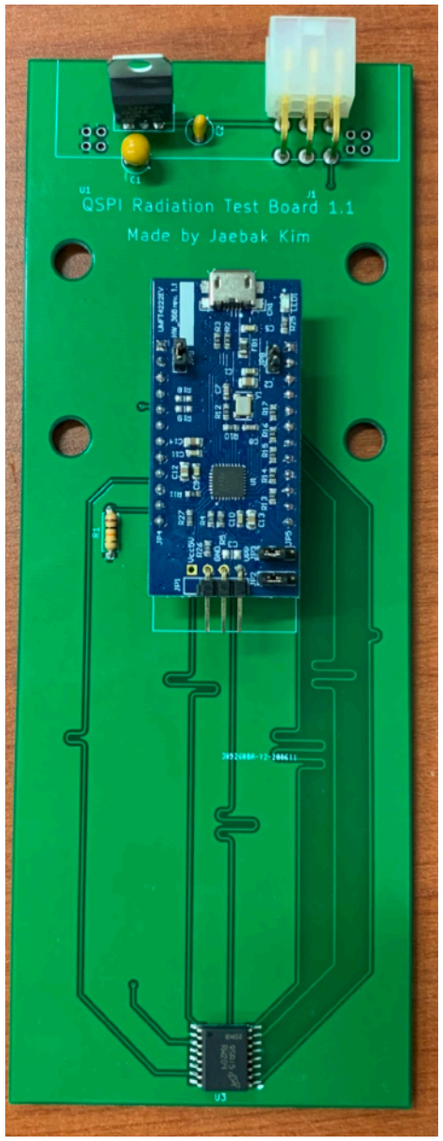
Status of Phase-2 Installation

- Work streams 1-3 fully completed before COVID19; 4th work stream (ME-X/1 refurbishment) was just about to begin
- CERN shutdown from March 18th to June 2nd
- CERN starting back up again: ME-X/1 refurbishment will be shifted by 2.5 month and extended by 2 months
- ME-2/1 reinstallation started July 21



Irradiation longevity studies

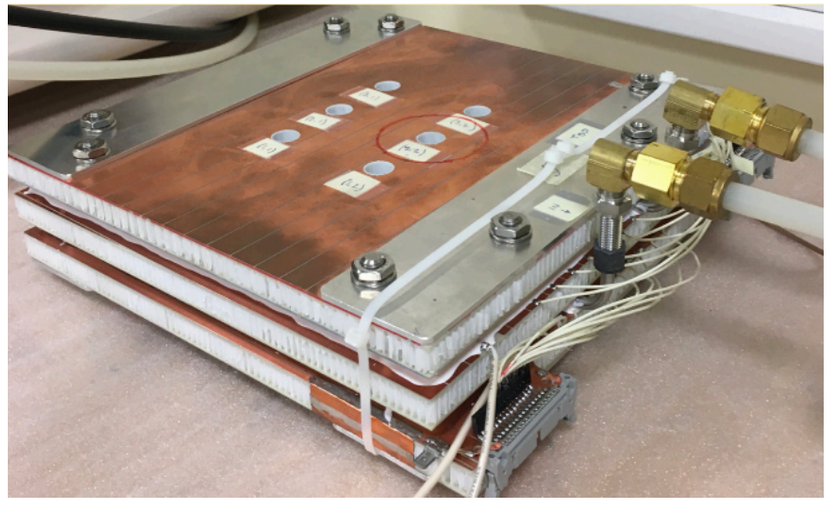
- HL-LHC will expose CSC electronic components to intense radiation, in particular on-board electronics in inner-ring chambers
- Need radiation-tolerant optical transceivers, memory units,…
- New components being tested at
  - ✓ CHARM, CERN (mixed hadron spectrum)
  - ✓ Texas A&M University cyclotron (protons)
  - ✓ Texas A&M University reactor (neutrons and photons)
  - ✓ UC Davis cyclotron (protons)
- Each component receives dose up to 30 kRad (3 x HL-LHC)
  - ✓ Count single-event upsets (bit-flips caused by ionizing particles) and electronics dead-time in during beam exposure
- Example of test in June 2020: prototype EPROM board for inner-chamber ODMBs



Radiation test board for the ODMB EPROM tested at TAMU cyclotron

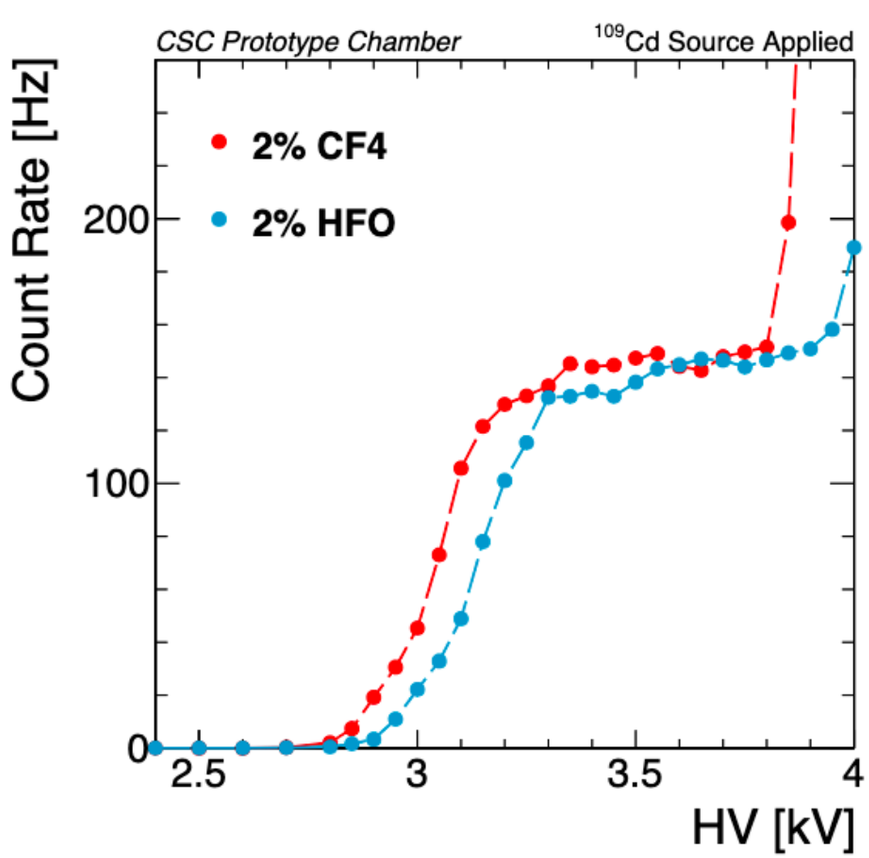
Gas mixture studies

- Gas mixture: 40% Ar + 50% CO_2 + 10% CF_4
  - ✓ Ar: provides gas gain of electronic avalanche in HV
  - ✓ CO2： quenching of spurious pulses to enhance time response
  - ✓ CF4： anti-aging additive which prevents wire etching and polymerization
    - ◉ (GWP ~6500 for 100 year)



CSC prototype at CERN: 30 x 30 cm2, 2 gas gaps, Standard CSC electronics and DAQ

- European regulations restrict usage of greenhouse gases including CF_4
- Alternative gas mixtures are being investigated at CERN using a prototype CSC
- Two-fold approach:
  - ✓ 1) Longevity properties of gases with less CF_4
  - ✓ 2) Performance studies with more eco-friendly gases
    - ◉ HFO-1234ze (GWP < 1 for 100 year)



Summary

- The CSC system will be upgraded for the HL-LHC during LS2 and LS3
- Extensive upgrade program with new electronics, new algorithms, interface with GEM system, and usage of new gas mixture
- LS2 operation currently ongoing. Three work-streams fully completed.
- Shift and extension of operations due to COVID-19 crisis
- CERN is opening up again; fourth work-stream (ME-X/1) has started
- Irradiation studies and alternative gas mixture studies ongoing

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