Development of the CMS MTD Endcap Timing Layer for the HL-LHC

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CMS MIP Timing Detector group
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Overview

Motivation for precision timing at the HL-LHC

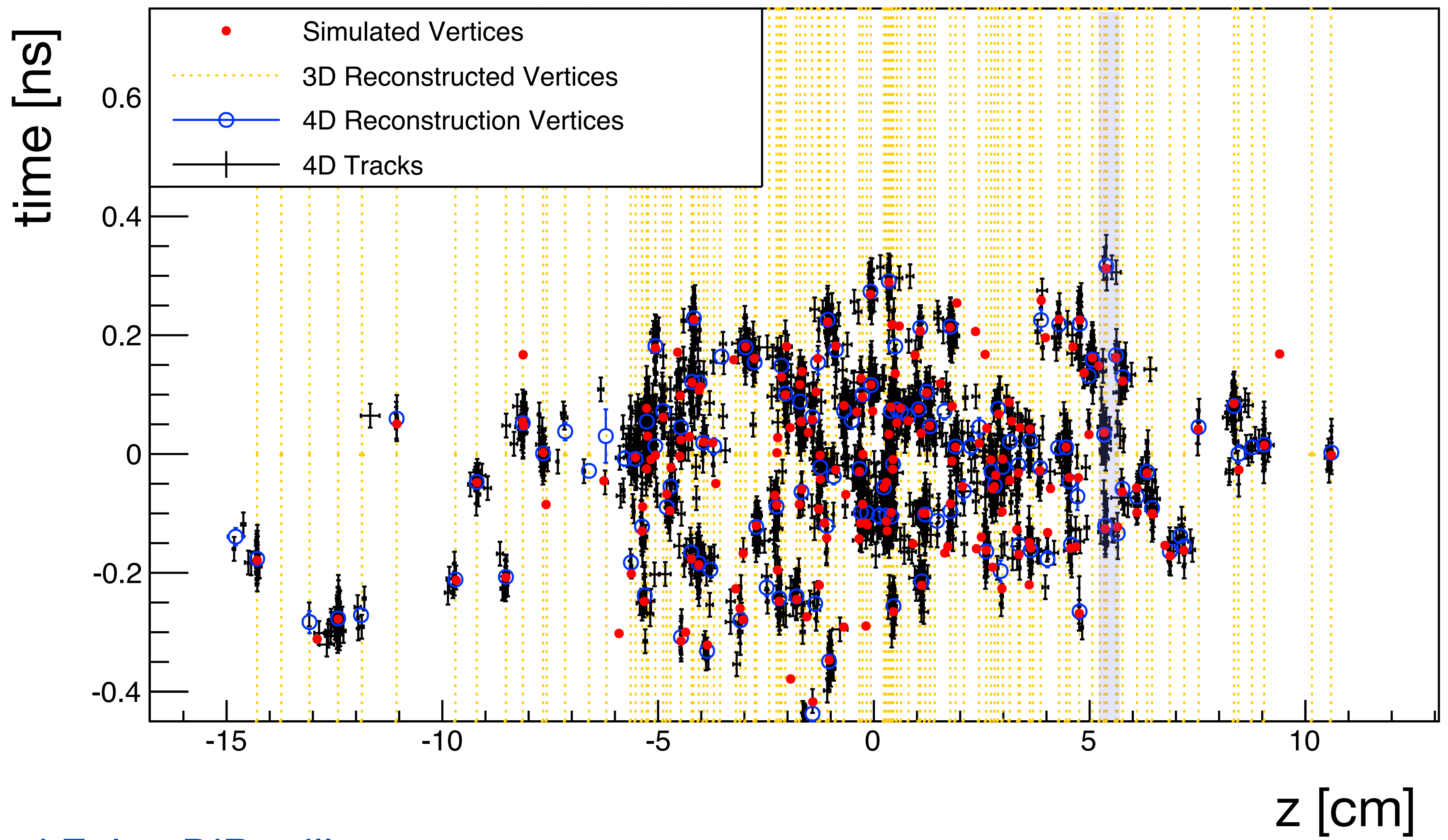
CMS Endcap Timing Layer design

Recent test beam results

Motivation for precision timing

Timing disentangles pile-up interactions

- average pile-up in Run 2: 50-60 pp-collisions per bunch crossing
- increases to 140-200 at the High Luminosity LHC
- expect even more pile-up at future colliders, eg. FCC-hh ~1000



200 PU
~30 ps time resolution

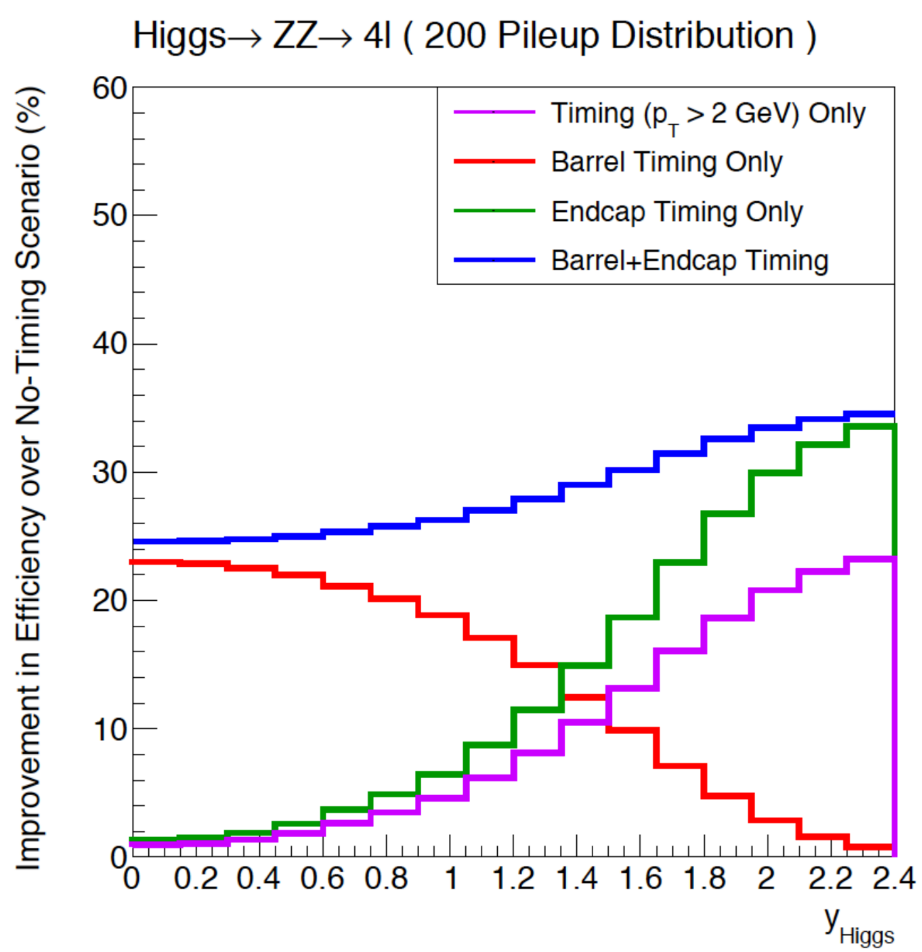
luminous region
RMS time: 150 ps
RMS z: 4.8 cm

vertices merged in z can be separated with timing

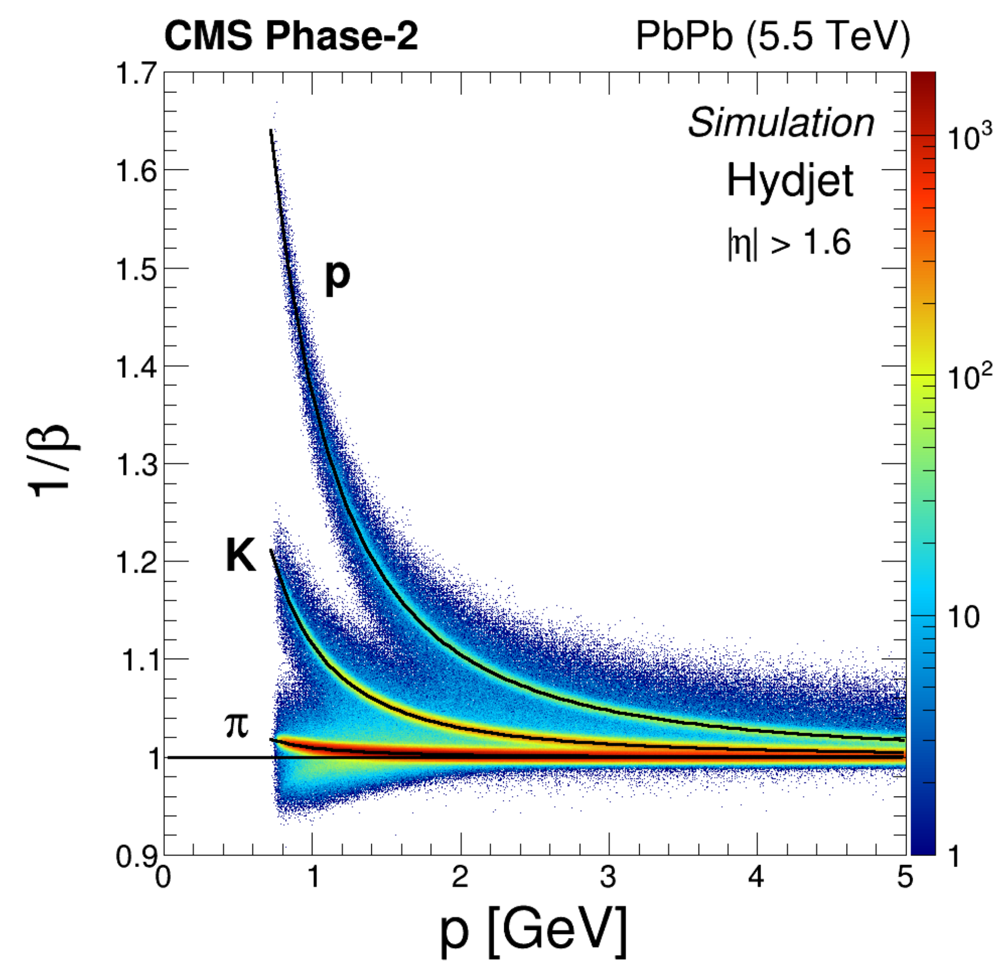
Impact on physics

~30 ps precision timing

- improves/maintains nearly every area of physics performance
- new potential for particle ID and long-lived particle searches



26% increase in effective luminosity for H→ZZ→4l



proton ID up to ~5 GeV
kaon ID up to ~3 GeV

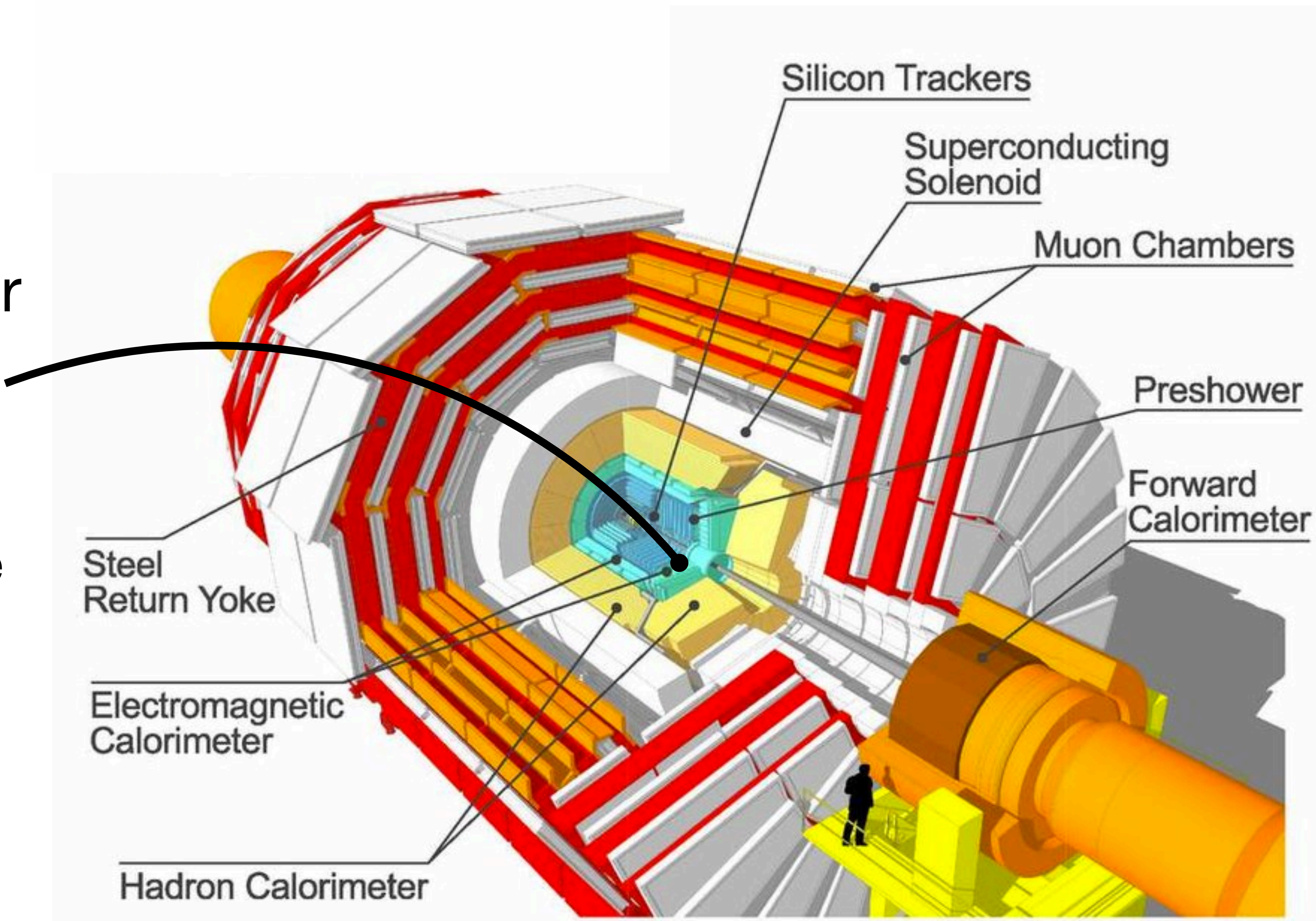
MIP Timing Detector

Provides 30-50 ps time stamp for every charged particle

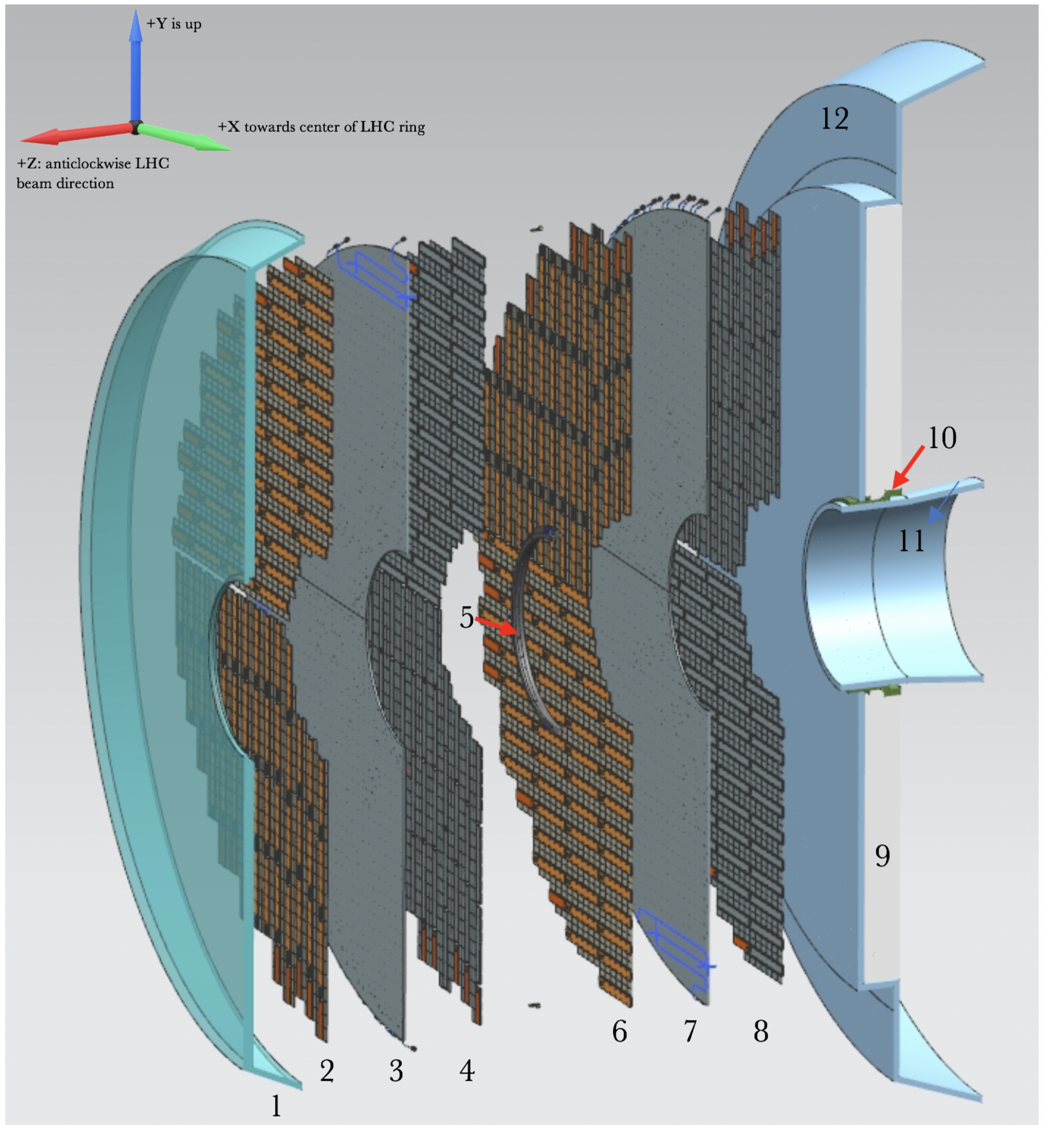
Located between Calorimeter and Tracker

Endcap Timing Layer (ETL)

- up to 10x higher radiation than Barrel
- Low Gain Avalanche Detectors (LGADs)



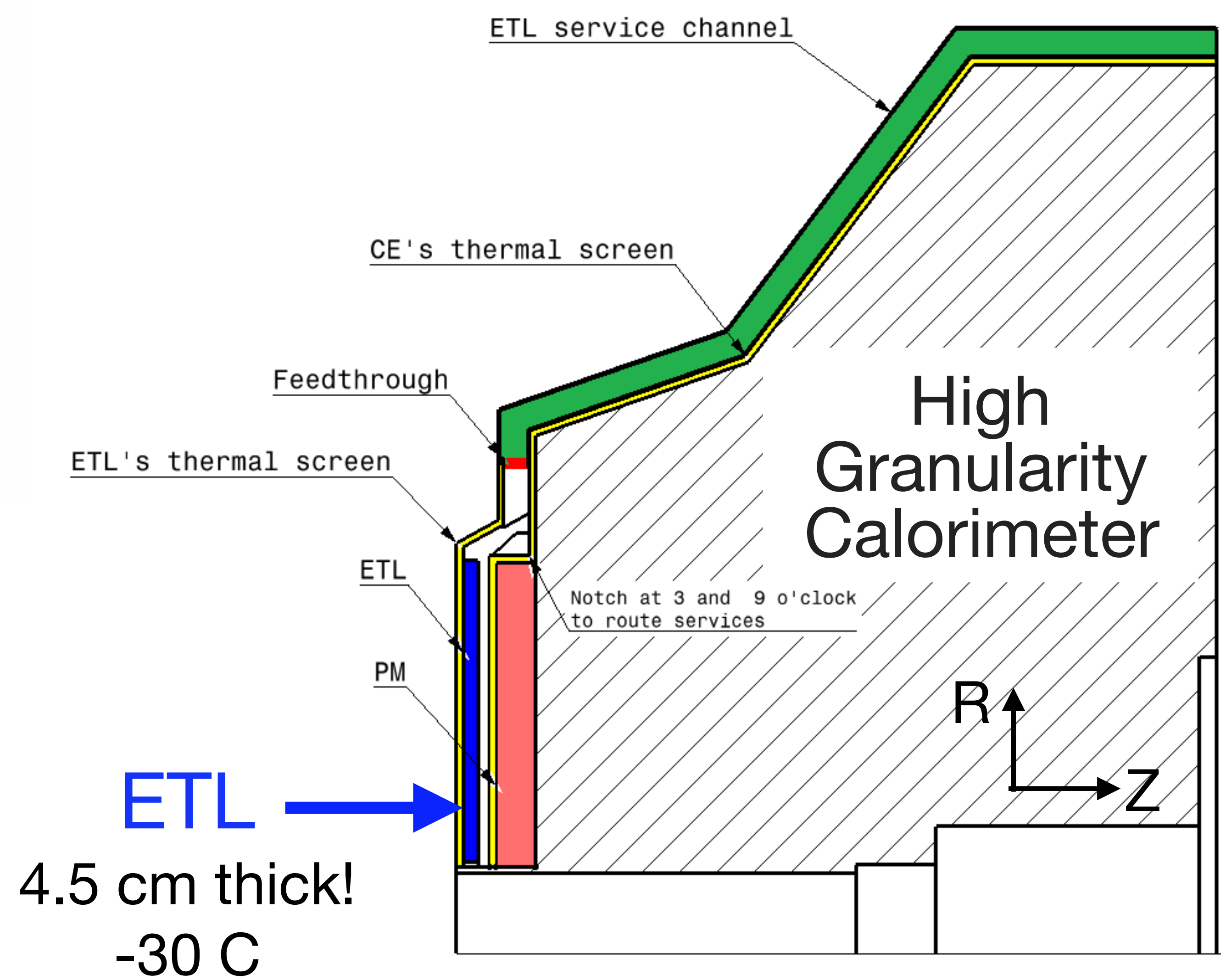
Endcap Timing Layer design



1: ETL Thermal Screen
2: Disk 1, Face 1
3: Disk 1 Support Plate
4: Disk 1, Face 2
5: ETL Mounting Bracket
6: Disk 2, Face 1
7: Disk 2 Support Plate
8: Disk 2, Face 2
9: HGCal Neutron Moderator
10: ETL Support Cone
11: Support cone insulation
12: HGCal Thermal Screen

2 double sided disks
1.8 hits per track
50 ps per hit → 35 ps per track
Number of channels 8.6 x 10^6
Active Area 16 m^2

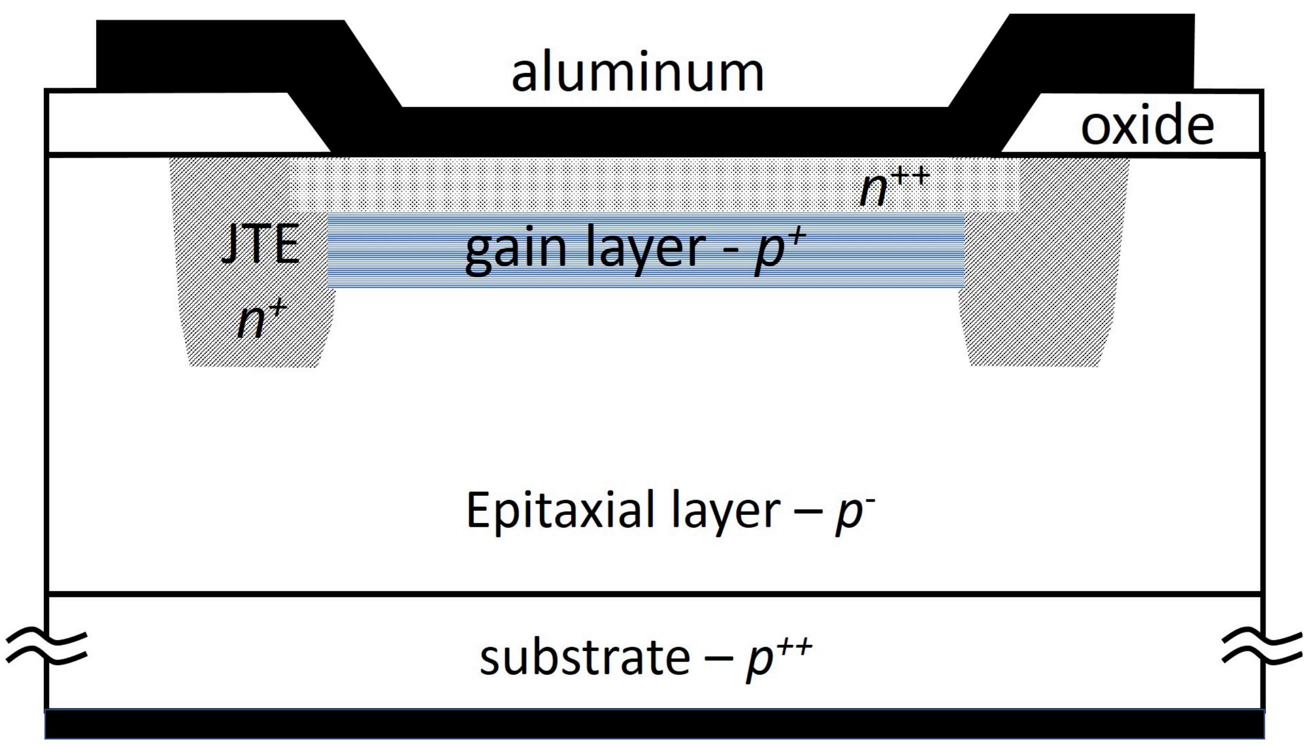
coverage:
$1.6 < \eta < 3.0$
$0.31 < R < 1.2$ m
Z = 3 m from pp-interaction

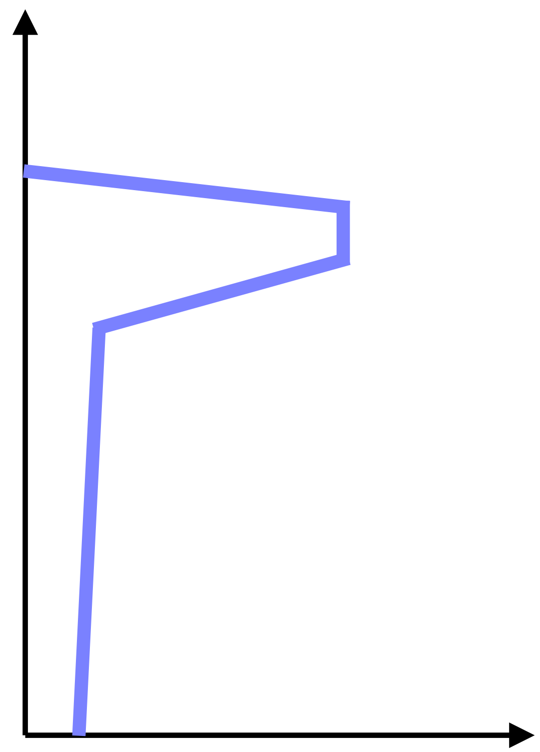


Low Gain Avalanche Detectors

Ultra-fast silicon detectors with a highly doped p+ gain layer

Moderate internal gain : 10-30





LGAD design choices

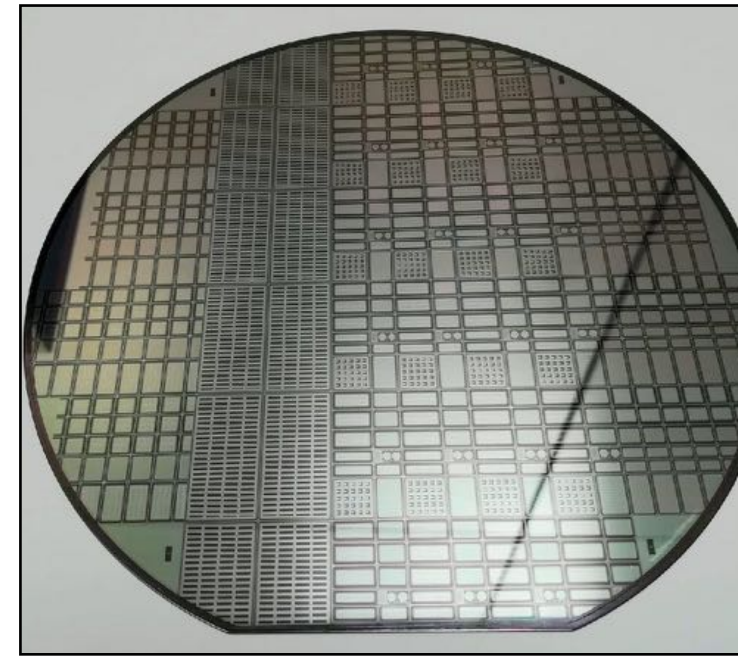
Key sensor characteristics

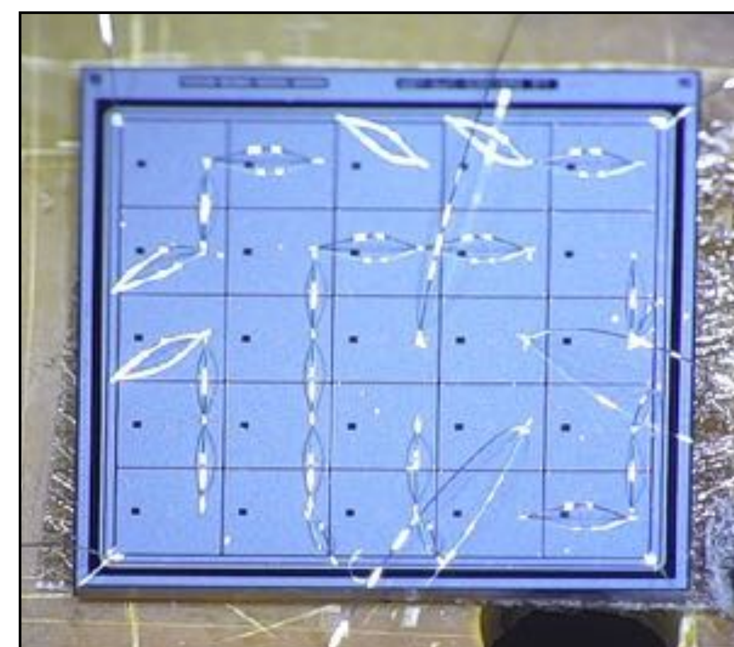
Depletion region thickness	50 µm	Minimize rise time, sufficient charge, gain uniformity
Pad size	1.3x1.3 mm^2	Minimize capacitance, Occupancy ~1%
Sensor size	2x4 cm^2 (16x32)	Optimize wafer usage
Interpad gap	< 90 µm	Fill factor > 85%
Time res. after irradiation	< 40 ps	up to $1.7 \cdot 10^{15}$ n_{eq}/cm^2

Recent prototypes from Hamamatsu (HPK), Fondazione Bruno Kessler (FBK) focus on

- improving radiation hardness
- increasing fill factor
- large arrays

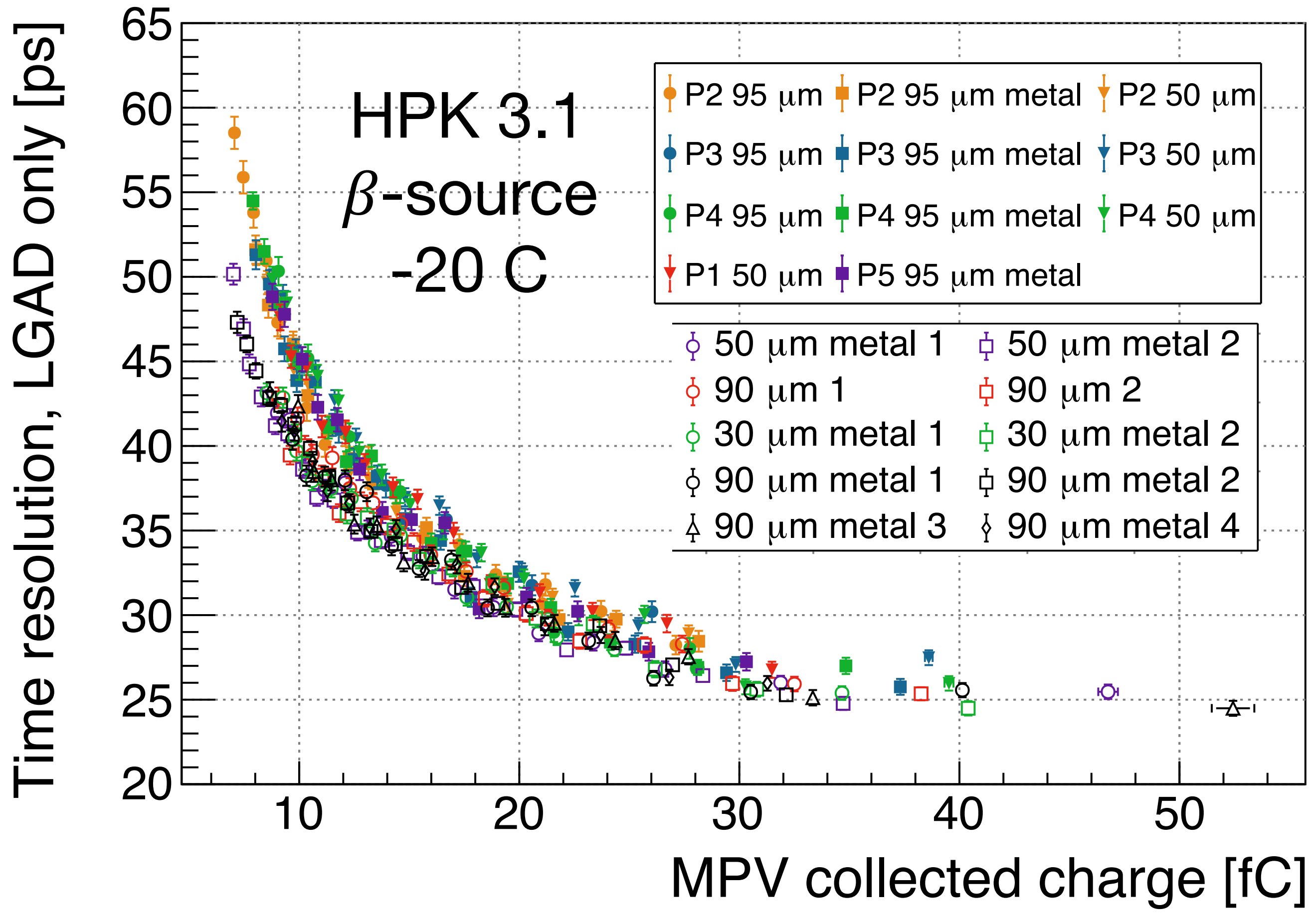
FBK UFSD3

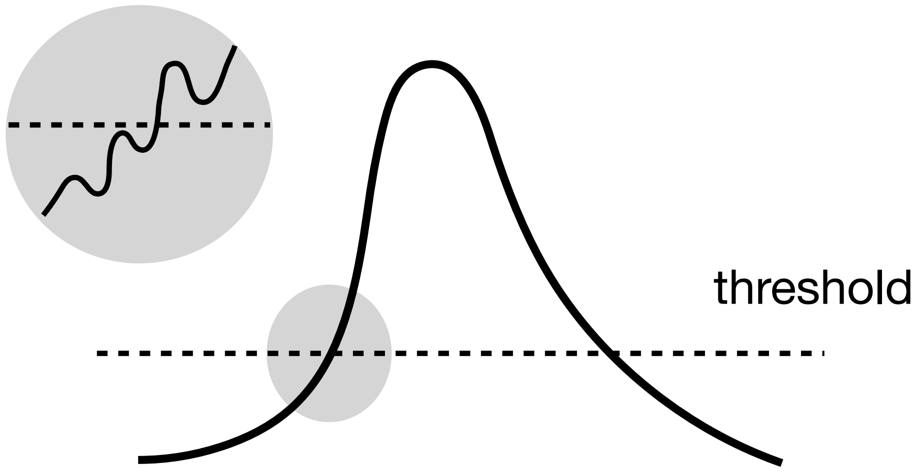




5x5 array from HPK

LGAD time resolution





$$\sigma_{\text{ioniz.}} \sim 30\text{ps}$$

fluctuations in Landau ionization for 50 μm thick LGAD dominates at high gain

$$\sigma_{\text{jitter}} \sim \frac{e_n C_{\text{d}}}{Q_{\text{in}}} \sqrt{t_{\text{rise}}}$$

jitter contribution subdominant at high gain

Front-end ASIC: ETROC

A delicate balancing act

Low noise & fast risetime

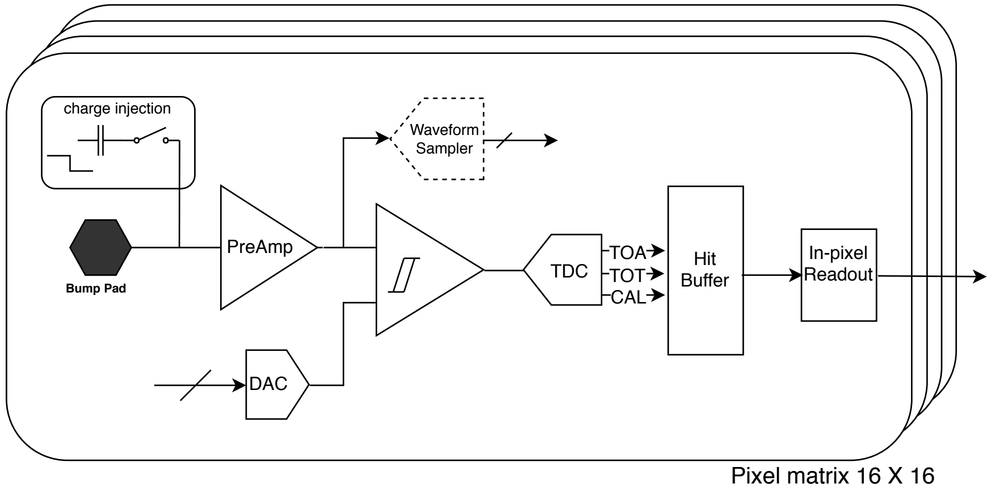
$$\sigma_{\text{jitter}} \sim \frac{e_n C_{\text{d}}}{Q_{\text{in}}} \sqrt{t_{\text{rise}}} < 40\text{ps}$$

Power Budget

1 W/chip, 4 mW/channel

ETROC innovations:

- Single TDC for both time of arrival and time over threshold
- Flexible low & high power amplifier modes

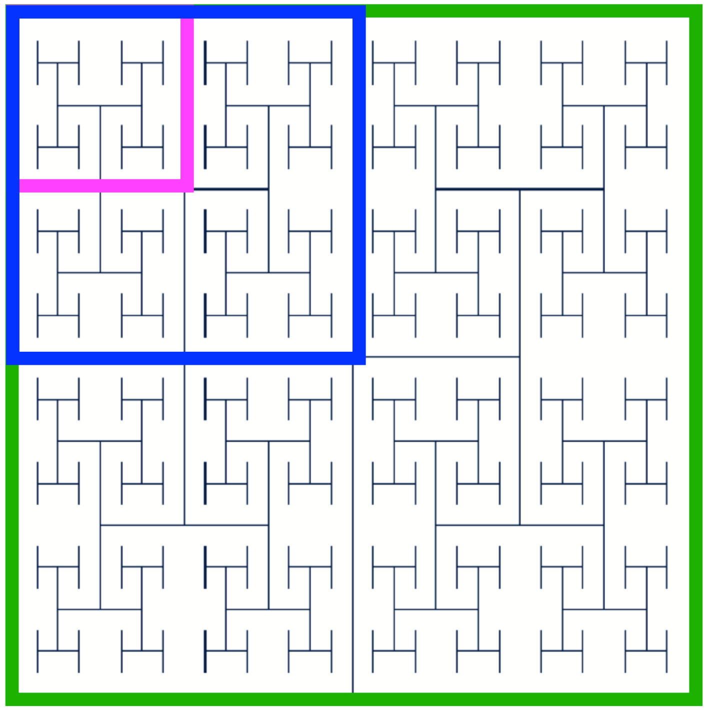


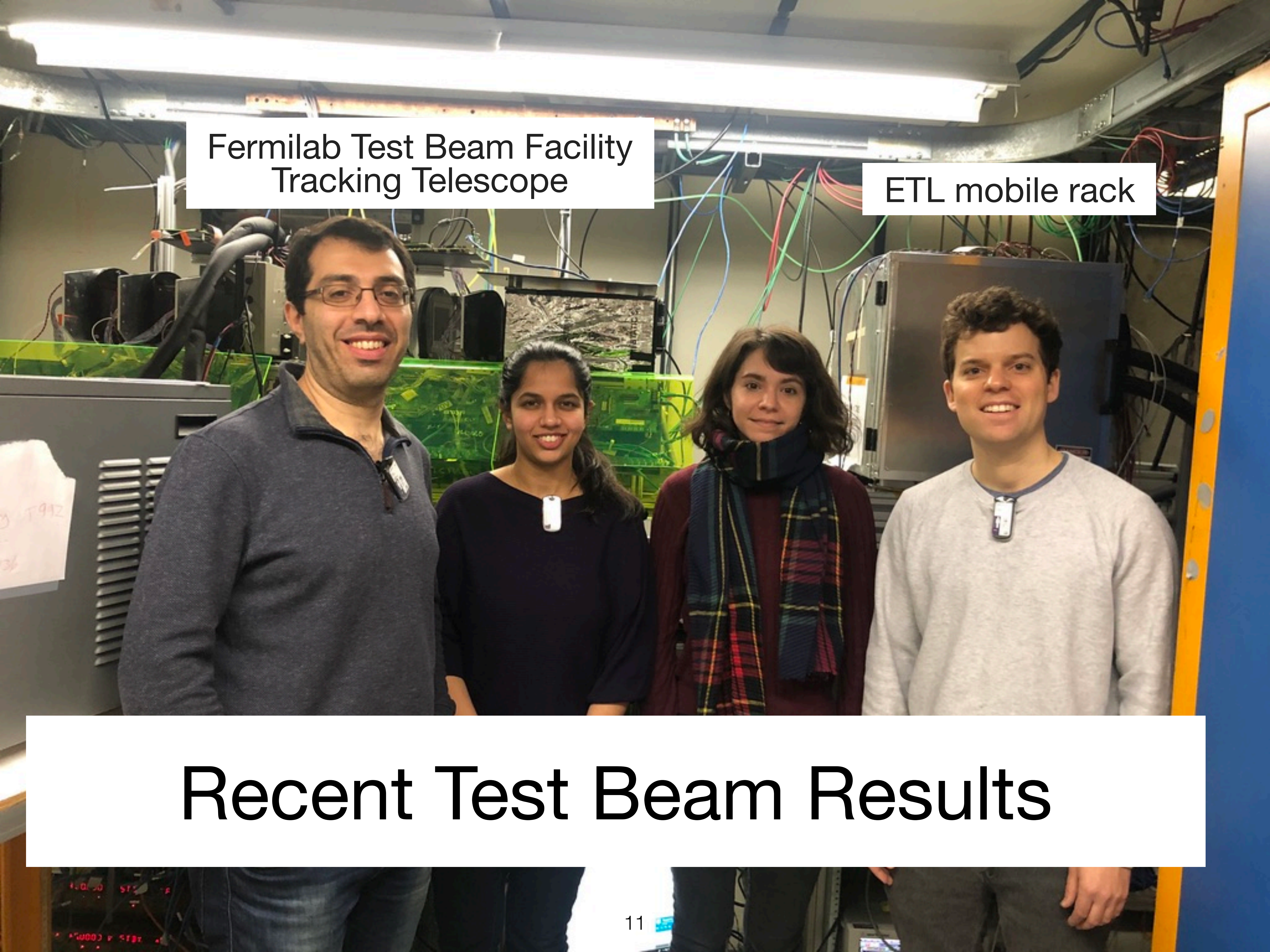
ETROC0 : single analog channel

ETROC1: with TDC and 4x4 clock tree

ETROC2: 8x8 full functionality

ETROC3: 16x16 full size chip

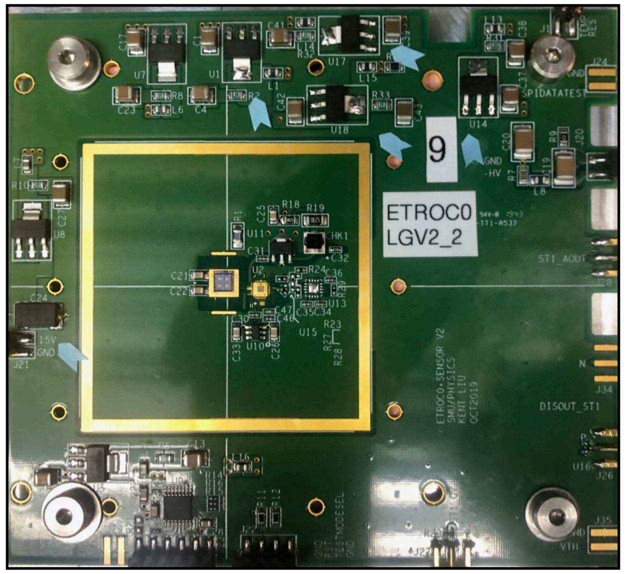




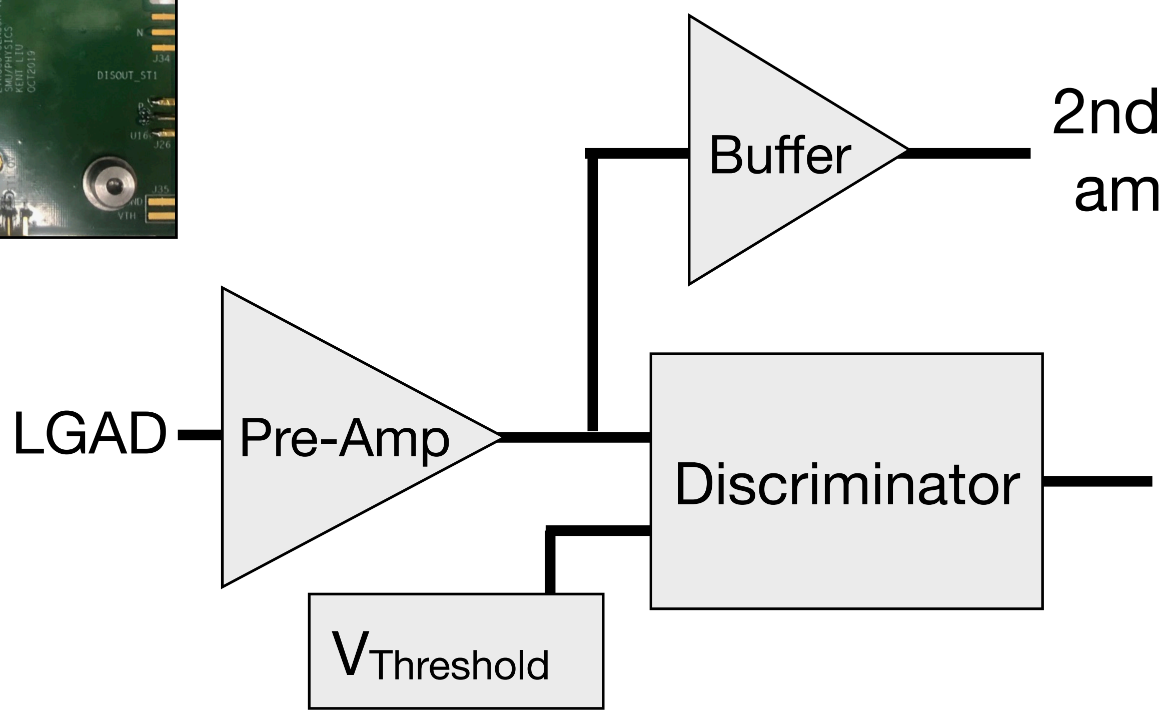
Recent Test Beam Results

ETROC0 with HPK 3.1 sensors

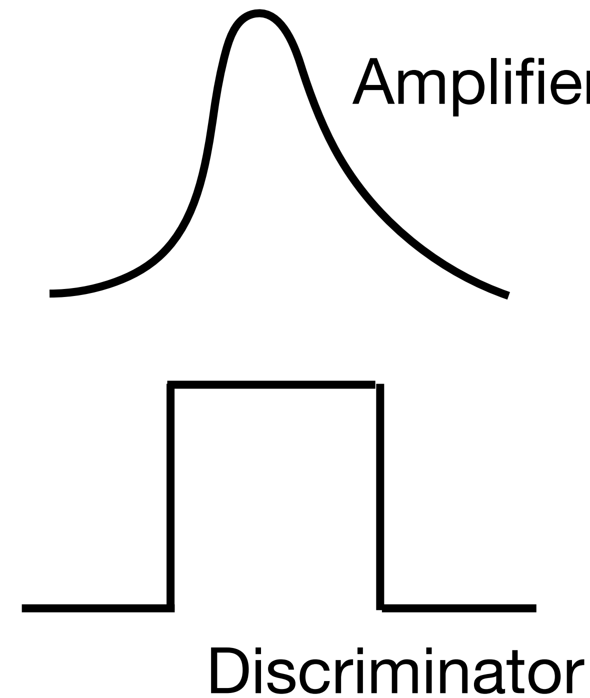
ETROC0 board



Simplified Concept



Two output paths



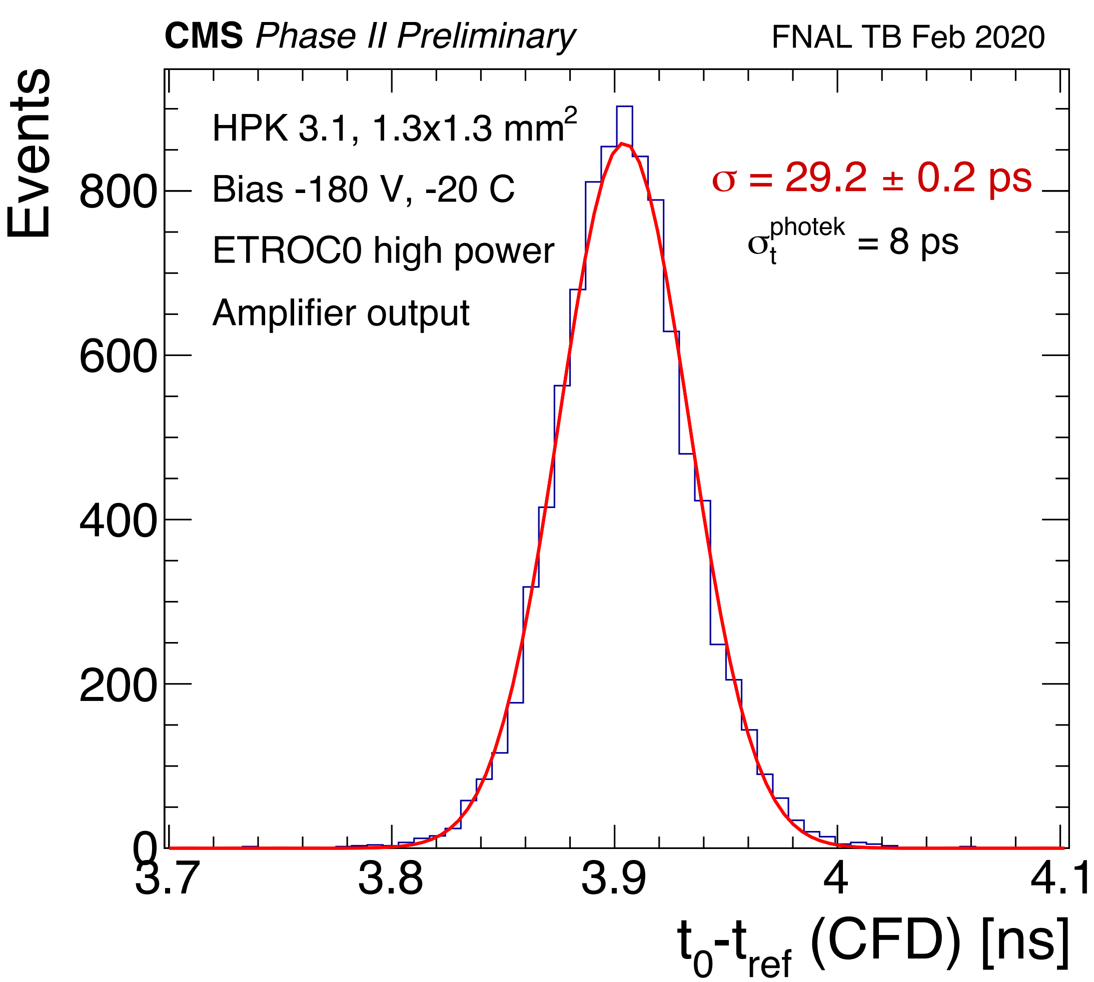
Two ETROC0 data paths used in beam tests

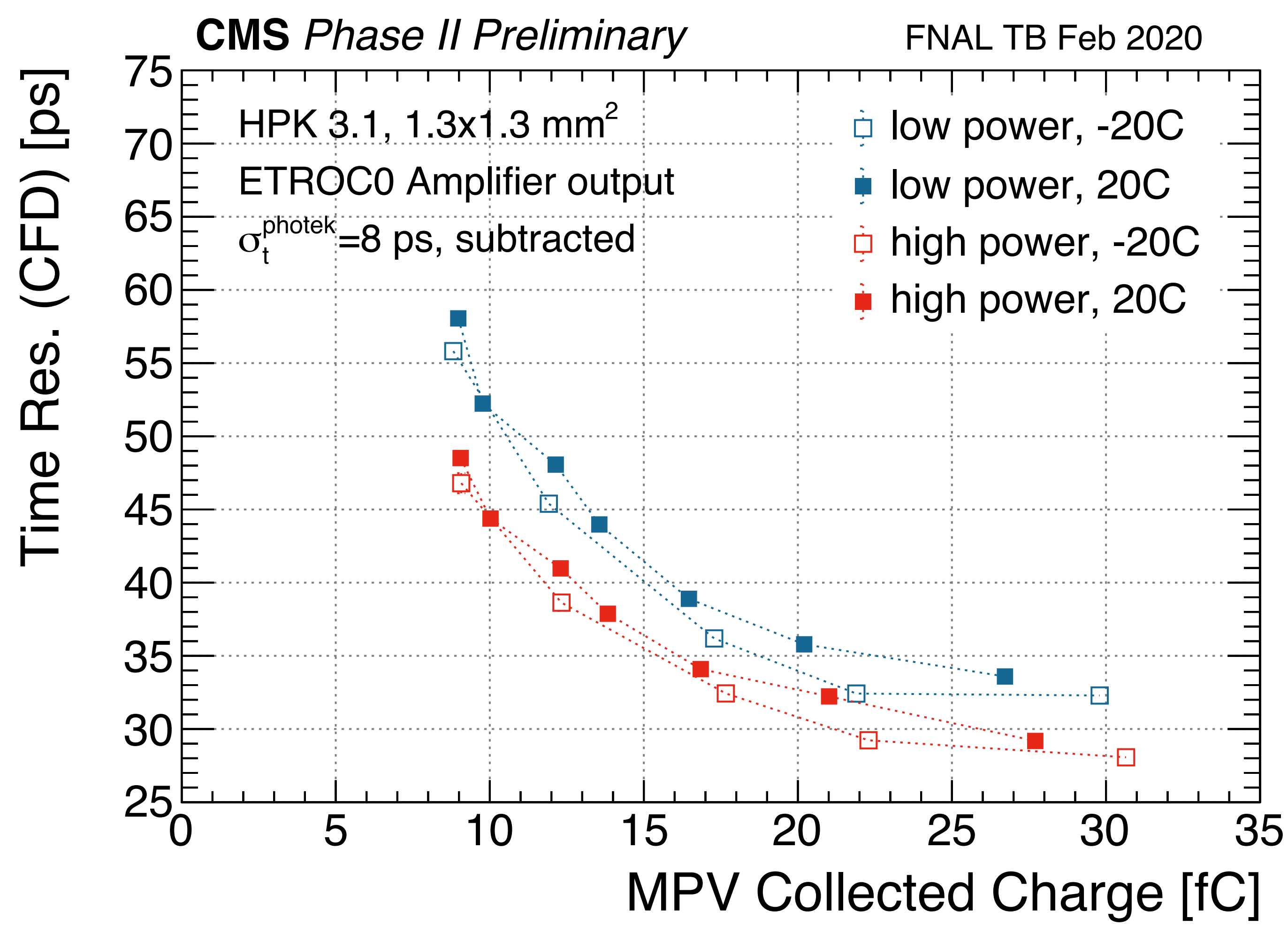
- “Amplifier output” recorded through internal buffer and external 2nd stage amplifier
- At “Discriminator output” study contributions to time resolution from sensor due to Landau fluctuations, and pre-amp & discriminator jitter, design goal $\sigma_t < 50$ ps

Amplifier: Time resolution

Achieved 30-35 ps time resolution for
pre-rad sensors operating above 20 fC!

high power mode 5-10% better time resolution than low power



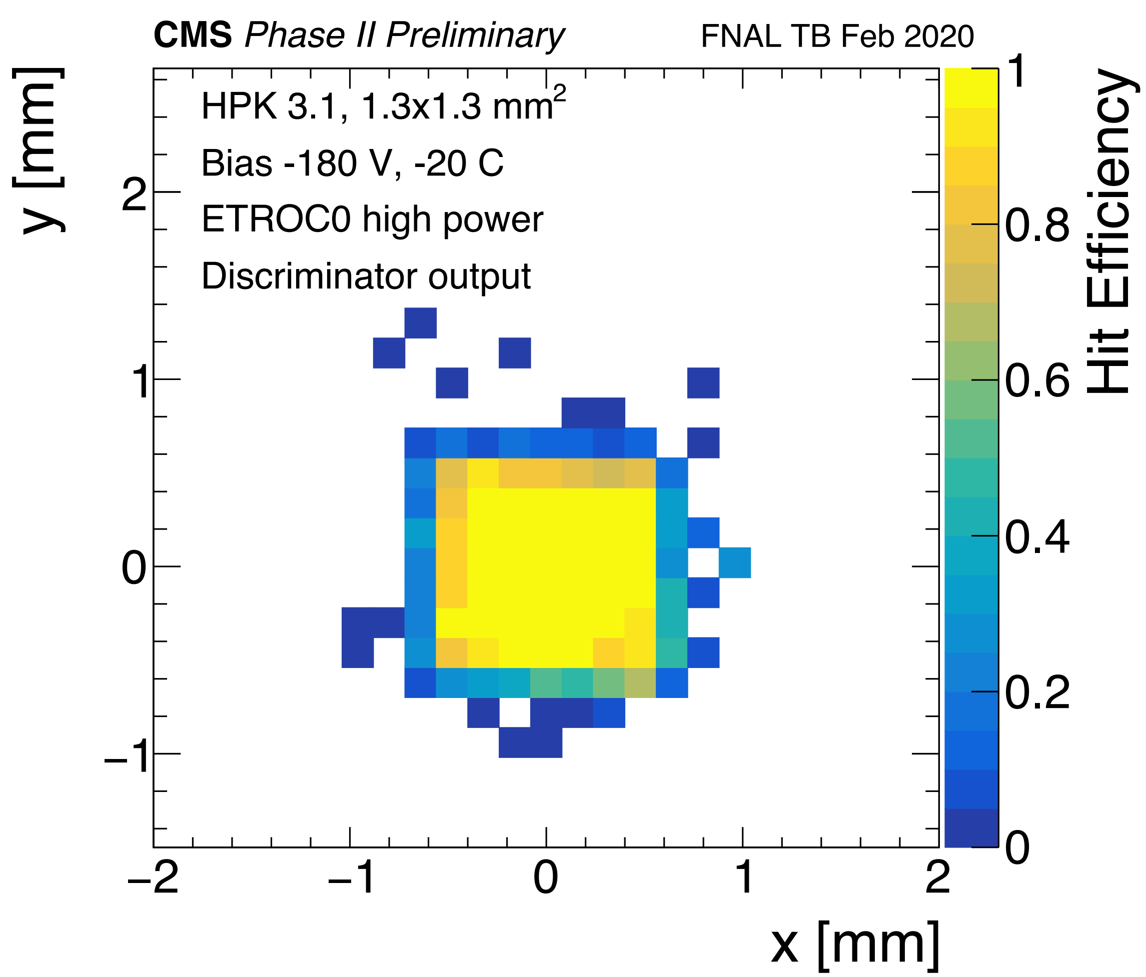


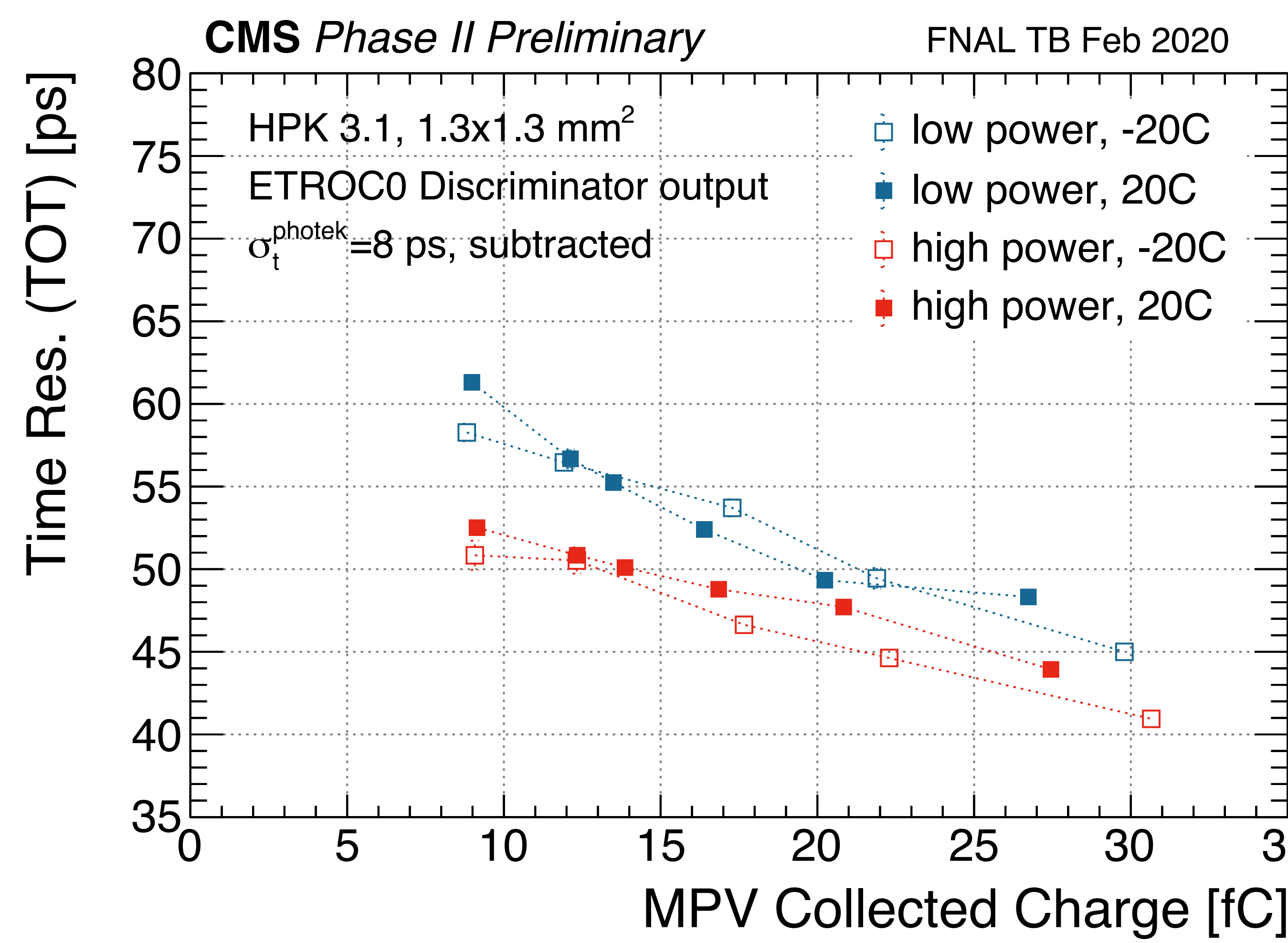
timestamp measured w/ constant fraction threshold of 20%
right plot has time reference contribution subtracted

Discriminator: Time Resolution

For pre-rad sensors operating above 20 fC, we obtain time resolution of 40-50 ps with 100% efficiency!

A great first result! Compatible with design target of 50 ps per hit





time resolution = $\sigma(t_0 - t_{ref}$ after ToT correction)
contribution from time reference is subtracted

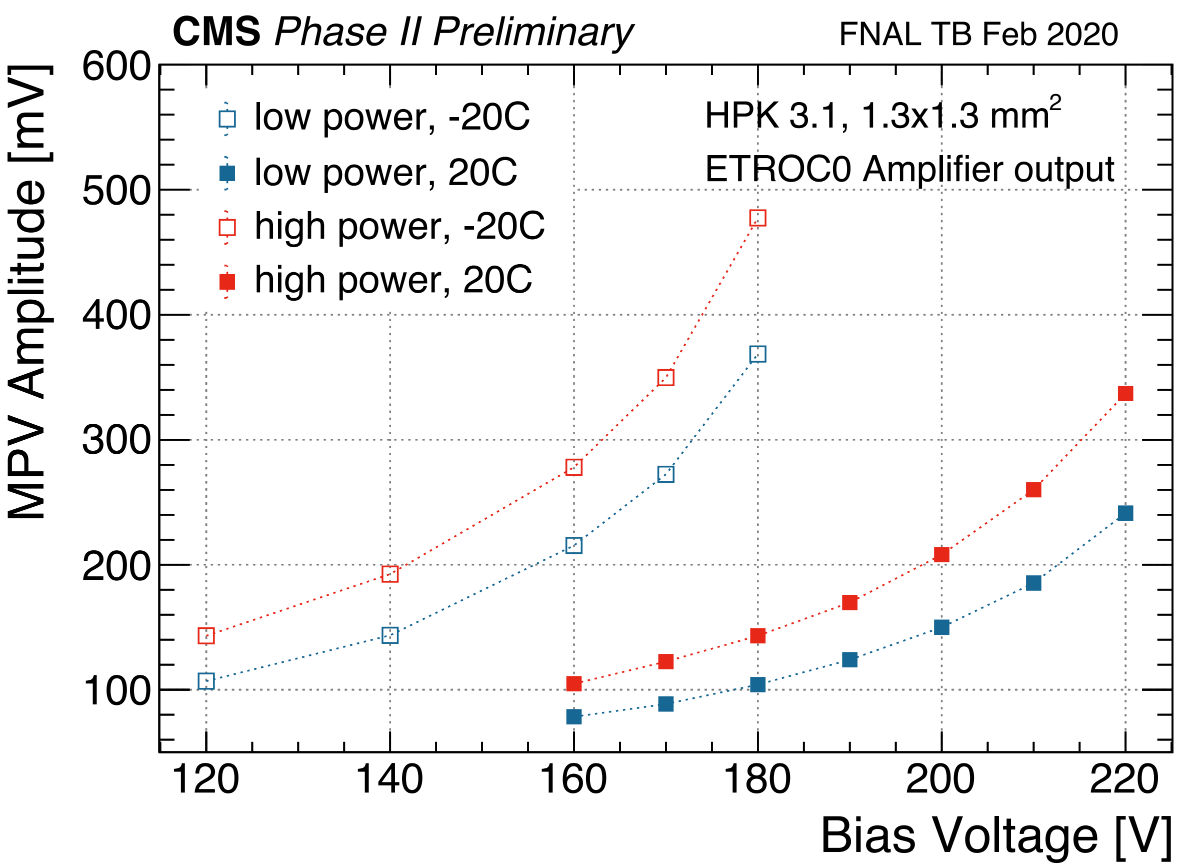
Conclusions

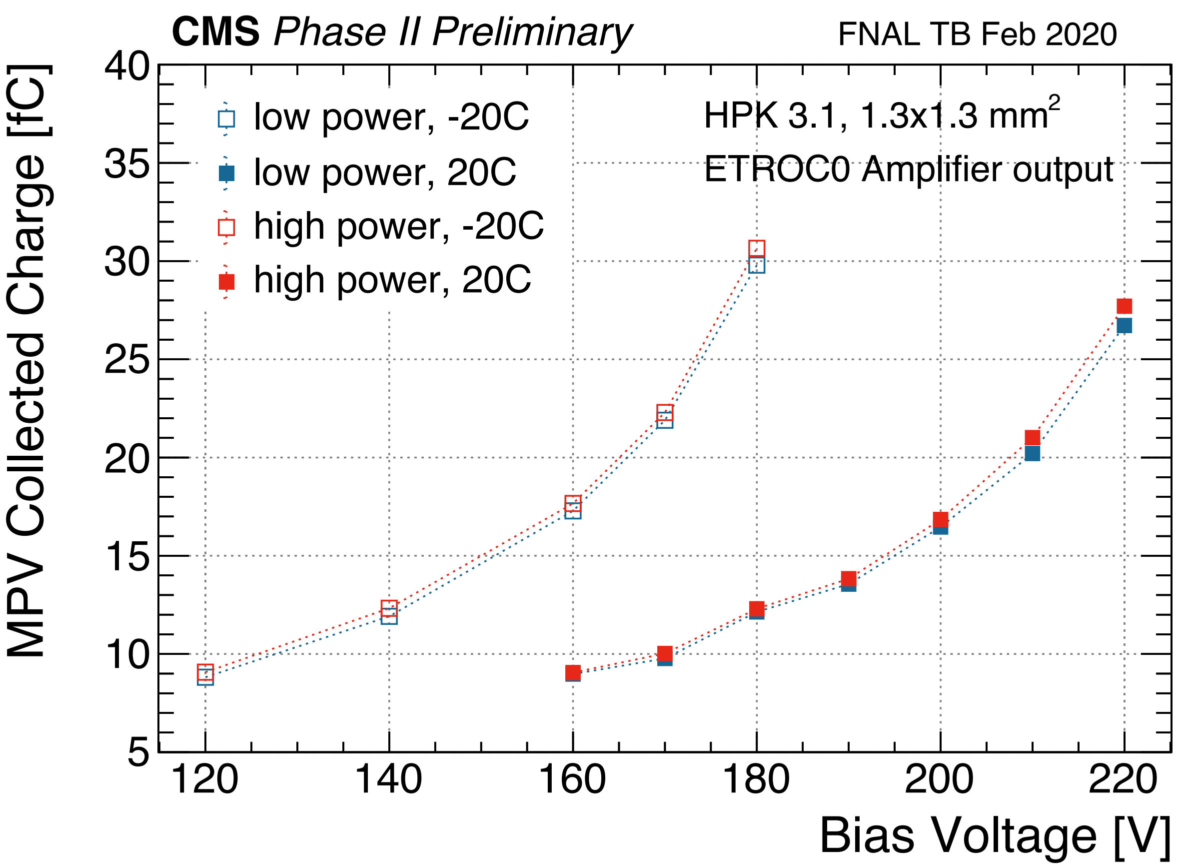
- HL-LHC high pile-up environment motivates 30-50 ps precision timing layer
- Presented Endcap Timing Layer detector design, and R&D motivated design choices
- Presented new results from Feb 2020 test beam
  - first beam tests of prototype sensors and front-end ASIC
  - achieved 30-35 ps time resolution with amplifier output and 40-50 ps with discriminator
  - excellent first results - within specs for final detector!

Backup

Amplifier performance

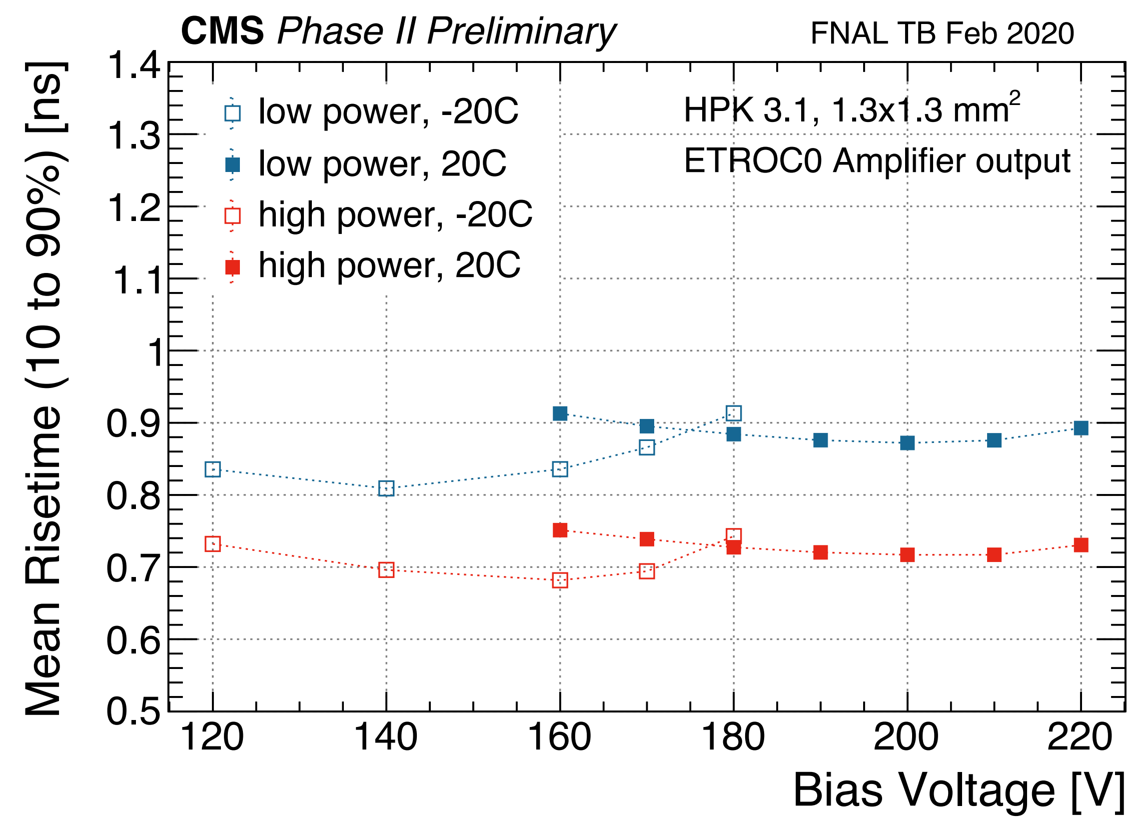
max amplitude and charge versus bias voltage

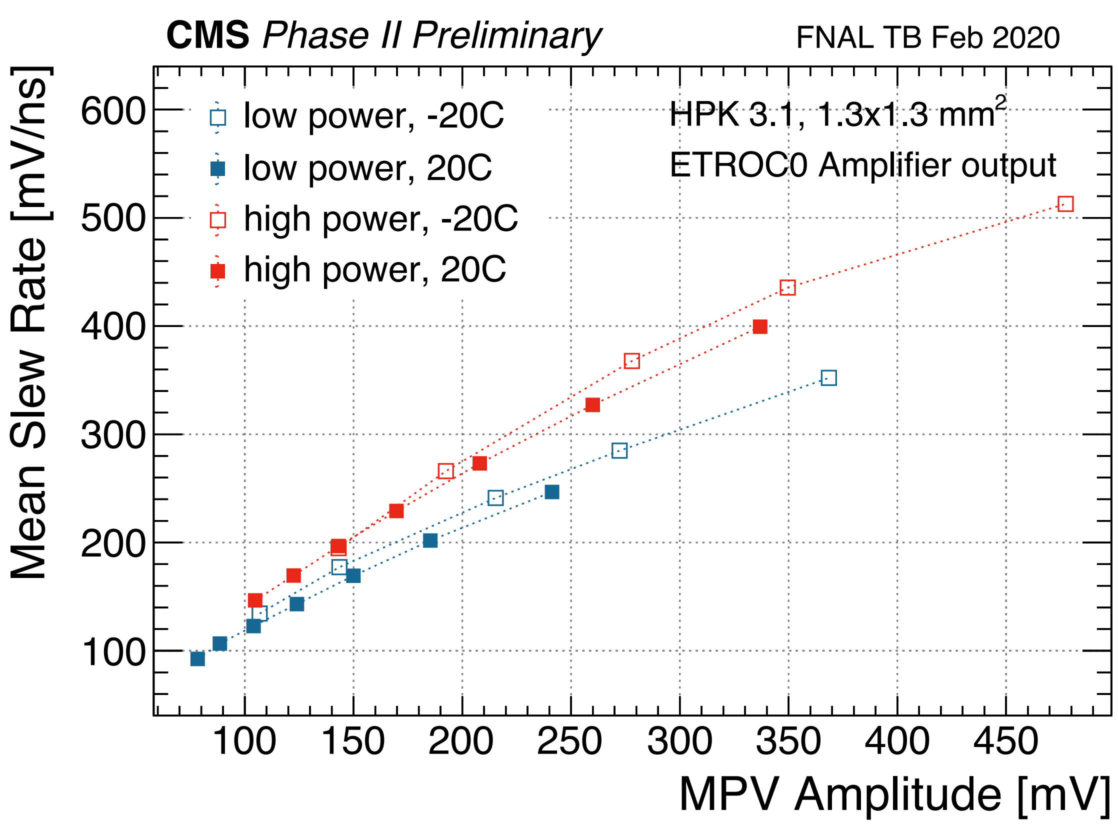


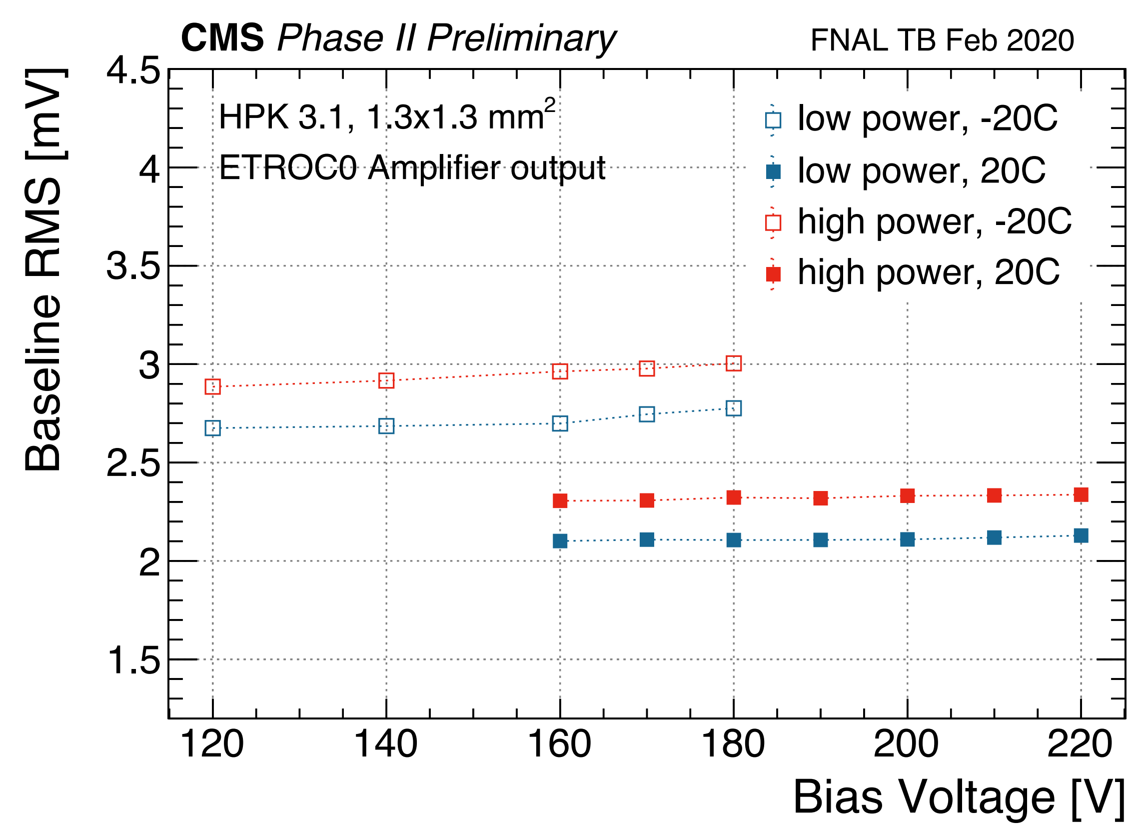


Amplifier performance

key ingredients for understanding jitter and time resolution

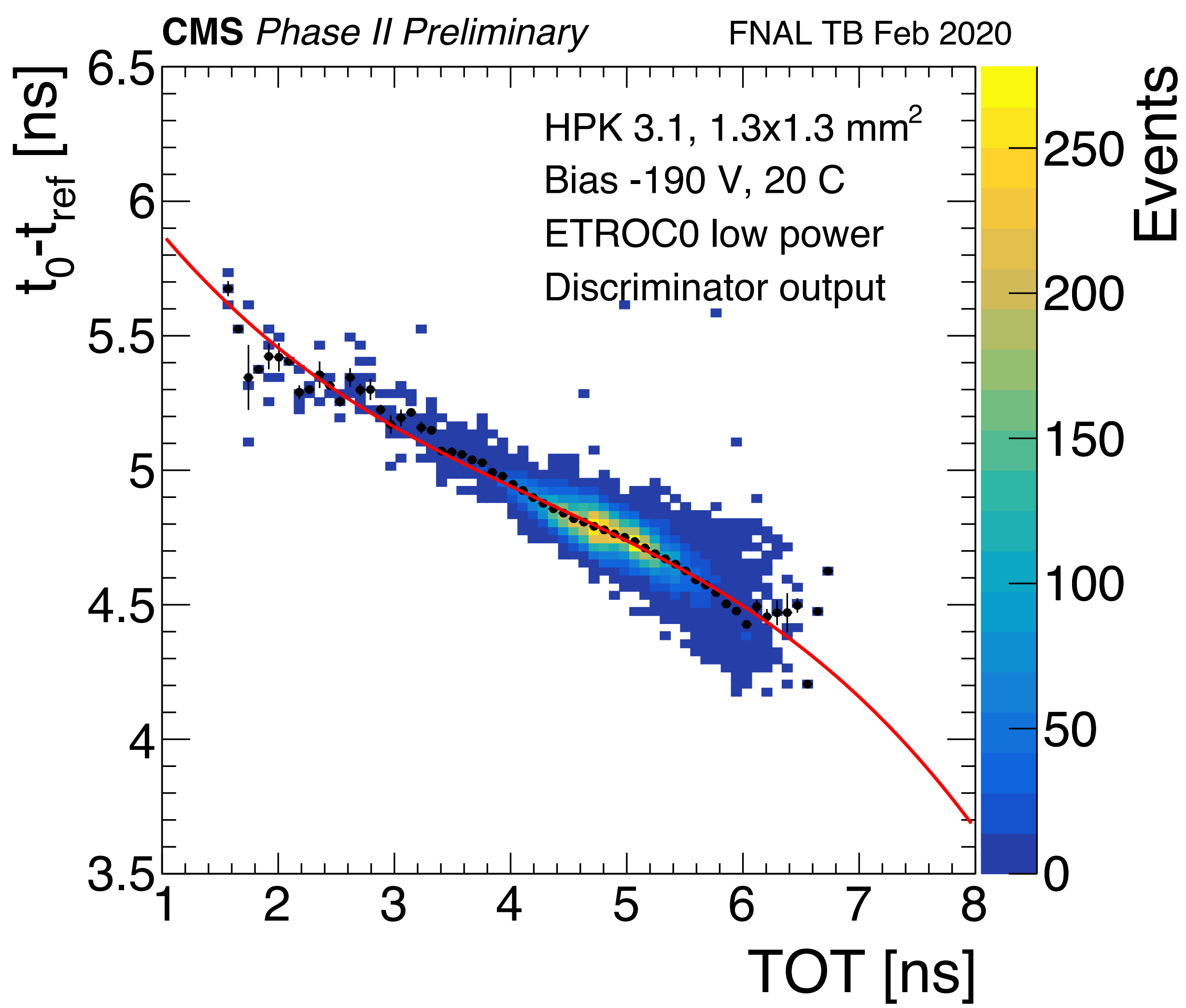






ETROC0 Discriminator procedure

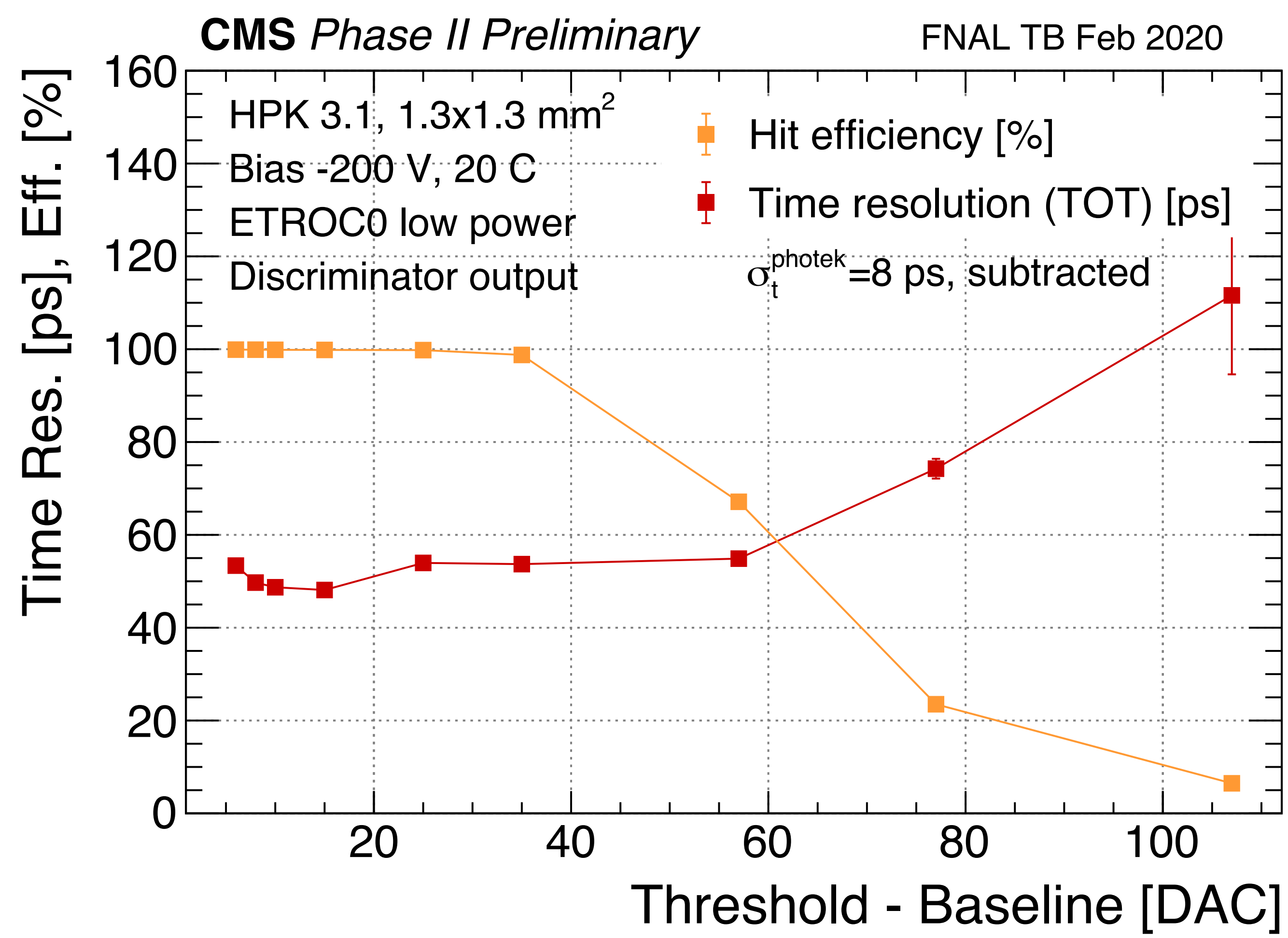
Example time-walk correction



in this configuration, MPV is 14 fC → 4.5 ns TOT, and the bulk is between 10-25 fC → TOT of 4-5.5 ns

Example threshold scan

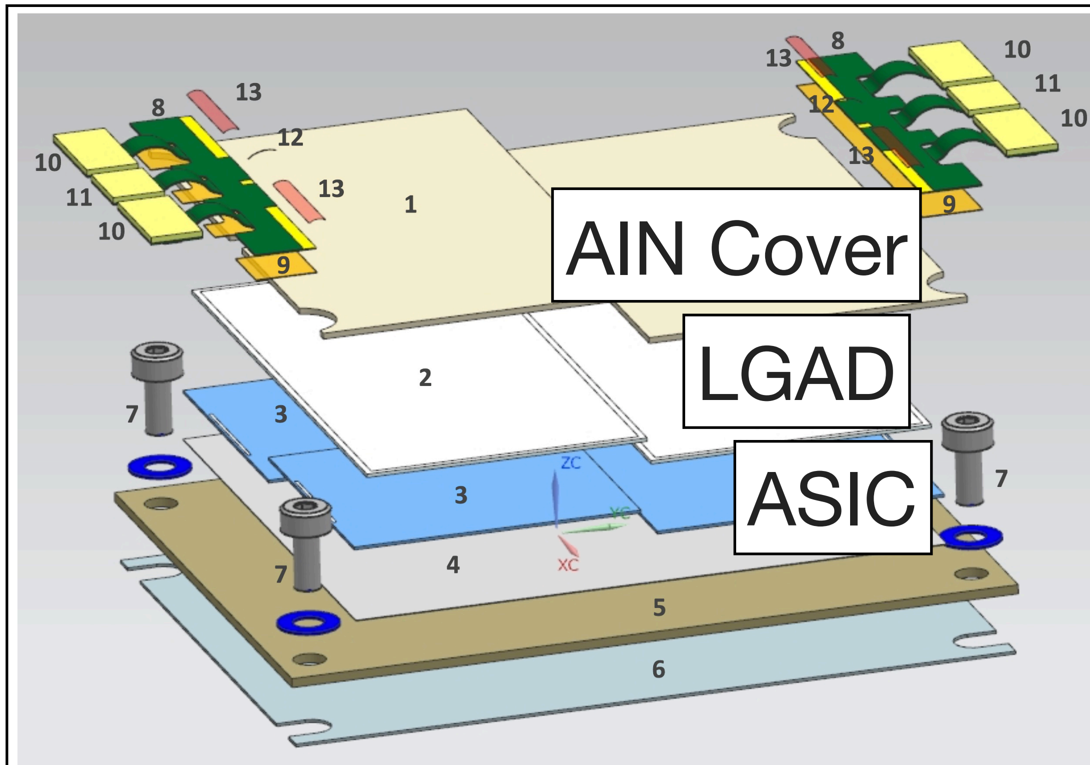
optimize efficiency & time resolution



nominally operate at 15 DAC above baseline

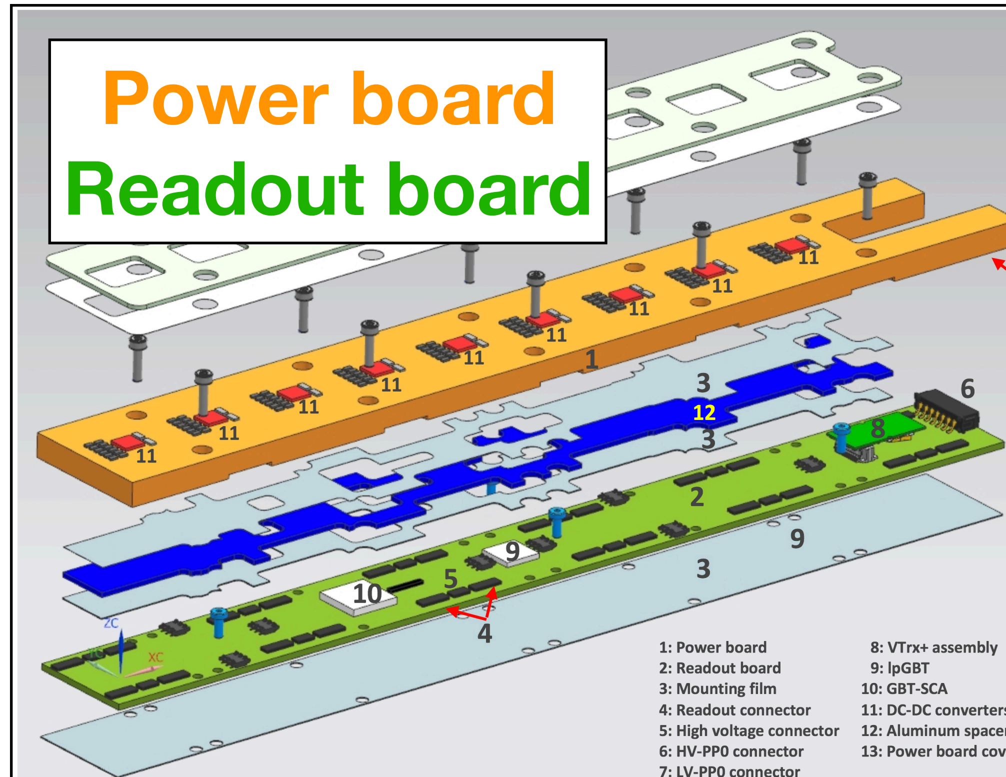
ETL Modules and Service Hybrids

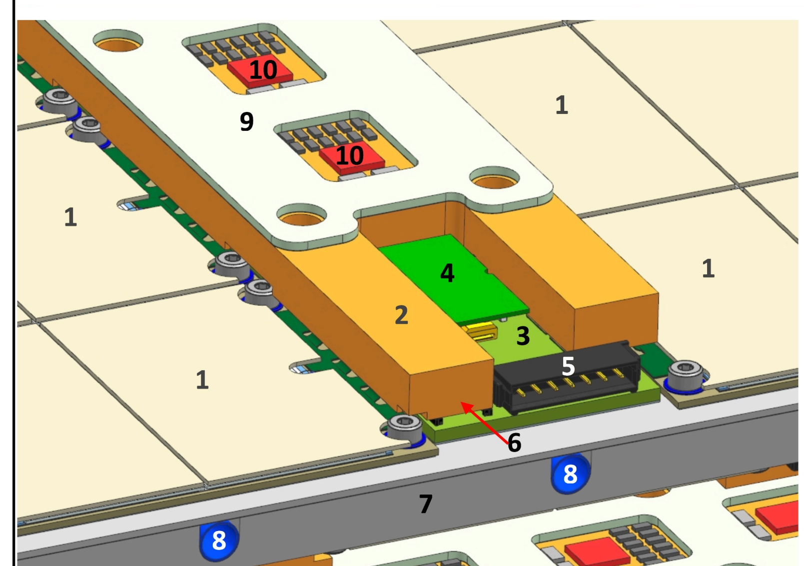
Module Design



1: AlN module cover
2: LGAD sensor
3: ETL ASIC
4: Mounting film
5: AlN carrier
6: Mounting film
7: Mounting screw
8: Front-end hybrid
9: Adhesive film
10: Readout connector
11: High voltage connector
12: LGAD bias voltage wirebond
13: ETROC wirebonds

Service Hybrid





1: AlN module cover
2: Power board
3: Readout board
4: VTRx+
5: HV-PP0 connector
6: LV-PP0 connector
7: Support disk
8: CO_2 cooling tube
9: Power board cover
10: DC-DC converters

ETL Detector Layout

Challenges at lower radii

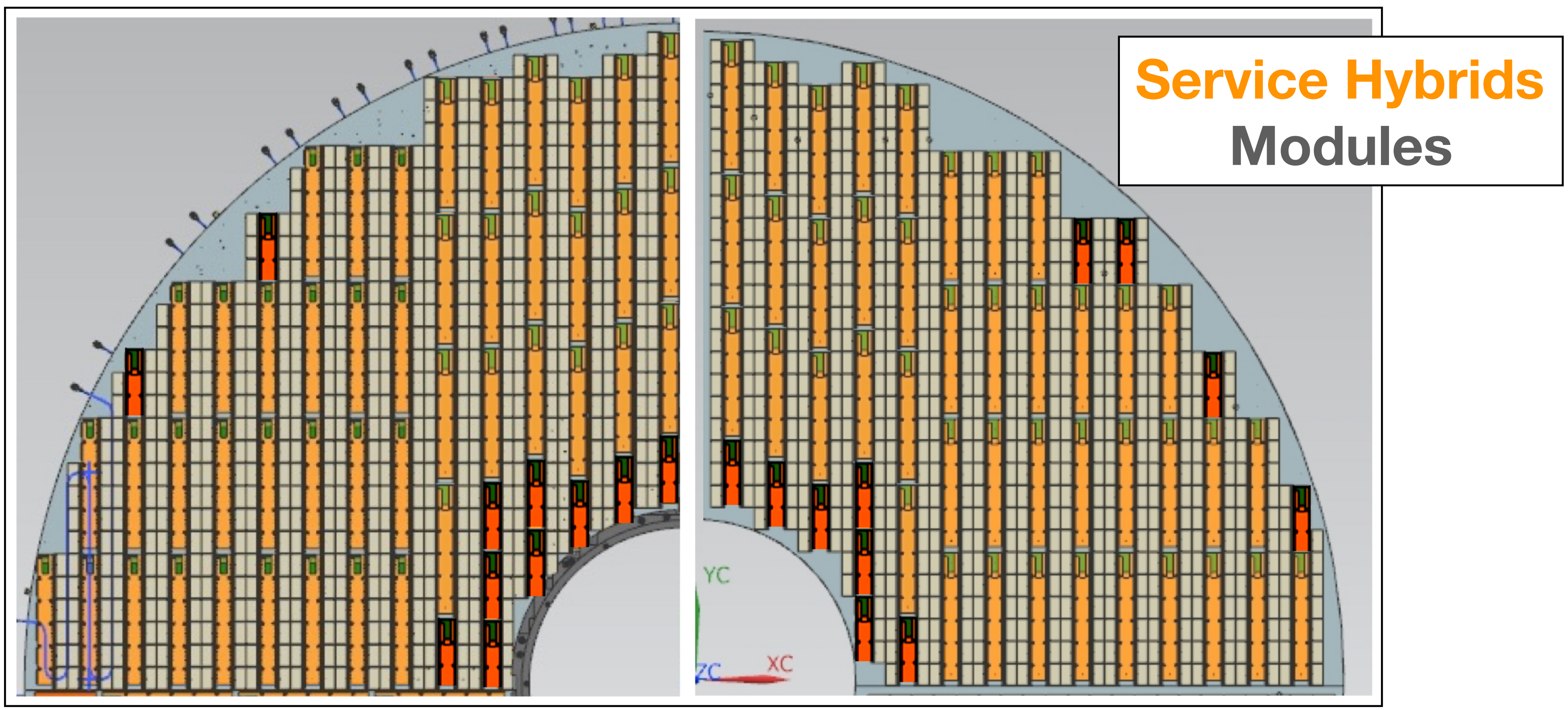
Increased radiation

15% of sensors: > 1 x 10^{15} neq/cm^2
80% of sensors: < 8 x 10^{14} neq/cm^2

Higher data rates for electronics

half-size service hybrids
to keep rates < 1 Gb/s

Front & back of one disk

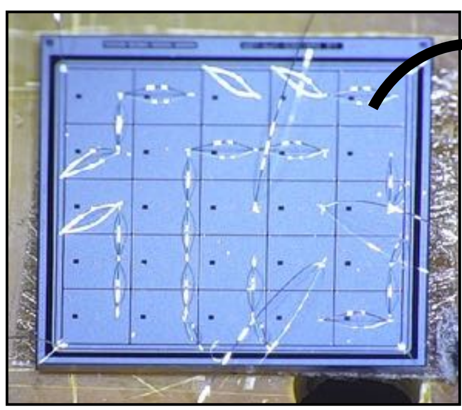


Time resolution performance

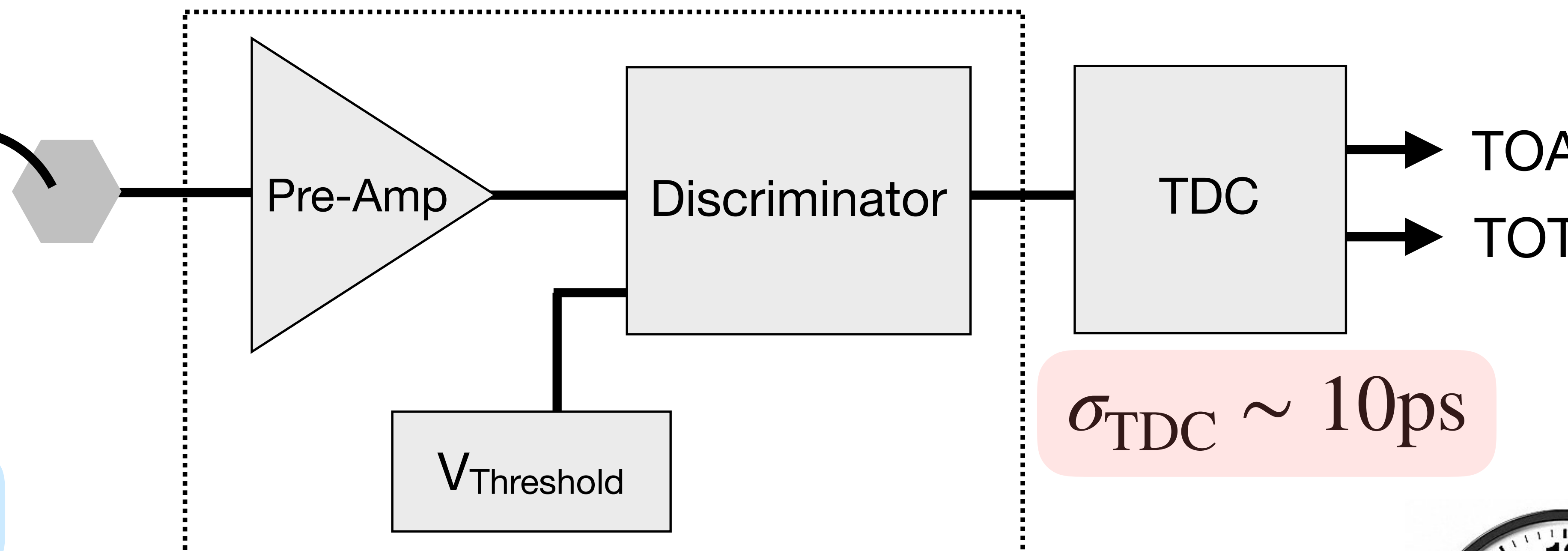
How to obtain 50 ps resolution per hit

$$\sigma_t^2 = \sigma_{\text{ionization}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{clock}}^2$$

Sensor

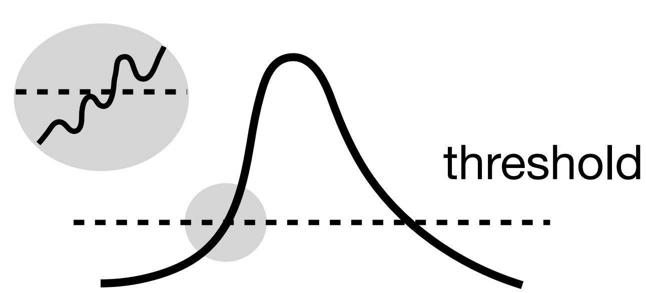


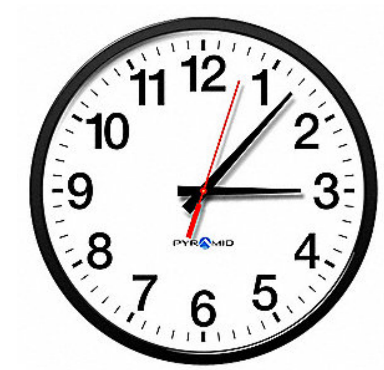
$\sigma_{\text{ioniz.}} \sim 30\text{ps}$



$\sigma_{\text{TDC}} \sim 10\text{ps}$

$$\sigma_{\text{jitter}} \sim \frac{\text{N}}{\text{dV/dt}} < 40\text{ps}$$





$\sigma_{\text{clock}} < 15\text{ps}$