

# Level-1 Track Finding at CMS for the HL-LHC

*Tuesday, 28 July 2020 16:45 (15 minutes)*

The success of the CMS physics program at the HL-LHC requires maintaining sufficiently low trigger thresholds to select processes at the electroweak scale. With an average expected 200 pileup interactions, critical to achieve this goal while maintaining manageable trigger rates is in the inclusion of tracking information in the Level-1 (L1) trigger. A 40 MHz silicon-based track trigger on the scale of the CMS detector has never before been built; it is a novel handle, which in addition to maintaining trigger rates can enable entirely new physics studies.

The main challenges of reconstructing tracks in the L1 trigger are the large data throughput at 40 MHz and the need for a trigger decision within 12.5  $\mu$ s. To address these challenges, the CMS outer tracker for HL-LHC uses modules with closely-spaced silicon sensors to read out only the hits compatible with charged particles above 2-3 GeV ("stubs"). These are used in the back-end L1 track finding system, implemented using commercially available FPGA technology. The ever-increasing capability of modern FPGAs combined with their programming flexibility are ideal for implementing fast track finding algorithms. The proposed reconstruction algorithm forms track seeds ("tracklets") from pairs of stubs in adjacent layers of the outer tracker. These seeds provide roads where consistent stubs are included to form track candidates. Track candidates sharing multiple stubs are combined prior to being fitted. A Kalman Filter track fitting algorithm is employed to identify the final track candidates and determine the track parameters. The system is divided into nine sectors in the r-phi plane, and time-multiplexed by a factor of 18, so that each event in one sector is processed by a dedicated track finding board.

This presentation will discuss the CMS L1 track finding algorithm and its implementation, present simulation studies of estimated performance, and show recent results from a scalable system demonstrator based on prototype hardware.

## I read the instructions

### Secondary track (number)

12.

**Primary author:** HART, Andrew Evan (Rutgers University)

**Presenter:** HART, Andrew Evan (Rutgers University)

**Session Classification:** Detectors for Future Facilities (incl. HL-LHC), R&D, Novel Techniques

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