环形正负电子对撞机
Circular Electron Positron Collider

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Chinese Academy of Sciences

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SHANDONG UNIVERSITY

Development of high resolution low power silicon pixel sensors for the CEPC vertex detector

Qun Ouyang (IHEP)

On behalf of the study group

ICHEP 2020 | PRAGUE

28 July 2020 to 6 August 2020
virtual conference
Europe/Prague timezone

Outline:

- Introduction
- Updates on CPV3(SOI) and JadePix3(CMOS)
- Perspective for the next step
- Summary

Introduction: requirements (CDR)

- **On the pixel sensor for the efficient tagging of heavy quarks**
- To achieve S.P. resolution
  - Digital pixel with in-pixel discriminator ~ 16 μm
  - Analog pixel ~ 20 μm (heavily rely on power pulsing as in the ILC)
- To lower the material budget
  - Sensor thickness ~ 50 μm
  - Heat load < 50 mW/cm^2 constrained by air cooling
- To tackle beam-related background
  - ~ μs level readout, 25 ns beam spacing @ Z-pole operation
  - 3.4 Mrad/year & 6.2×10^{12} $n_{eq}/(cm^2 \cdot year)$

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

time stamp

2 mm

foam

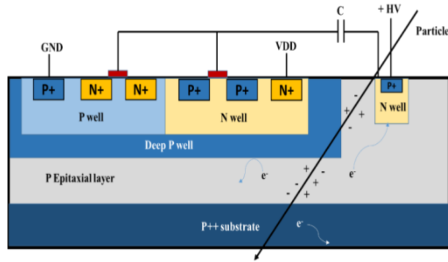
spatial resolution

ILD-like double-sided concept without power-pulsing mode

Physics driven requirements	Running constraints	Sensor specifications	
$\sigma_{s.p.}$ 2.8um		Small pixel	*~16 μm*
Material budget 0.15% X_0/layer		Thinning to	*50 μm*
	Air cooling	low power	*50 mW/cm^2*
r of Inner most layer 16mm	beam-related background	fast readout	*~1 μs*
	radiation damage	radiation tolerance	*≤3.4 Mrad/ year* *≤6.2×10^{12} $n_{eq}/(cm^2$ year)*

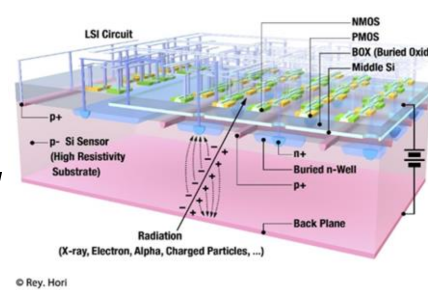
Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Overview of R&D activities



CMOS pixel sensor

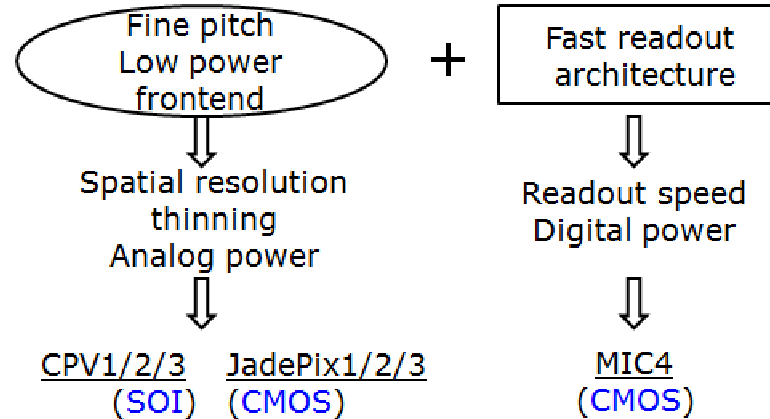
- *TowerJazz CIS 0.18 μm process*
- *Quadruple well process*
- *Thick (~20 μm) epitaxial layer*
- *with high resistivity (≥1 kΩ•cm)*



SOI pixel sensor

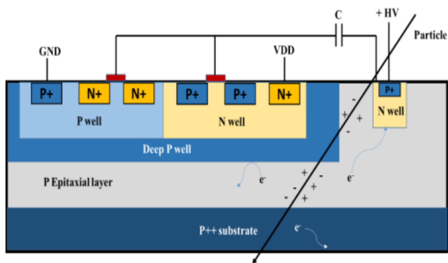
- *LAPIS 0.2 μm process*
- *High resistive substrate (≥1 kΩ•cm)*
- *Double SOI layers available*
- *Thinning and backside process*

Towards Baseline Requirements: CMOS and SOI R&D in Synergy



CEPC

Overview of R&D activities



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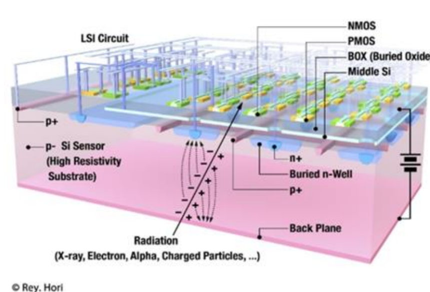

SOI pixel sensor

- *LAPIS 0.2 μm process*
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- *Thinning and backside process*

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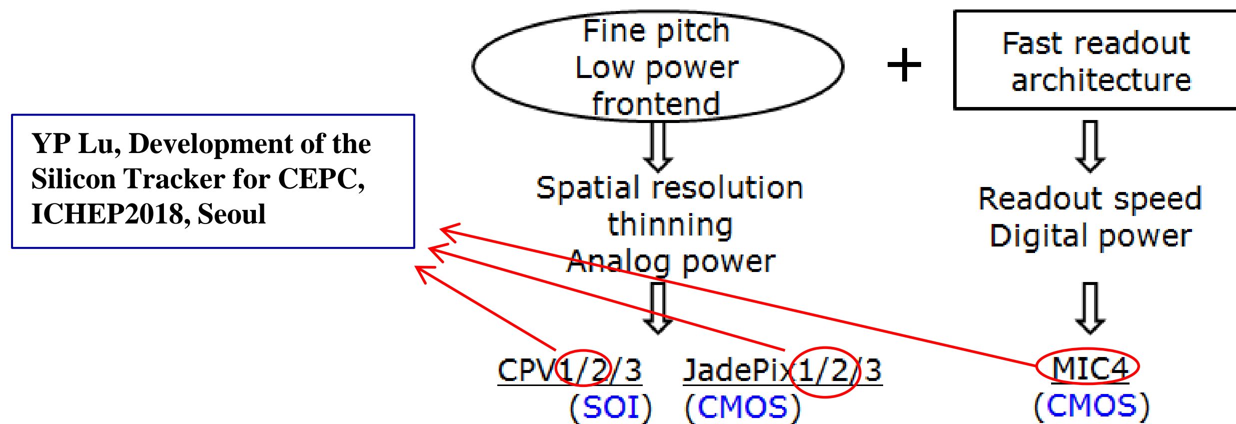
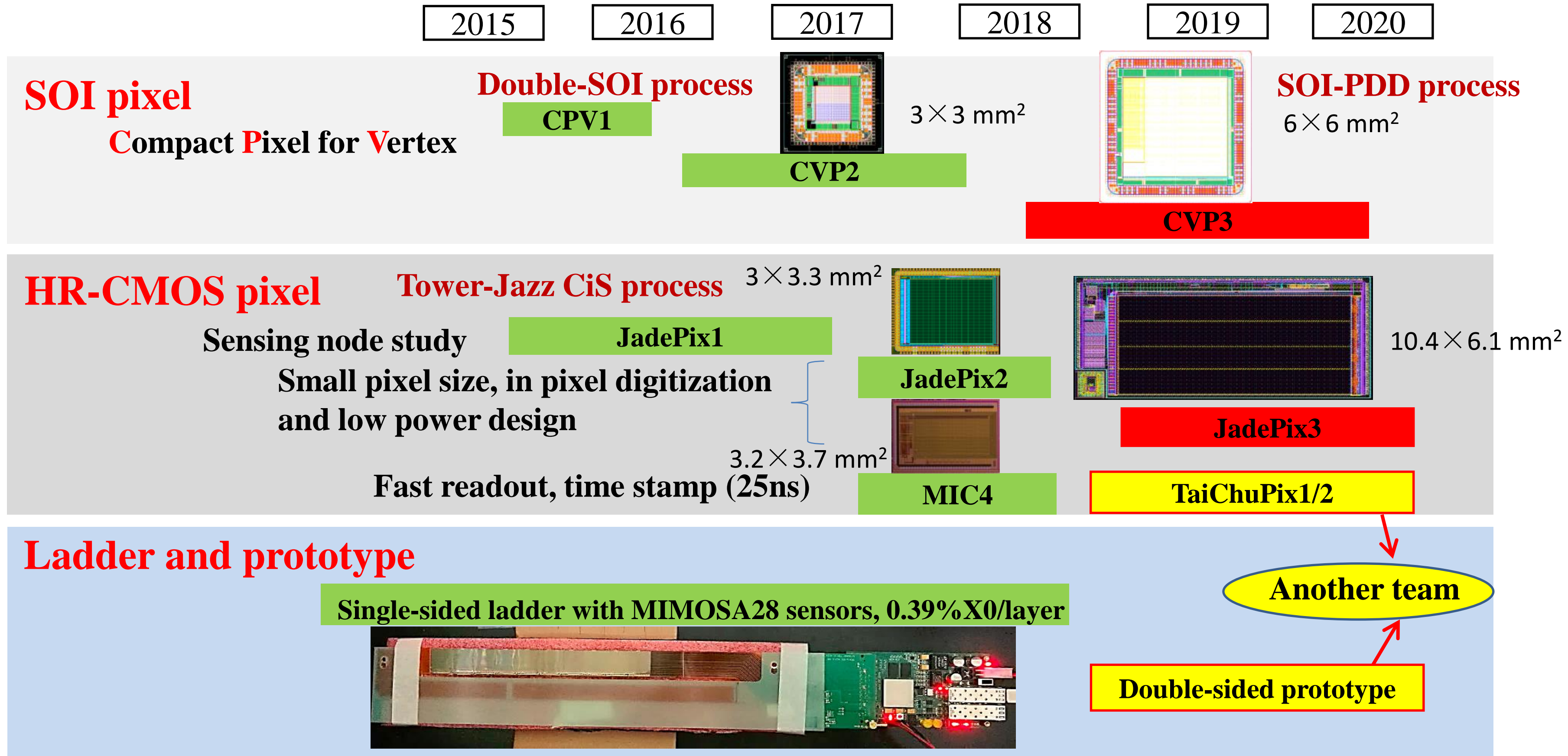


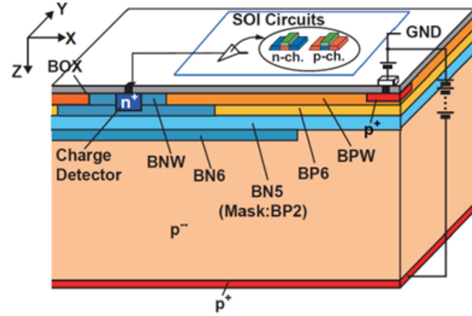
Overview of R&D activities (cont.)

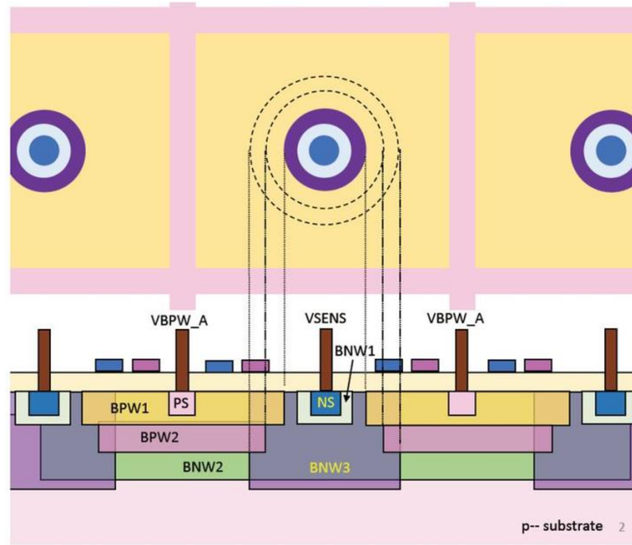


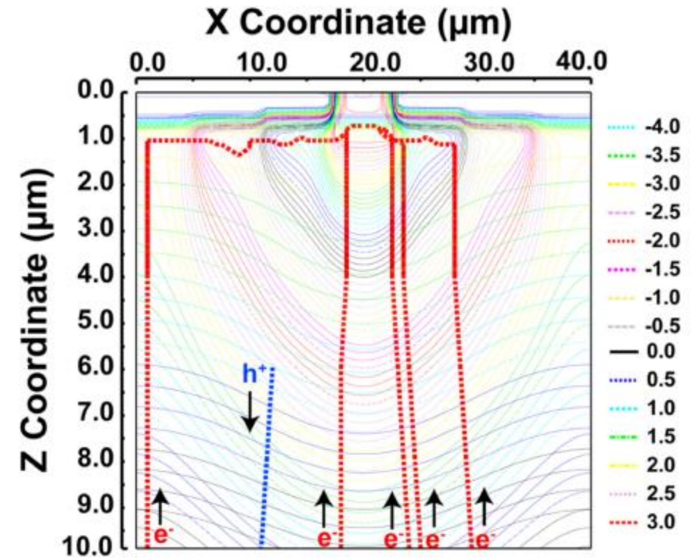
CEPC

CPV3: an novel design with SOI-PDD process

- **Pinned Depleted Diode** process proposed by Shoji Kawahito (Shizuoka U.)
  - Pinned Si surface layer → reduction of surface leakage by 2 orders
  - Depleted charge collection electrode → reduction of diode capacitance
  - Lateral electric field → improved charge collection efficiency





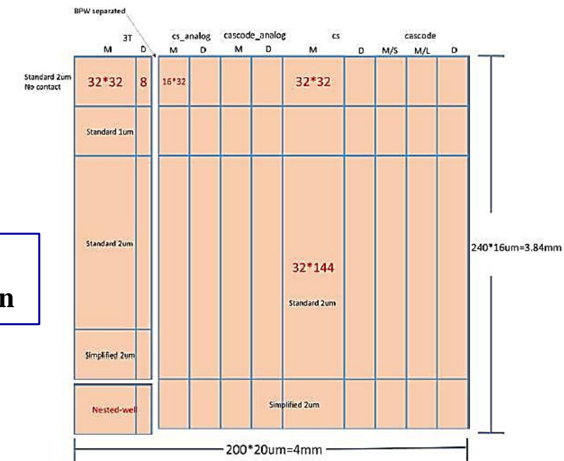


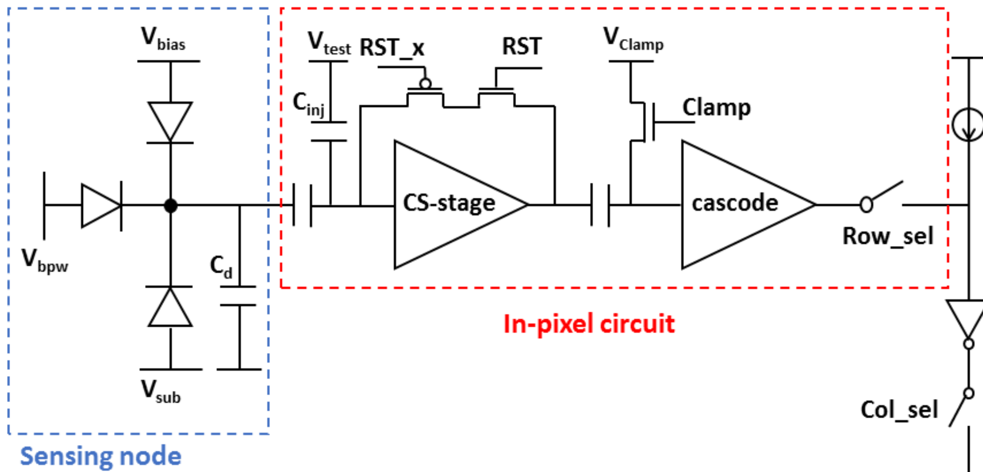
Ref: Sensors 2018, 18, 27; doi:10.3390/s18010027

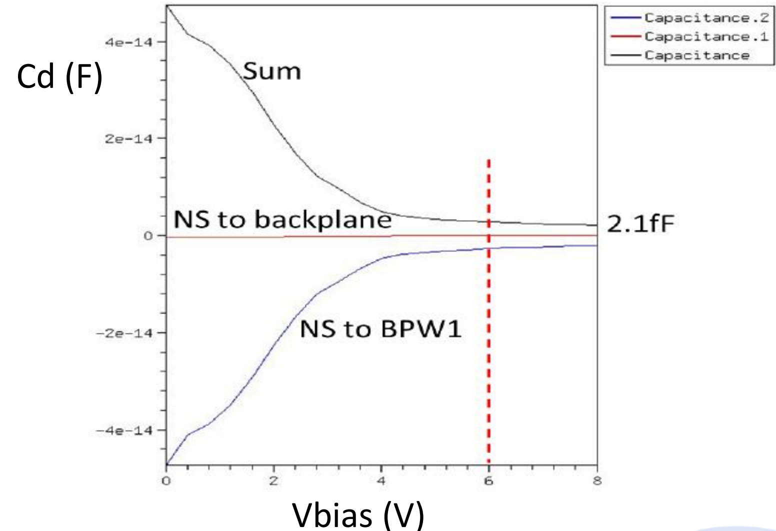
CPV3 design

- **Sensing node AC-coupled to the amplifier to allow V_{bias} up to +10V**
  - Minimize the capacitance at pixel pitch 16 μm×20 μm
- Common Source (CS) amplifier, DC gain = 13
- Cascode stage + current source, discriminator
- Statistical simulation, FPN = 12 e^- * CPV2: 114 e^-
- Mask area: 6mm×6mm
  - Optimized for low FPN
  - Pixel matrix divided as 45 regions, to verify design options
  - Rolling shutter readout

ZG Wu, HSTD12, 14-18 Dec.2019, Hiroshima, Japan

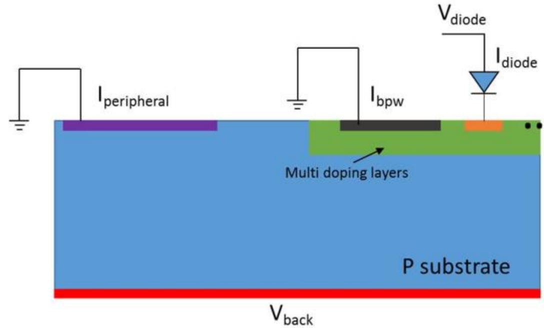






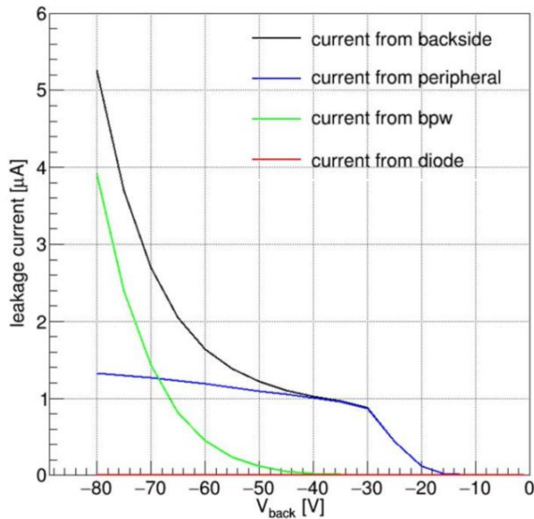
Sensor tests

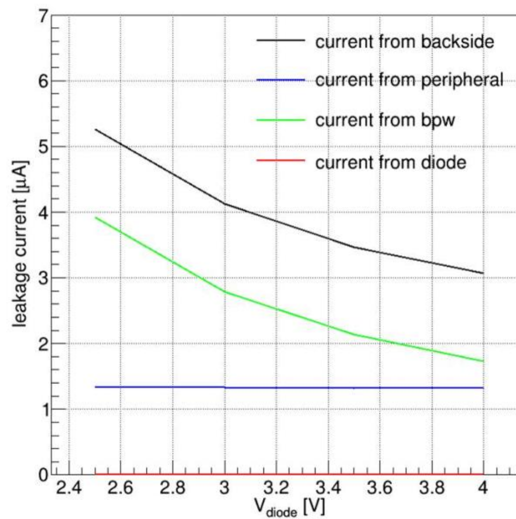
- Leakage current components
  - Dominated by the peripheral and bpw
  - Sum of sensing diode ~ nA
- V_{diode} = +4V suppressed leakage on bpw and peripheral
  - Increased barrier potential

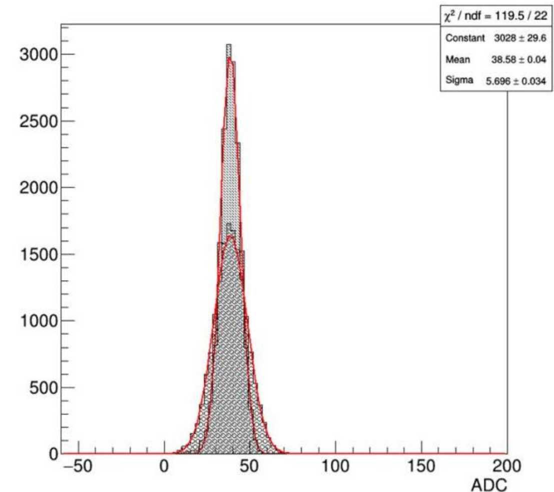


Calibration with ^{55}Fe X-ray

- V_{diode}=+4V，V_{bpw}=0V，V_{back}=-60V
- Charge collected in a 3*3 cluster
- Wider peak spread of 5*5 cluster due to electrical noise
- Equivalent C_d = 12fF



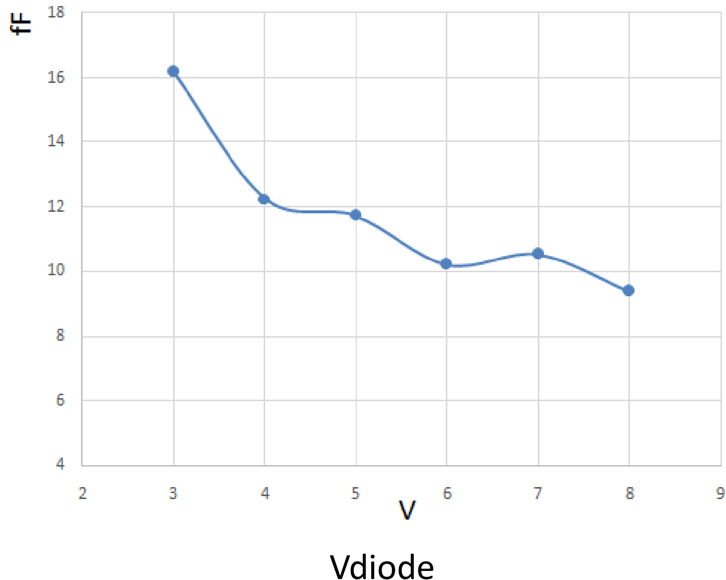


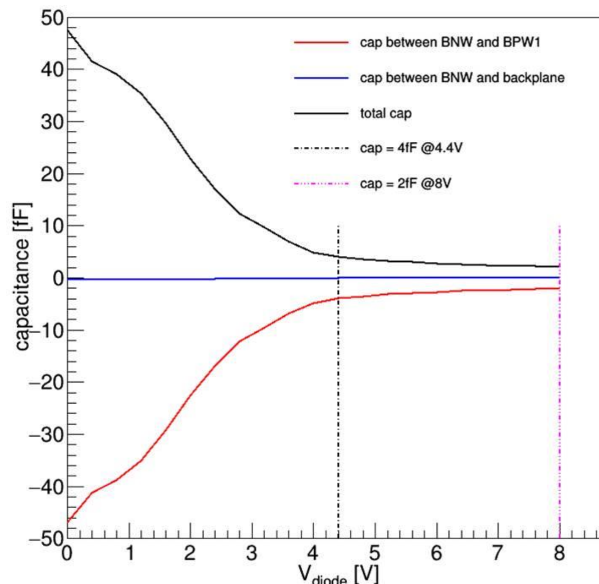


CEPC

Verification of C_d reduction

- V_{back}=-60V，V_{bpw}=0V，increase V_{diode}
  - Proof of PDD bias concept
- Expected to be 4fF@4.4V + parasitic capacitance
  - Parasitic capacitance from the routing, AC capacitor and input transistor
  - Patially confirmed by RC extraction (simulation)





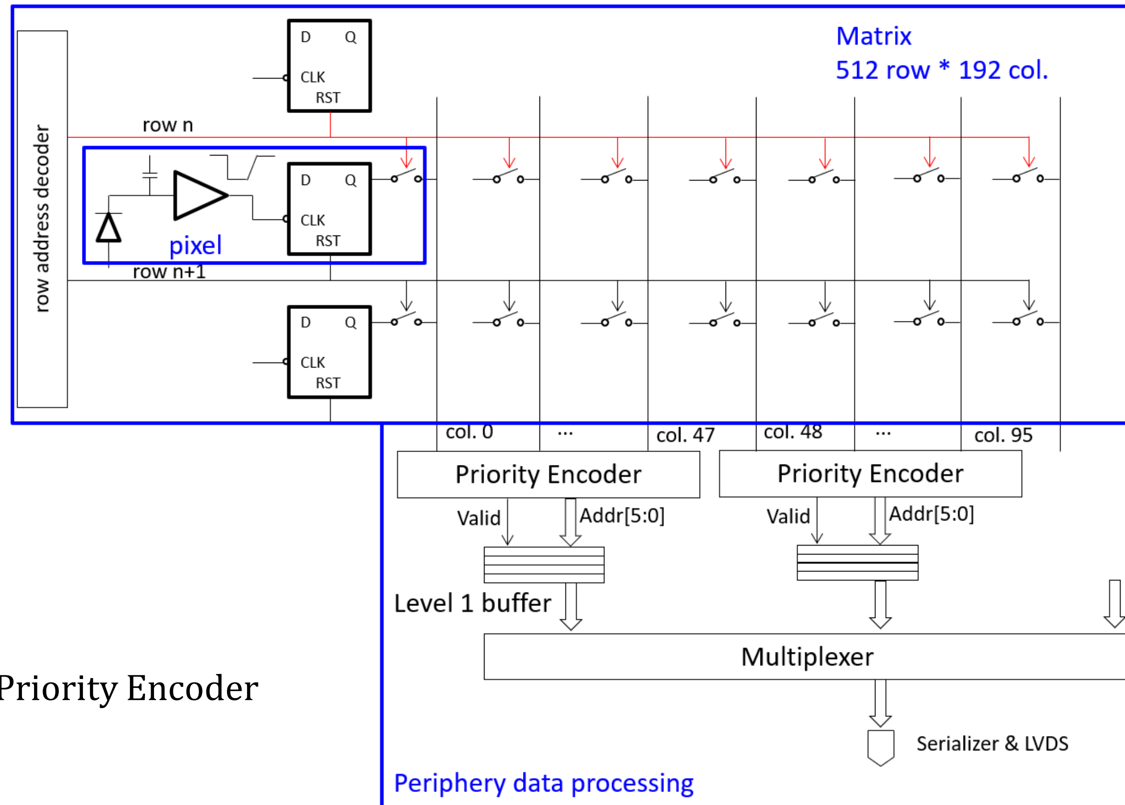
More tests to do

- Optimize the operation of pixel circuit
  - Compare different structures
- Noise and threshold measurement
- Laser test or beam test next year
  - the outcome of full characterization
  - and possible scheme together with CMOS sensor

JadePix3: fully functional prototype with small pixel design

- **Specification:**
- Spatial resolution
  - ~ 3 μm
  - Initial pixel size 16 μm × 20 μm
  - FPN < $20e^{-}$
- Power consumption
  - < $100mW/cm^2$
  - Measureable

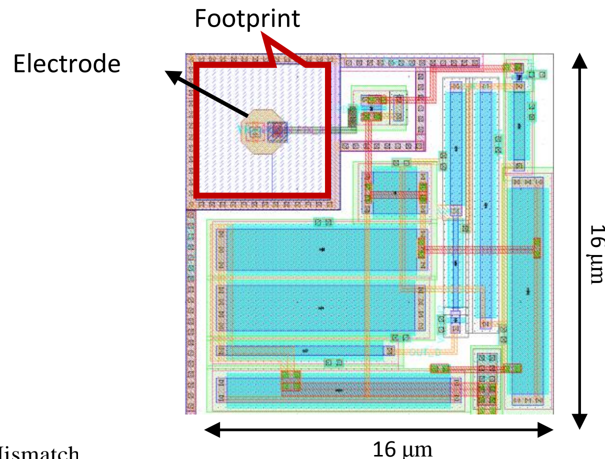
Small pixel: Low power FE + Rolling shutter Readout

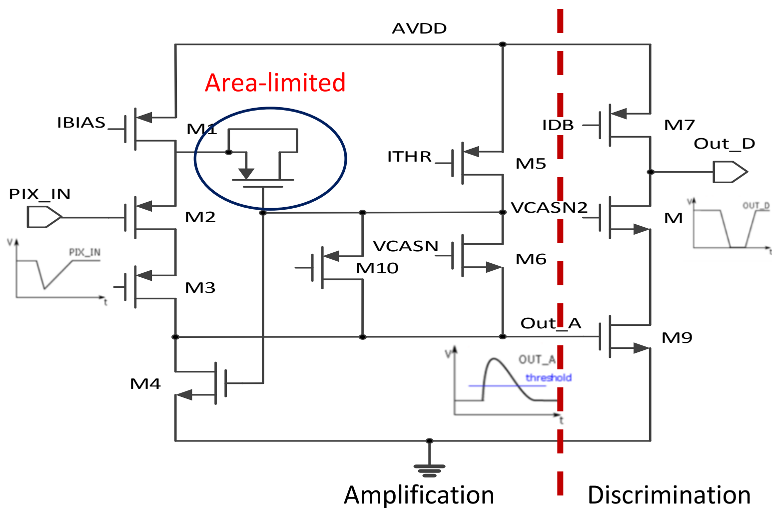


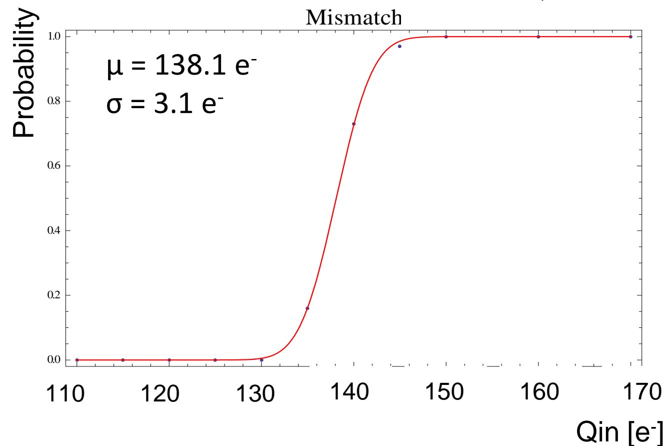
- **Rolling shutter readout**
  - 512 row × 192 col
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Encoder at the end of columns.

JadePix3: Diode & Front-end design

- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 μm^2, with a small footprint 36 μm^2
- Frontend: tradeoff between layout area and FPN
  - Reduction on the layout area, ~200 μm^2
  - Improvement on the FPN = 3.1e$^-$ (simulation)
  - A low power version (20nA), equivalent to 9 mW/cm^2







CEPC

JadePix3: chip status

P Yang, CEPC workshop, Nov.2019
YP Lu, HSTD12, 14-18 Dec.2019, Hiroshima, Japan

- Submitted in Oct. 2019
- Process finished in May 2020
- Diode, minimum size
  $S_{diode}=4\mu m^2$, $S_{footprint}=36\mu m^2$, $C_{diode}\sim 4\text{-}5fF$
- Front-end, 2 versions
  - FE_V0, FE_V1 (20nA, 60nA)
- Pixel digital, 3 versions
  - DGT_V0, DGT_V1, DGT_V2
- Pixel area
  - $16\times26\ \mu m^2$
  - $16\times23.11\ \mu m^2$

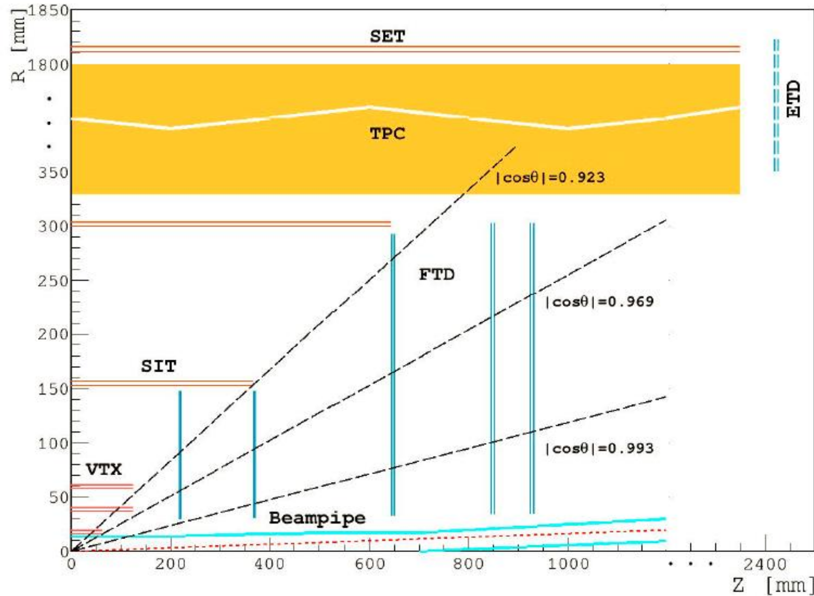
Estimated: ~$55mW/cm^2$:
- $9mW/cm^2$（pixel array）
- $30mW/cm^2$（zero suppression & data buffer）
- $6.25mW/cm^2$（Serializer）
- $5mW/cm^2$（PLL）
- $4mW/cm^2$（LVDS）

Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	**$16\times26\ \mu m^2$**
1	2 + 2 μm	FE_V0	DGT_V1	**$16\times26\ \mu m^2$**
2	2 + 2 μm	FE_V0	DGT_V2	**$16\times23.11\ \mu m^2$**
3	2 + 2 μm	FE_V1	DGT_V0	**$16\times26\ \mu m^2$**

Test plan

- May - Aug. 2020
  - Sub-board to mount the chip into readout system
  - Readout system debugging
- Sep. 2020 - Feb. 2021
  - Characterization of individual parts on chip
  - Optimization of operation
  - ^{55}Fe 5.9 keV X-ray calibration
- Sometime in 2021
  - Beam test

Perspective for the R&D of next few years



Design parameters of the CEPC vertex system in CDR

	R(mm)	$\mid Z \mid$(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	$0.15\%/X_0$
Layer 2	18	62.5	6	$0.15\%/X_0$
Layer 3	37	125.0	4	$0.15\%/X_0$
Layer 4	39	125.0	4	$0.15\%/X_0$
Layer 5	58	125.0	4	$0.15\%/X_0$
Layer 6	60	125.0	4	$0.15\%/X_0$

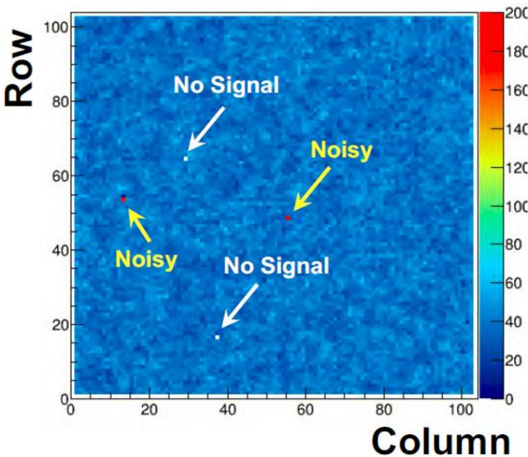
- Optimization for system requirements: resolution, radiation level, Z-pole operation mode, ...
- Development of CMOS sensors with fast readout and time stamp
- Exploration of new process
  - 3D process → SOI-3D accessible via SOIPIX
  - Ultra-light, self-supported layers with stitching CMOS sensors

SOI based 3D integration

T-Micro process

Miho Yamada, 3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment, IEEE 3DIC, Sendai, October 8th, 2019

Hit Map (50 kEvents)



Connection yield > 99.9%

SOFIST

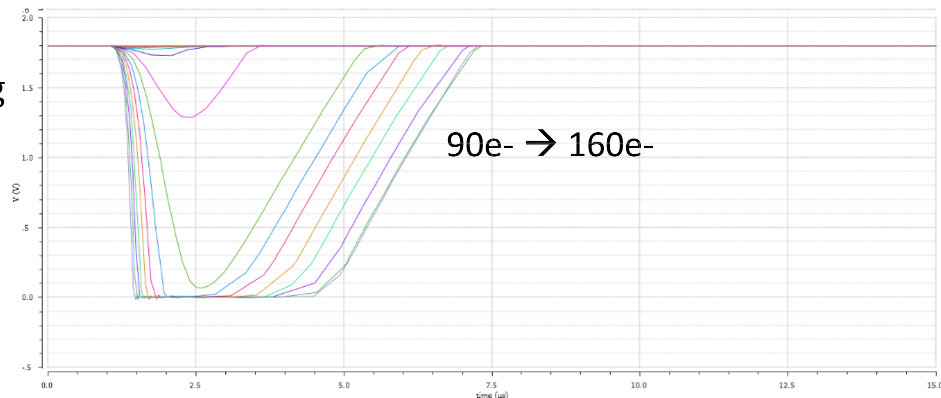
Upper Chip
Lower Chip
Remove Handle Wafer
CMOS Circuit (Digital)
inject glue
CMOS Circuit (Analog)
Sensor
Wire bonding pad for packaging
Upper Chip
Lower Chip
CMOS Circuit (Digital)
CMOS Circuit (Analog)
Sensor
Passivation
Al Wire Bonding Pad for Packaging
BOX
PMOS
NMOS
Gate Poly Si
Metal 1
Metal 2
Metal 3
Metal 4
Metal 5
Upper Chip
Al
p+
p-
Handle Wafer
Remove Sensor by Wet Etching
Lower Chip

3D integration by T-Micro

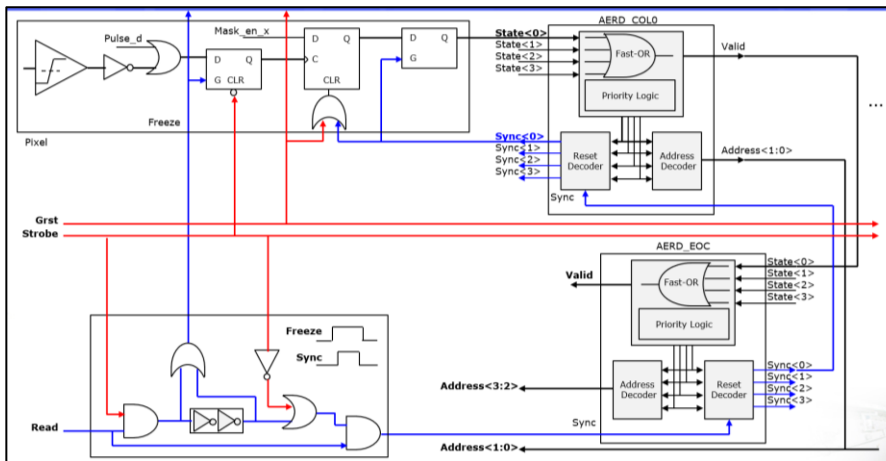
	SOFIST1	SOFIST2	SOFIST3	SOFIST4 (3D)
				4.45 x 4.45
				20 x 20
				104 x 104 (Analog signal and Time stamp)
				Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Under evaluation	Delivered (Jan. 2019 ~)

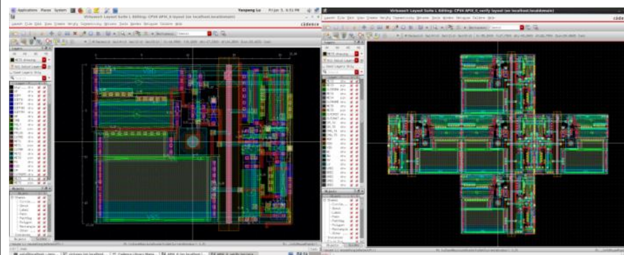
Development of SOI-3D chip for CEPC

- Faster and low power
  - Timing ~ 1us, hit registered at the fast falling edge
  - Power consumption ~ 50mW/cm^2
  - Shrink the pixel size by SOI-3D
- Continuous readout mode (AERD)
  - Compatible with trigger mode
- CPV4_3D submission plan ~Nov.2020

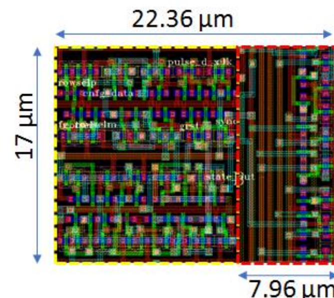


Output Waveform of Discriminator



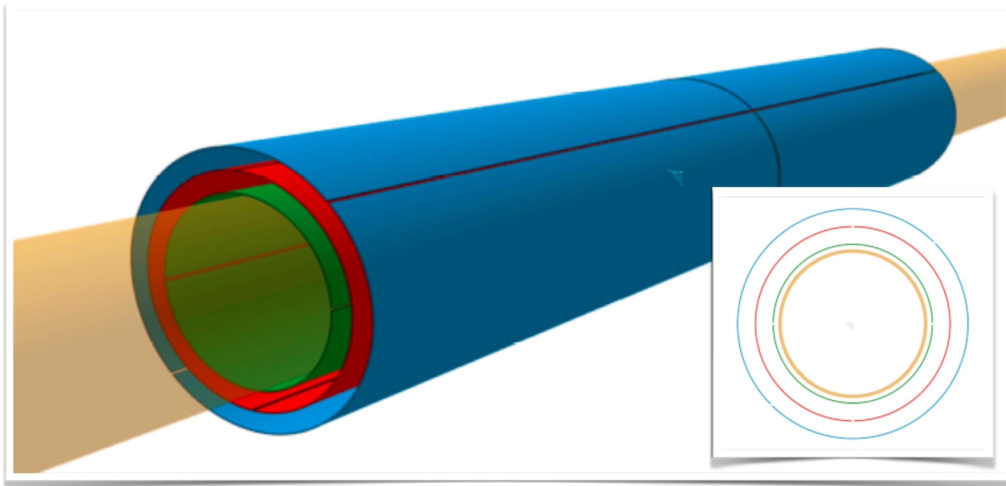


pixel layout (analog)



Digital Pixel Section	Priority encoder

ALICE ITS3 with stitching CMOS technology



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

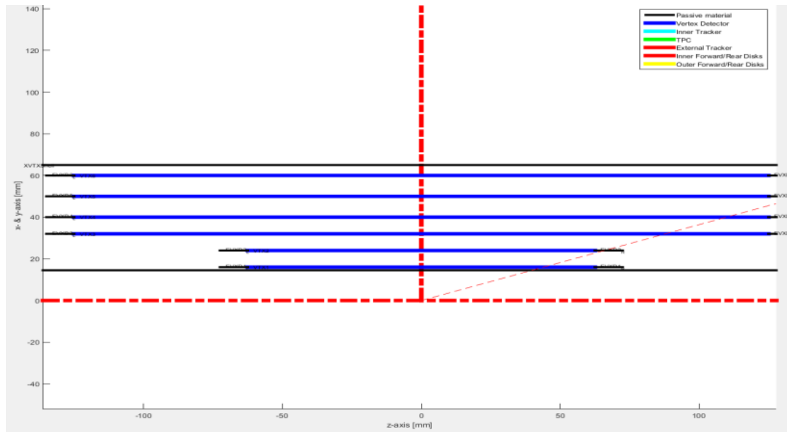
Similar layout with CEPC layer 1-3

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 μm (0.14% X0)
  - Sensor thickness: 20-40 μm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

M. Mager | ITS3 | VERTEX 2019 | 17.10.2019 | 14

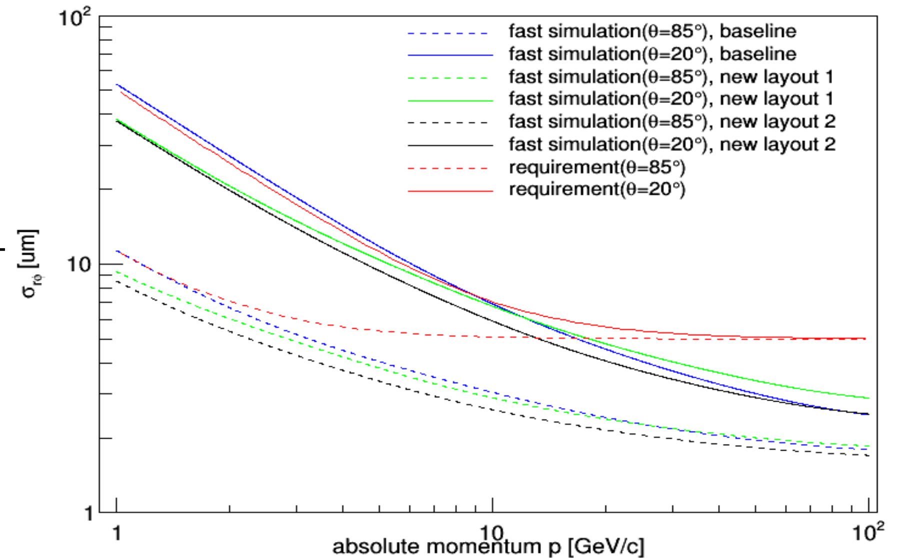
An ultra light structure vertex layout

	R(mm)	|Z|(mm)	σ(μm) (layout1/layout2)	material budget
Layer1	16	62.5	4/2.8	$0.05\%X_0$
Layer2	24	62.5	4/4	$0.05\%X_0$
Layer3	32	125	4/4	$0.05\%X_0$
Layer4	40	125	4/4	$0.05\%X_0$
Layer5	50	125	4/4	$0.05\%X_0$
Layer6	60	125	4/4	$0.05\%X_0$



- Technology to be explored with 55 nm CiS process
- Joint effort of CCNU and IHEP

ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop, Nov.2019, Beijing

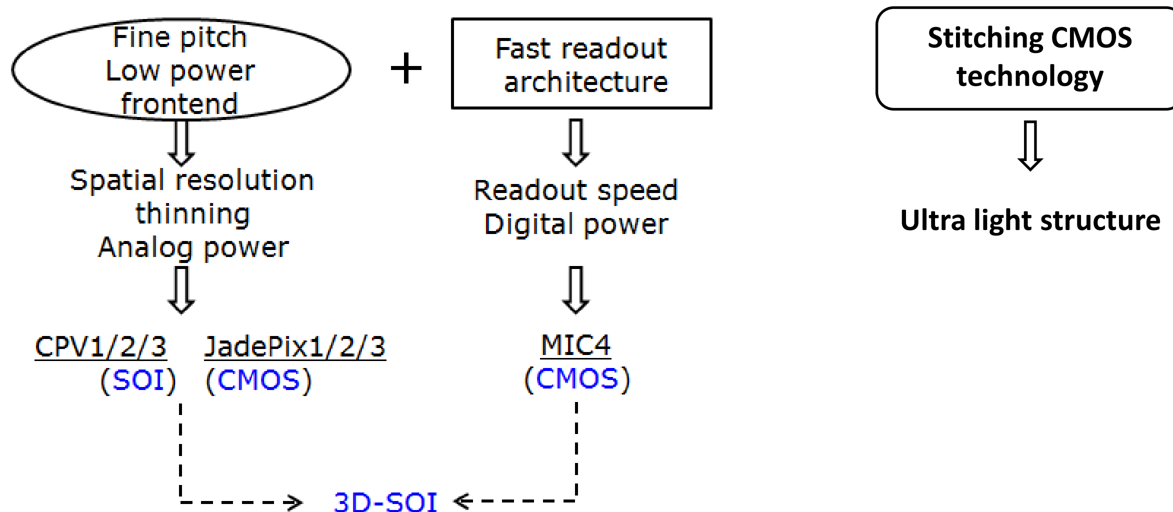


Comparing with baseline layout

- better performance (~20% improvement) for layout1 at low momentum, but poor performance at high momentum
- both within the requirement

Summary

- Stringent requirements for CEPC vertex detector have driven R&D programs
- CMOS and SOI development in synergy
  - Following the same roadmap
  - Using the same readout system
- JadePix3 and CPV3 produced, and tests underway in parallel
- CPV4_3D design is ongoing, and stitching CMOS technology will be explored
- A Pixel Vertex prototype being built (to be finished in 2023) but it was not covered in this talk



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Study team

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- **CCNU:** *Ping Yang, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng, Anyang Xu, Xiangming Sun*
- **Dalian Minzu Unv:** *Zhan Shi*
- **SDU:** *Liang Zhang*

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- *the CAS Center for Excellence in Particle Physics (CCEPP)*

Thank you for your attention!

Backup

Updated Parameters of Collider Ring since CDR

	Higgs		Z (2T)	
	CDR	Updated	CDR	Updated
Beam energy (GeV)	120	-	45.5	-
Synchrotron radiation loss/turn (GeV)	1.73	1.68	0.036	-
Piwinski angle	2.58	3.78	23.8	33
Number of particles/bunch N_e (10^{10})	15.0	17	8.0	15
Bunch number (bunch spacing)	242 (0.68μs)	218 (0.68μs)	12000	15000
Beam current (mA)	17.4	17.8	461.0	1081.4
Synchrotron radiation power /beam (MW)	30	-	16.5	38.6
Cell number/cavity	2	-	2	1
β function at IP β_x^* / β_y^* (m)	0.36/0.0015	0.33/0.001	0.2/0.001	-
Emittance $\varepsilon_x/\varepsilon_y$ (nm)	1.21/0.0031	0.89/0.0018	0.18/0.0016	-
Beam size at IP σ_x/σ_y (μm)	20.9/0.068	17.1/0.042	6.0/0.04	-
Bunch length σ_z (mm)	3.26	3.93	8.5	11.8
Lifetime (hour)	0.67	0.22	2.1	1.8
Luminosity/IP L (10^{34} $cm^{-2}s^{-1}$)	2.93	5.2	32.1	101.6

Luminosity increase factor: × 1.8 (Higgs) × 3.2 (Z)

8

Br(H->bb, cc) measurement

- Br (H -> cc) is extremely sensitive to the vertex design
- Br (H -> bb) is not really sensitive to the vertex design

ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop Nov.2019

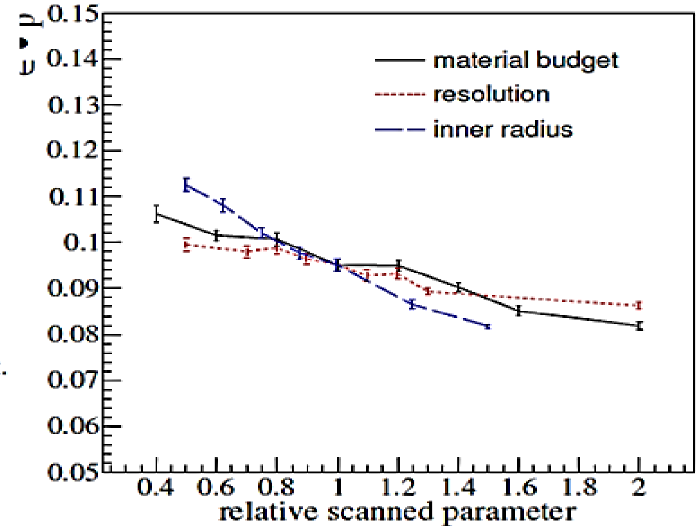
	Scenario A (Aggressive)	Scenario B (Baseline)	Scenario C (Conservative)
Material per layer/X_0	0.075	0.15	0.3
Spatial resolution/μm	1.4 - 3	2.8 - 6	5 - 10.7
R_{in}/mm	8	16	23

σ_{SP}<2.8 μm very difficult

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.133 ± 0.002	0.095 ± 0.001	0.078 ± 0.001
	41%		-22%

Table 4. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \to b\bar{b})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.925 ± 0.001	0.914 ± 0.001	0.900 ± 0.001
	1%		-1.5%



$$\epsilon \cdot p = 0.095(1 - 0.14\frac{\Delta x_{material}}{x_{material}})(1 - 0.09\frac{\Delta x_{resolution}}{x_{resolution}})(1 - 0.23\frac{\Delta x_{radius}}{x_{radius}})$$

Z. Wu, et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002

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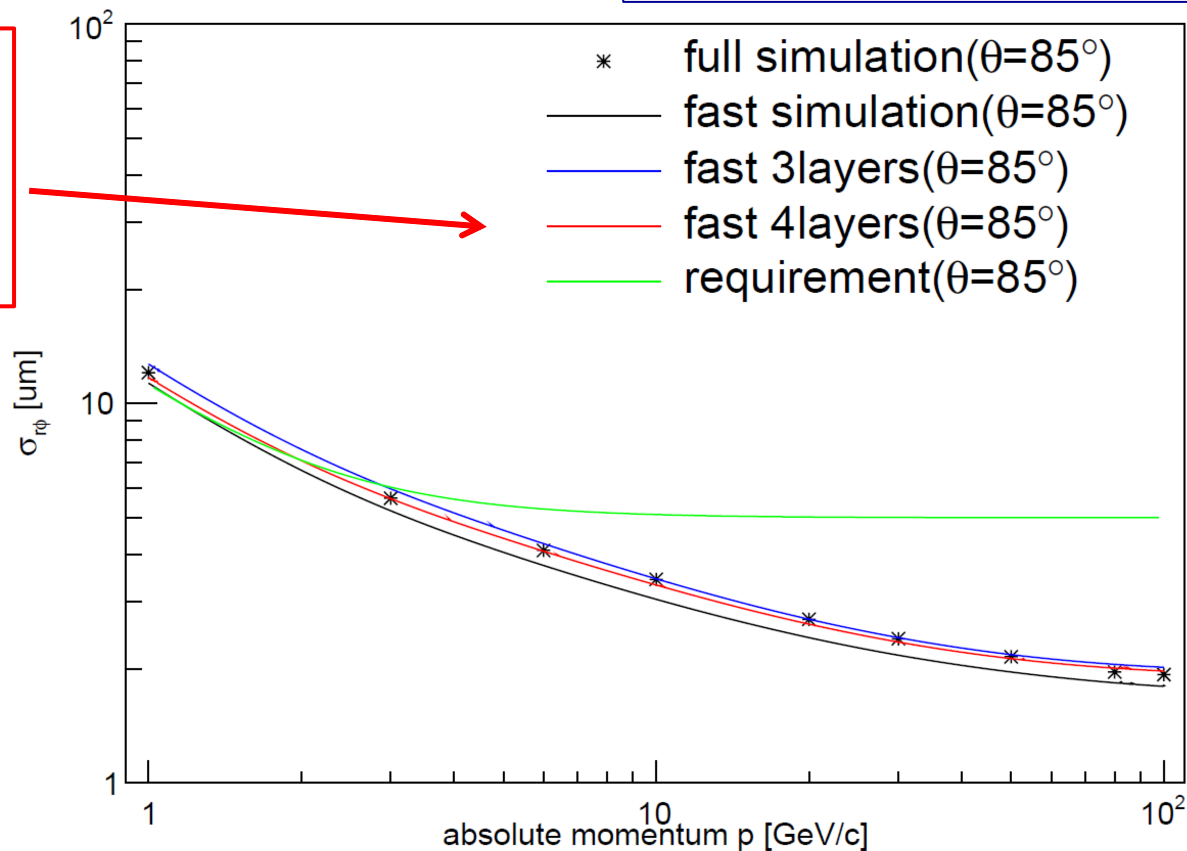
Same layout as in CDR

Q Ouyang, CEPC CDR review, Sept.2018

- σ_{sp}=4μm for L1 and L2
- σ_{sp}=3μm for combination of L3 and L4, and combination of L5 and L6

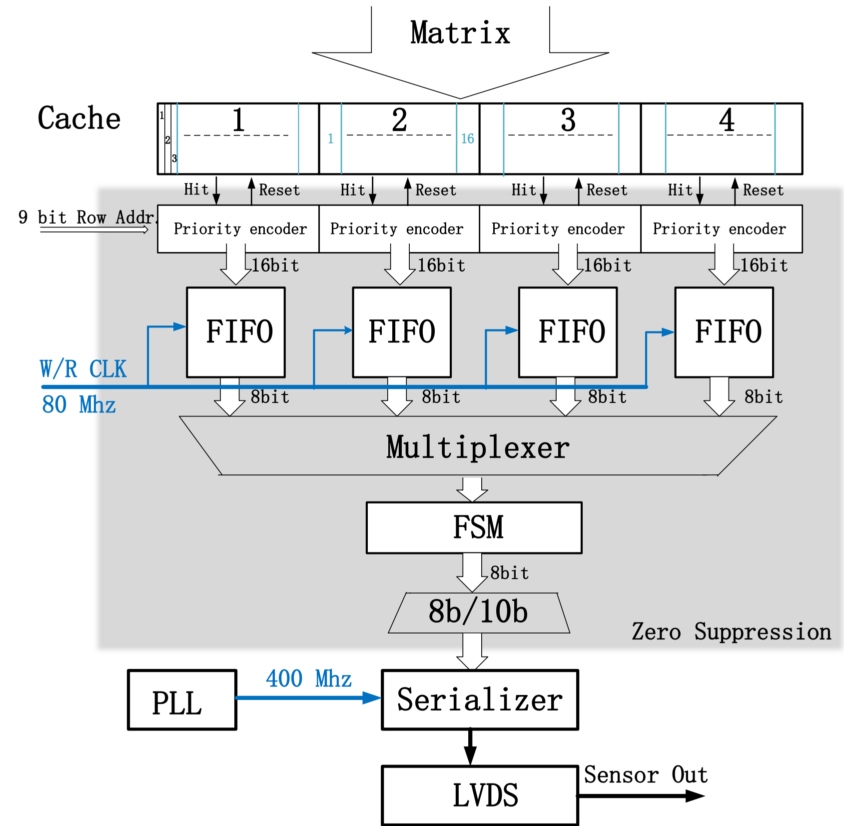


JadePix3: Periphery data processing

- Zero suppression at the end of column
  - Each 48 columns divided into 16 blocks
  - 'Fired' blocks identified sequentially by a 4-bit priority encoder
  - 12.5 ns * 16 blocks = 200 ns/row
- Only hit information fed into FIFO

Row #	Block #	hits in block
9-bit	4-bit	3-bit

  - FIFO R/W clk: 80 MHz
  - FIFO depth: 48
- Data stream steered by a Finite State Machine
- Data after 8b/10b: 800 Mbit/s
- Estimated Power consumption 76mW
  - 15mW (Zero suppression), 25mW (Serializer), 20mW (PLL), 16mW (LVDS)



CEPC

CPV4_3D: Readout mode

- Continuous readout
  - strobe == 1
  - Timing by falling edge ~1us
- Triggered readout
  - Strobe as gate signal
  - Timing by trigger ~5us