Development of high resolution low power silicon pixel sensors for the CEPC vertex detector

Qun Ouyang (IHEP)

On behalf of the study group
Outline:

♦ Introduction

♦ Updates on CPV3(SOI) and JadePix3(CMOS)

♦ Perspective for the next step

♦ Summary
**Introduction: requirements (CDR)**

- **On the pixel sensor for the efficient tagging of heavy quarks**
  - To achieve S.P. resolution
    - Digital pixel with in-pixel discriminator ~ 16 μm
    - Analog pixel ~ 20 μm (heavily rely on power pulsing as in the ILC)
  - To lower the material budget
    - Sensor thickness ~ 50 μm
    - Heat load < 50 mW/cm² constrained by air cooling
  - To tackle beam-related background
    - ~ μs level readout, 25 ns beam spacing @ Z-pole operation
    - 3.4 Mrad/year & $6.2 \times 10^{12} n_{eq}/ (cm^2 \cdot year)$

**Physics driven requirements**

<table>
<thead>
<tr>
<th>Coverage</th>
<th>Resolution $\sigma_{s.p.}$</th>
<th>Material budget 0.15% $X_0$/layer</th>
<th>Material budget 0.15% $X_0$/layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{s.p.}$</td>
<td>2.8um</td>
<td>0.15% $X_0$/layer</td>
<td>0.15% $X_0$/layer</td>
</tr>
</tbody>
</table>

**Running constraints**

- Air cooling
- Beam-related background
- Radiation damage

**Sensor specifications**

- Small pixel ~16 μm
- Thinning to 50 μm
- Low power 50 mW/cm²
- Fast readout ~1 μs
- Radiation tolerance
- ≤3.4 Mrad/year
- ≤$6.2 \times 10^{12} n_{eq}/ (cm^2 \cdot year)$

Overview of R&D activities

CMOS pixel sensor
- TowerJazz CIS 0.18 μm process
- Quadruple well process
- Thick (~20 μm) epitaxial layer
- with high resistivity (≥1 kΩ•cm)

SOI pixel sensor
- LAPIS 0.2 μm process
- High resistive substrate (≥1 kΩ•cm)
- Double SOI layers available
- Thinning and backside process

Towards Baseline Requirements: CMOS and SOI R&D in Synergy

Fine pitch
Low power frontend

Spatial resolution thinning
Analog power

CPV1/2/3 (SOI)
JadePix1/2/3 (CMOS)

Fast readout architecture

Readout speed
Digital power

MIC4 (CMOS)
Overview of R&D activities

CMOS pixel sensor
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Towards Baseline Requirements: CMOS and SOI R&D in Synergy

YP Lu, Development of the Silicon Tracker for CEPC, ICHEP2018, Seoul
### Overview of R&D activities (cont.)

<table>
<thead>
<tr>
<th>Year</th>
<th>SOI pixel</th>
<th>Double-SOI process</th>
<th>SOI-PDD process</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>CPV1</td>
<td>CVP2</td>
<td>CVP3</td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2020</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### SOI pixel
- **Compact Pixel for Vertex**
- **Double-SOI process**
  - CPV1
  - CVP2
  - CVP3
- **SOI-PDD process**
  - $6 \times 6 \text{ mm}^2$

#### HR-CMOS pixel
- **Tower-Jazz CiS process**
  - $3 \times 3 \text{ mm}^2$
  - JadePix1
  - JadePix2
  - JadePix3
  - MIC4
  - TaiChuPix1/2

#### Ladder and prototype
- **Single-sided ladder with MIMOSA28 sensors, 0.39\%X0/layer**
  - Double-sided prototype

#### References
- SOI-PDD process: $6 \times 6 \text{ mm}^2$
- Double-SOI process: CPV1, CVP2, CVP3
- Tower-Jazz CiS process: JadePix1, JadePix2, JadePix3, MIC4, TaiChuPix1/2
  - $3 \times 3.3 \text{ mm}^2$
  - $10.4 \times 6.1 \text{ mm}^2$
  - Fast readout, time stamp (25ns)

Another team

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July 30th ICHEP2020  Q.Ouyang  Pixel sensors for the CEPC vertex detector  6
CPV3: an novel design with SOI-PDD process

- **Pinned Depleted Diode** process proposed by Shoji Kawahito (Shizuoka U.)
  - Pinned Si surface layer $\rightarrow$ reduction of surface leakage by 2 orders
  - Depleted charge collection electrode $\rightarrow$ reduction of diode capacitance
  - Lateral electric field $\rightarrow$ improved charge collection efficiency

Ref: Sensors 2018, 18, 27; doi:10.3390/s18010027
CPV3 design

- Sensing node AC-coupled to the amplifier to allow $V_{bias}$ up to $+10V$
  - Minimize the capacitance at pixel pitch $16 \mu m \times 20 \mu m$
- Common Source (CS) amplifier, DC gain = 13
- Cascode stage + current source, discriminator
- Statistical simulation, FPN = $12 \ e^- * CPV2: 114 \ e^-$
- Mask area: $6mm \times 6mm$
  - Optimized for low FPN
  - Pixel matrix divided as 45 regions, to verify design options
  - Rolling shutter readout

Statistical simulation, FPN = $12 \ e^- * CPV2: 114 \ e^-$

Mask area: $6mm \times 6mm$
- Optimized for low FPN
- Pixel matrix divided as 45 regions, to verify design options
- Rolling shutter readout
Sensor tests

- Leakage current components
  - Dominated by the peripheral and bpw
  - Sum of sensing diode ~ nA
- $V_{\text{diode}} = +4V$ suppressed leakage on bpw and peripheral
  - Increased barrier potential

Calibration with $^{55}\text{Fe}$ X-ray

- $V_{\text{diode}} = +4V$, $V_{\text{bpw}} = 0V$, $V_{\text{back}} = -60V$
- Charge collected in a 3*3 cluster
- Wider peak spread of 5*5 cluster due to electrical noise
- Equivalent $C_d = 12fF$
Validation of $C_d$ reduction

- $V_{\text{back}}=-60\text{V}$, $V_{\text{bpw}}=0\text{V}$, increase $V_{\text{diode}}$
  - Proof of PDD bias concept
- Expected to be $4fF@4.4\text{V}$ + parasitic capacitance
  - Parasitic capacitance from the routing, AC capacitor and input transistor
  - Partially confirmed by RC extraction (simulation)

More tests to do

- Optimize the operation of pixel circuit
  - Compare different structures
- Noise and threshold measurement
- Laser test or beam test next year
  - the outcome of full characterization
  - and possible scheme together with CMOS sensor
JadePix3: fully functional prototype with small pixel design

- **Specification:**
  - Spatial resolution
    - ~ 3 μm
    - Initial pixel size 16 μm × 20 μm
    - FPN < 20e-
  - Power consumption
    - < 100mW/cm²
    - Measureable

- **Rolling shutter readout**
  - 512 row ×192 col
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Encoder at the end of columns.
JadePix3: Diode & Front-end design

- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 \( \mu m^2 \), with a small footprint 36 \( \mu m^2 \)
- Frontend: tradeoff between layout area and FPN
  - Reduction on the layout area, \( \sim 200 \mu m^2 \)
  - Improvement on the FPN = 3.1e\(^{-}\) (simulation)
  - A low power version (20nA), equivalent to 9 mW/cm\(^2\)

![Diode & Front-end design diagram]

- Amplification
- Discrimination

![Amplification and Discrimination schematic]

- Mismatch: \( \mu = 138.1 e^- \)
  - \( \sigma = 3.1 e^- \)

![Mismatch distribution graph]

Electrode footprint: 16 \( \mu m \) x 16 \( \mu m \)
### JadePix3: chip status

- Submitted in Oct. 2019
- Process finished in May 2020
- Diode, minimum size
  \[ S_{\text{diode}} = 4 \mu m^2, \quad S_{\text{footprint}} = 36 \mu m^2, \quad C_{\text{diode}} \approx 4-5 fF \]
- Front-end, 2 versions
  - FE_V0, FE_V1 (20nA, 60nA)
- Pixel digital, 3 versions
  - DGT_V0, DGT_V1, DGT_V2
- Pixel area
  - \( 16 \times 26 \mu m^2 \)
  - \( 16 \times 23.11 \mu m^2 \)

Estimated: \( \sim 55 mW/cm^2 \):
- \( 9 mW/cm^2 \) (pixel array)
- \( 30 mW/cm^2 \) (zero suppression & data buffer)
- \( 6.25 mW/cm^2 \) (Serializer)
- \( 5 mW/cm^2 \) (PLL)
- \( 4 mW/cm^2 \) (LVDS)

### Test plan

- **May - Aug. 2020**
  - Sub-board to mount the chip into readout system
  - Readout system debugging
- **Sep. 2020 - Feb. 2021**
  - Characterization of individual parts on chip
  - Optimization of operation
  - \( ^{55}Fe \) 5.9 keV X-ray calibration
- Sometime in 2021
  - Beam test

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<table>
<thead>
<tr>
<th>Sector</th>
<th>Diode</th>
<th>Front-end</th>
<th>Pixel digital</th>
<th>Pixel layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2 + 2 ( \mu m )</td>
<td>FE_V0</td>
<td>DGT_V0</td>
<td>( 16 \times 26 \mu m^2 )</td>
</tr>
<tr>
<td>1</td>
<td>2 + 2 ( \mu m )</td>
<td>FE_V0</td>
<td>DGT_V1</td>
<td>( 16 \times 26 \mu m^2 )</td>
</tr>
<tr>
<td>2</td>
<td>2 + 2 ( \mu m )</td>
<td>FE_V0</td>
<td>DGT_V2</td>
<td>( 16 \times 23.11 \mu m^2 )</td>
</tr>
<tr>
<td>3</td>
<td>2 + 2 ( \mu m )</td>
<td>FE_V1</td>
<td>DGT_V0</td>
<td>( 16 \times 26 \mu m^2 )</td>
</tr>
</tbody>
</table>
Perspective for the R&D of next few years

Design parameters of the CEPC vertex system in CDR

| Layer | R (mm) | |Z| (mm) | σ (μm) | material budget |
|-------|--------|----------|-------|--------|----------------|
| Layer 1 | 16     | 62.5     | 2.8   | 0.15%/X_0 |
| Layer 2 | 18     | 62.5     | 6     | 0.15%/X_0 |
| Layer 3 | 37     | 125.0    | 4     | 0.15%/X_0 |
| Layer 4 | 39     | 125.0    | 4     | 0.15%/X_0 |
| Layer 5 | 58     | 125.0    | 4     | 0.15%/X_0 |
| Layer 6 | 60     | 125.0    | 4     | 0.15%/X_0 |

- Optimization for system requirements: resolution, radiation level, Z-pole operation mode, ...
- Development of CMOS sensors with fast readout and time stamp
- Exploration of new process
  - 3D process \(\rightarrow\) SOI-3D accessible via SOIPIX
  - Ultra-light, self-supported layers with stitching CMOS sensors
SOI based 3D integration

SOFIST

Miho Yamada, 3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment, IEEE 3DIC, Sendai, October 8th, 2019

Connection yield > 99.9%

T-Micro process
Development of SOI-3D chip for CEPC

- Faster and low power
  - Timing ~ 1us, hit registered at the fast falling edge
  - Power consumption ~ 50mW/cm²
  - Shrink the pixel size by SOI-3D
- Continuous readout mode (AERD)
  - Compatible with trigger mode
- CPV4_3D submission plan ~Nov.2020

Output Waveform of Discriminator

- Faster and low power
  - Timing ~ 1us, hit registered at the fast falling edge
  - Power consumption ~ 50mW/cm²
  - Shrink the pixel size by SOI-3D

Continuous readout mode (AERD)

- Compatible with trigger mode

CPV4_3D submission plan ~Nov.2020
ALICE ITS3 with stitching CMOS technology

- New beam pipe:
  - “old” radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm

- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)

- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

<table>
<thead>
<tr>
<th>Beam pipe Inner/Outer Radius (mm)</th>
<th>16.0/16.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB Layer Parameters</td>
<td>Layer 0</td>
</tr>
<tr>
<td>Radial position (mm)</td>
<td>18.0</td>
</tr>
<tr>
<td>Length (sensitive area) (mm)</td>
<td>300</td>
</tr>
<tr>
<td>Pseudo-rapidity coverage</td>
<td>±2.5</td>
</tr>
<tr>
<td>Active area (cm²)</td>
<td>610</td>
</tr>
<tr>
<td>Pixel sensor dimensions (mm²)</td>
<td>280 x 56.5</td>
</tr>
<tr>
<td>Number of sensors per layer</td>
<td>2</td>
</tr>
<tr>
<td>Pixel size (µm²)</td>
<td>0 (10 x 10)</td>
</tr>
</tbody>
</table>

Similar layout with CEPC layer 1-3

M. Mager | ITS3 | VERTEX 2019 | 17.10.2019 | 14
An ultra light structure vertex layout

| Layer | R (mm) | |Z| (mm) | \( \sigma (\mu m) \) (layout1/layout2) | Material budget |
|-------|-------|---------|-------|----------------------------------------|-----------------|
| Layer 1 | 16   | 62.5    | 4/2.8 | 0.05%\( X_0 \)                        |
| Layer 2 | 24   | 62.5    | 4/4   | 0.05%\( X_0 \)                        |
| Layer 3 | 32   | 125     | 4/4   | 0.05%\( X_0 \)                        |
| Layer 4 | 40   | 125     | 4/4   | 0.05%\( X_0 \)                        |
| Layer 5 | 50   | 125     | 4/4   | 0.05%\( X_0 \)                        |
| Layer 6 | 60   | 125     | 4/4   | 0.05%\( X_0 \)                        |

Comparing with baseline layout
- better performance (~20% improvement) for layout1 at low momentum, but poor performance at high momentum
- both within the requirement

- Technology to be explored with 55 nm CiS process
- Joint effort of CCNU and IHEP

ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop, Nov.2019, Beijing
Summary

- Stringent requirements for CEPC vertex detector have driven R&D programs
- CMOS and SOI development in synergy
  - Following the same roadmap
  - Using the same readout system
- JadePix3 and CPV3 produced, and tests underway in parallel
- CPV4_3D design is ongoing, and stitching CMOS technology will be explored
- A Pixel Vertex prototype being built (to be finished in 2023) but it was not covered in this talk

![Diagram](image-url)
Thank you for your attention!
Backup
## Updated Parameters of Collider Ring since CDR

<table>
<thead>
<tr>
<th></th>
<th>Higgs</th>
<th>Z (2T)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Beam energy (GeV)</strong></td>
<td>CDR: 120</td>
<td>Updated: -</td>
</tr>
<tr>
<td></td>
<td>CDR: 45.5</td>
<td>Updated: -</td>
</tr>
<tr>
<td><strong>Synchrotron radiation loss/turn (GeV)</strong></td>
<td>CDR: 1.73</td>
<td>Updated: 1.68</td>
</tr>
<tr>
<td></td>
<td>CDR: 0.036</td>
<td>Updated: -</td>
</tr>
<tr>
<td><strong>Pionwski angle</strong></td>
<td>CDR: 2.58</td>
<td>Updated: 3.78</td>
</tr>
<tr>
<td></td>
<td>CDR: 23.8</td>
<td>Updated: 33</td>
</tr>
<tr>
<td><strong>Number of particles/bunch N_e (10^{10})</strong></td>
<td>CDR: 15.0</td>
<td>Updated: 17</td>
</tr>
<tr>
<td></td>
<td>CDR: 8.0</td>
<td>Updated: 15</td>
</tr>
<tr>
<td><strong>Bunch number (bunch spacing)</strong></td>
<td>CDR: 242 (0.68μs)</td>
<td>Updated: 218 (0.68μs)</td>
</tr>
<tr>
<td></td>
<td>CDR: 12000</td>
<td>Updated: 15000</td>
</tr>
<tr>
<td><strong>Beam current (mA)</strong></td>
<td>CDR: 17.4</td>
<td>Updated: 17.8</td>
</tr>
<tr>
<td></td>
<td>CDR: 461.0</td>
<td>Updated: 1081.4</td>
</tr>
<tr>
<td><strong>Synchrotron radiation power/beam (MW)</strong></td>
<td>CDR: 30</td>
<td>Updated: -</td>
</tr>
<tr>
<td></td>
<td>CDR: 16.5</td>
<td>Updated: 38.6</td>
</tr>
<tr>
<td><strong>Cell number/cavity</strong></td>
<td>CDR: 2</td>
<td>Updated: -</td>
</tr>
<tr>
<td></td>
<td>CDR: 2</td>
<td>Updated: 1</td>
</tr>
<tr>
<td><em><em>β function at IP β_x</em>/β_y</em> (m)**</td>
<td>CDR: 0.36/0.0015</td>
<td>Updated: 0.33/0.001</td>
</tr>
<tr>
<td></td>
<td>CDR: 0.2/0.001</td>
<td>Updated: -</td>
</tr>
<tr>
<td><strong>Emittance ε_x/ε_y (nm)</strong></td>
<td>CDR: 1.21/0.0031</td>
<td>Updated: 0.89/0.0018</td>
</tr>
<tr>
<td></td>
<td>CDR: 0.18/0.0016</td>
<td>Updated: -</td>
</tr>
<tr>
<td><strong>Beam size at IP σ_x/σ_y (μm)</strong></td>
<td>CDR: 20.9/0.068</td>
<td>Updated: 17.1/0.042</td>
</tr>
<tr>
<td></td>
<td>CDR: 6.0/0.04</td>
<td>Updated: -</td>
</tr>
<tr>
<td><strong>Bunch length σ_z (mm)</strong></td>
<td>CDR: 3.26</td>
<td>Updated: 3.93</td>
</tr>
<tr>
<td></td>
<td>CDR: 8.5</td>
<td>Updated: 11.8</td>
</tr>
<tr>
<td><strong>Lifetime (hour)</strong></td>
<td>CDR: 0.67</td>
<td>Updated: 0.22</td>
</tr>
<tr>
<td></td>
<td>CDR: 2.1</td>
<td>Updated: 1.8</td>
</tr>
<tr>
<td><strong>Luminosity/Ip L (10^{34} cm^{-2}s^{-1})</strong></td>
<td>CDR: 2.93</td>
<td>Updated: 5.2</td>
</tr>
<tr>
<td></td>
<td>CDR: 32.1</td>
<td>Updated: 101.6</td>
</tr>
</tbody>
</table>

**Luminosity increase factor:**

- Higgs: $\times 1.8$
- Z (2T): $\times 3.2$
Br(H→bb, cc) measurement

- Br (H → cc) is extremely sensitive to the vertex design
- Br (H → bb) is not really sensitive to the vertex design

<table>
<thead>
<tr>
<th>Scenario A (Aggressive)</th>
<th>Scenario B (Baseline)</th>
<th>Scenario C (Conservative)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material per layer/X₀</td>
<td>0.075</td>
<td>0.15</td>
</tr>
<tr>
<td>Spatial resolution/µm</td>
<td>1.4 - 3</td>
<td>2.8 - 6</td>
</tr>
<tr>
<td>R_{in}/mm</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>

\[ \sigma_{SP} < 2.8 \, \mu m \text{ very difficult} \]

Z. Wu, et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002

Table 4. Maximum \( \epsilon \cdot p \) value comparison for the Br(H → b\bar{b}) measurement.

<table>
<thead>
<tr>
<th>Scenario A</th>
<th>Scenario B</th>
<th>Scenario C</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \epsilon \cdot p )</td>
<td>0.133 ± 0.002</td>
<td>0.095 ± 0.001</td>
</tr>
</tbody>
</table>

\[ \text{41\%} \quad \text{-22\%} \]

\[ \epsilon \cdot p = 0.095(1 - 0.14 \frac{\Delta x_{\text{material}}}{x_{\text{material}}})(1 - 0.09 \frac{\Delta x_{\text{resolution}}}{x_{\text{resolution}}})(1 - 0.23 \frac{\Delta x_{\text{radius}}}{x_{\text{radius}}}) \]

ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop Nov.2019
Same layout as in CDR

- $\sigma_{sp} = 4\,\mu m$ for L1 and L2
- $\sigma_{sp} = 3\,\mu m$ for combination of L3 and L4, and combination of L5 and L6

![Graph showing dependencies between $\sigma_{sp}$ and absolute momentum $p$.

- Full simulation ($\theta = 85^\circ$)
- Fast simulation ($\theta = 85^\circ$)
- Fast 3 layers ($\theta = 85^\circ$)
- Fast 4 layers ($\theta = 85^\circ$)
- Requirement ($\theta = 85^\circ$)
JadePix3: Periphery data processing

- Zero suppression at the end of column
  - Each 48 columns divided into 16 blocks
  - ‘Fired’ blocks identified sequentially by a 4-bit priority encoder
  - 12.5 ns * 16 blocks = 200 ns/row
- Only hit information fed into FIFO

<table>
<thead>
<tr>
<th>Row #</th>
<th>Block #</th>
<th>hits in block</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-bit</td>
<td>4-bit</td>
<td>3-bit</td>
</tr>
</tbody>
</table>

- FIFO R/W clk: 80 MHz
- FIFO depth: 48
- Data stream steered by a Finite State Machine
- Data after 8b/10b: 800 Mbit/s
- Estimated Power consumption 76mW
  - 15mW (Zero suppression), 25mW (Serializer), 20mW (PLL), 16mW (LVDS)
CPV4_3D: Readout mode

- **Continuous readout**
  - strobe == 1
  - Timing by falling edge ~1us

- **Triggered readout**
  - Strobe as gate signal
  - Timing by trigger ~5us

![Diagram showing readout modes with waveforms for pixel_out1, pixel_out2, strobe, grst, valid, read, freeze, sync, and addr<3:0> with time stamps 1 and 2.]