Development of high resolution low power silicon pixel sensors for the CEPC vertex detector

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The Circular Electron Positron Collider (CEPC) has been proposed as a Higgs/Z0 (flavor) factory, which would allow precision measurements of the Higgs boson properties, as well as of $W\pm/Z0$ bosons. The baseline design of CEPC vertex system consists of three concentric double-sided pixel layers, to reach the unprecedented impact parameter resolution. Driven by physics studies and experimental conditions, the silicon pixel sensor of vertex system has similar performance requirements to that of ILC detectors, such as a single point resolution of around 3μ m, very low material budget of 0.15%X0 per single layer and power consumption of below 50mW/cm2, but without power-pulsing, which leads to significantly additional constrains on detector specifications, especially for the case of machine operating at Z-pole energy region with high luminosity. In this presentation, I will give an overview of the conceptual design, the requirements and challenges for the CEPC vertex system. The on-going R&D activities will be mainly reported, based on monolithic CMOS pixel sensor (CPS) and Silicon on Insulator (SOI) pixel sensor technologies, for the purpose of development of high resolution and low power consumption pixel sensors. To reach the target, several CMOS and SOI pixel prototypes with small pitch ('20µm) and digital readout are explored. Recent R&D achievements will be presented, and the prospects of future R&D with novel stitching and 3D sensor technologies will also be shown.

Secondary track (number)

Author: Prof. OUYANG, Qun (Institute of High Energy Physics, Chinese Academy of Sciences)

Co-authors: Dr ZHOU, Yang (Institute of High Energy Physics, Chinese Academy of Sciences); Dr ZHANG, Ying (Institute of High Energy Physics, Chinese Academy of Sciences); Dr YANG, Ping (Central Chinese Normal University); Dr LU, Yunpeng (Institute of High Energy Physics, Chinese Academy of Sciences)

Presenter: Prof. OUYANG, Qun (Institute of High Energy Physics, Chinese Academy of Sciences)

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