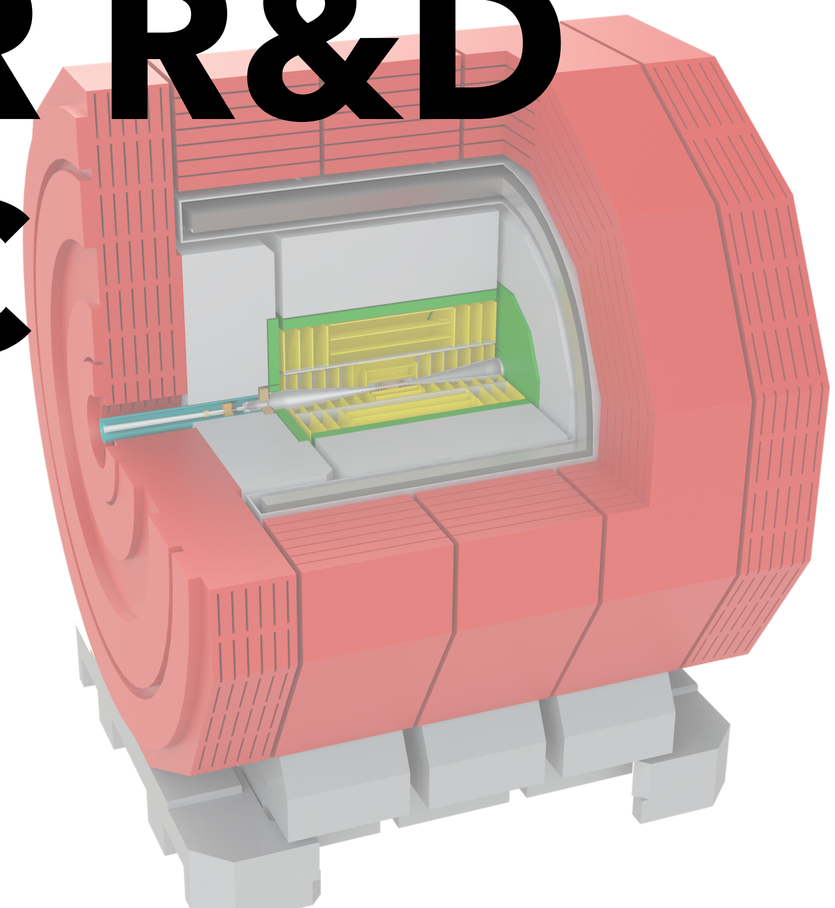
SILICON VERTEX AND TRACKER R&D FOR CLIC



ICHEP 2020

31/07/2020

Katharina Dort
CERN & University of Giessen
On behalf of the CLICdp collaboration

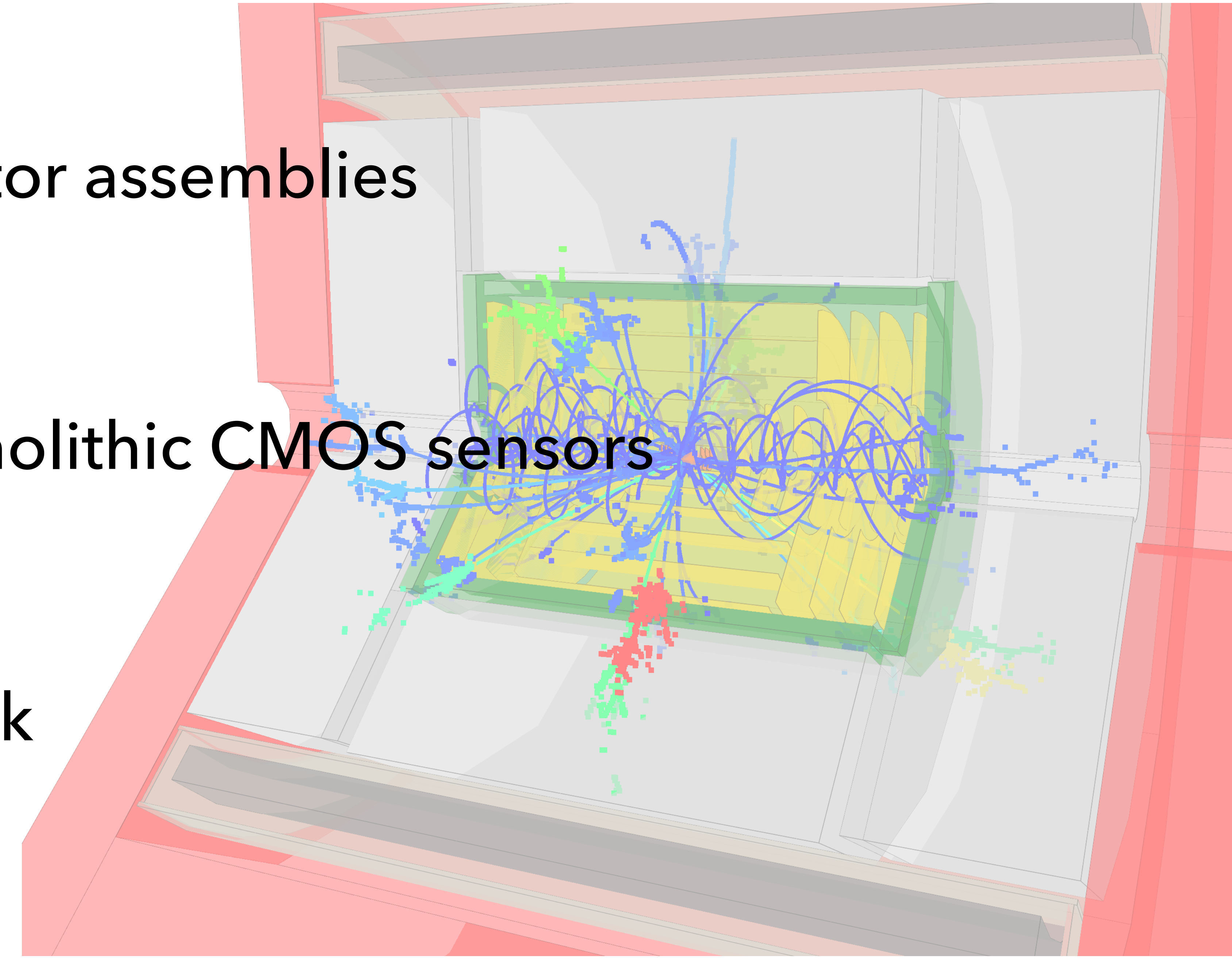
OVERVIEW

The Compact Linear Collider (CLIC)

Hybrid pixel-detector assemblies

Fully depleted monolithic CMOS sensors

Summary & Outlook

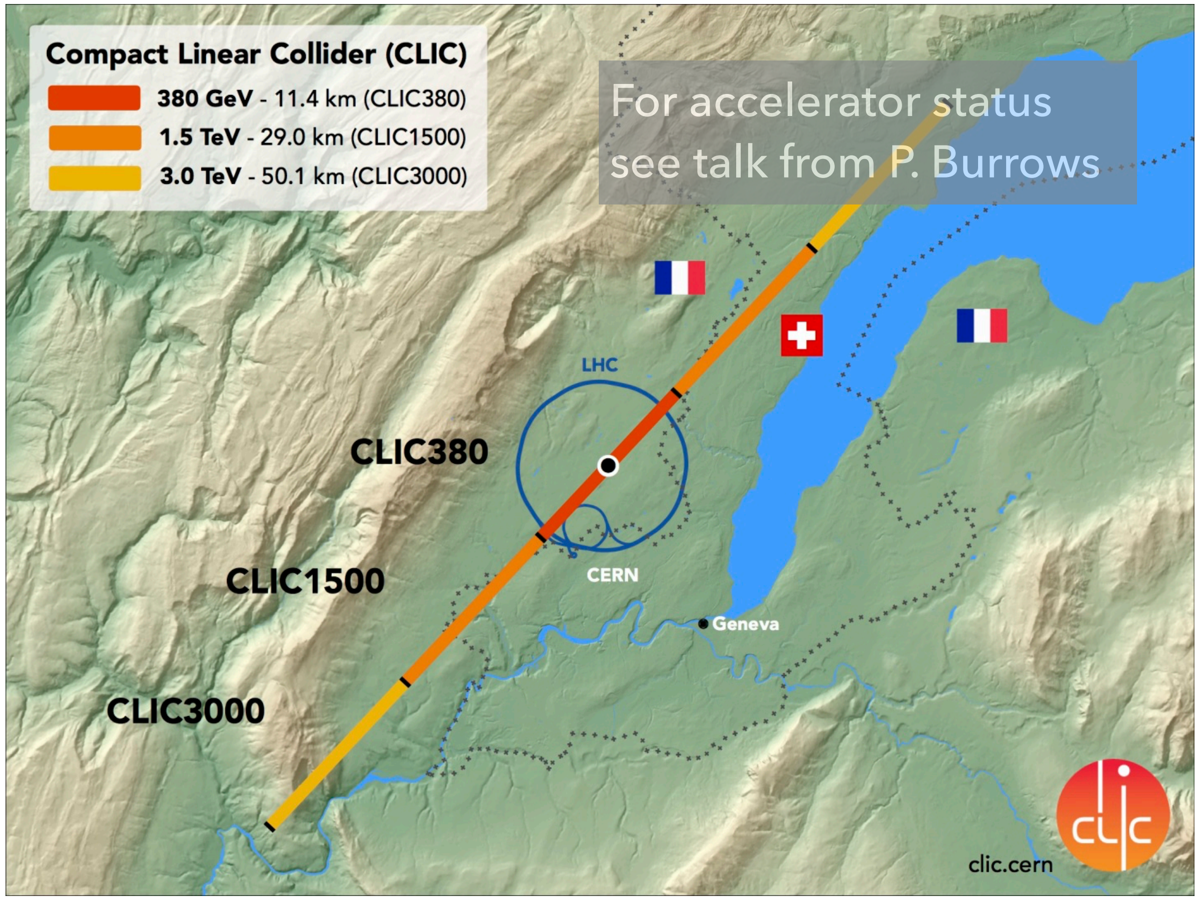


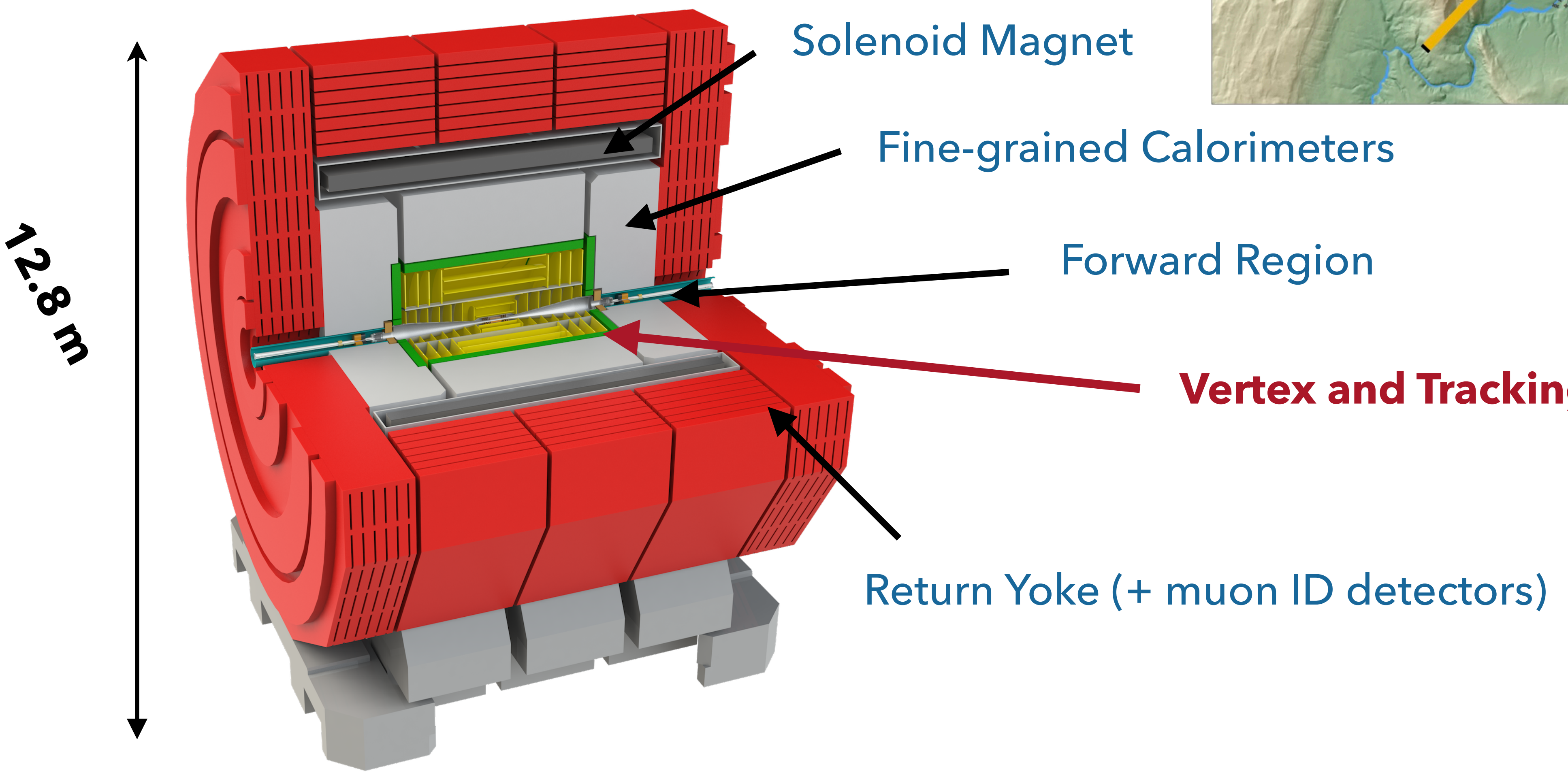
THE COMPACT LINEAR COLLIDER

- Concept for post-LHC linear electron-positron collider at CERN built in three energy stages (380 GeV -> 3 TeV)

- **Highlights of physics program**: precision SM Top and Higgs + BSM

  See talks from P. Roloff and M. Weber





CLIC 2018 Summary Report, CERN-2018-005

REQUIREMENTS FOR VERTEX AND TRACKING DETECTORS

- Triggerless readout
- Heavy quark tagging through precise determination of displaced vertices
- Momentum resolution: $\frac{\sigma(p_T)}{p_T^2} \approx 2 \times 10^{-5}\,\text{Gev}^{-1}$

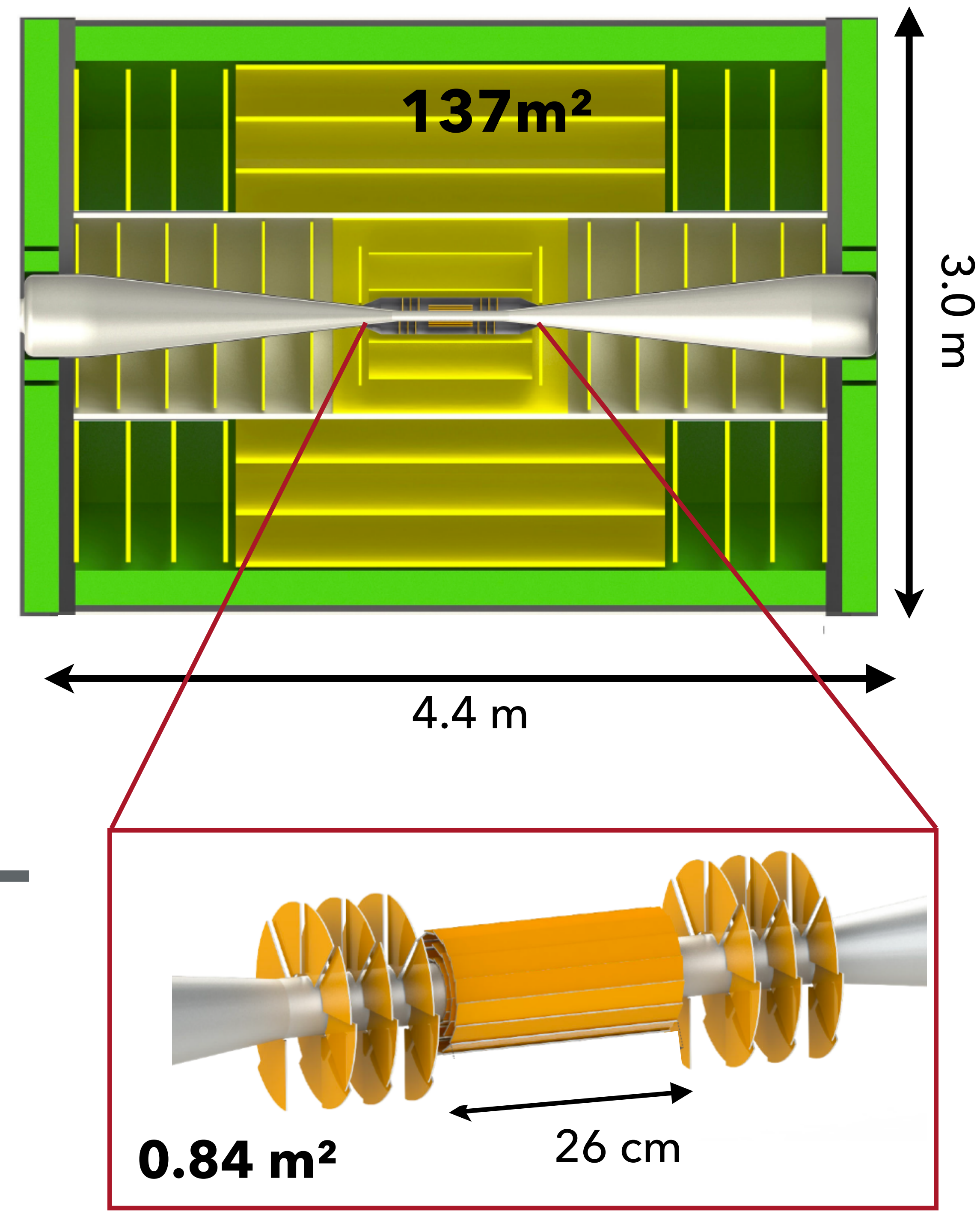
➡ Synergies with HL-LHC experiments, ILC, circular Higgs factories -> R&D beyond CLIC experiment

- Strategic R&D programme on technology for future experiments launched beginning of 2020

EP R&D

See talk from E. Rivera

	Vertex Detector	Tracking Detector
Timing resolution	5 ns	5 ns
Single point resolution	~3 µm	~7 µm
Hit detection efficiency	> 99.7%	> 99.7%
Material budget per layer	~0.2% X0	1-2% X0
Average power consumption (after power-pulsing*)	50 mW/cm²	150 mW/cm²
Radiation tolerance	$< 10^{11}\text{neq/cm}^2$	$< 10^{11}\text{neq/cm}^2$



Detector technologies for CLIC, CERN-2019-001

*more details in back-up

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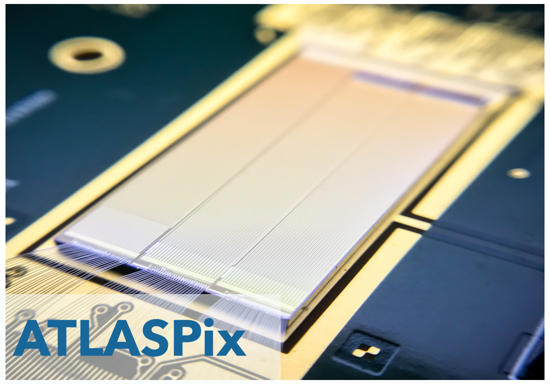
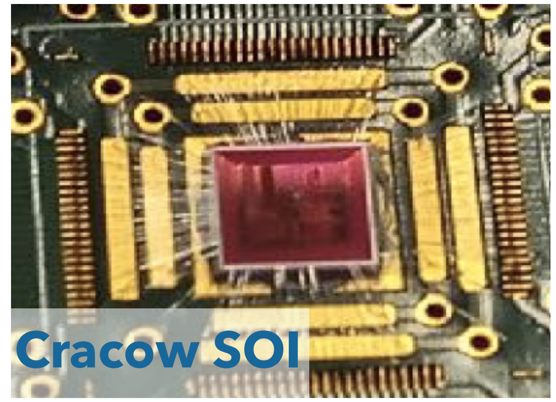
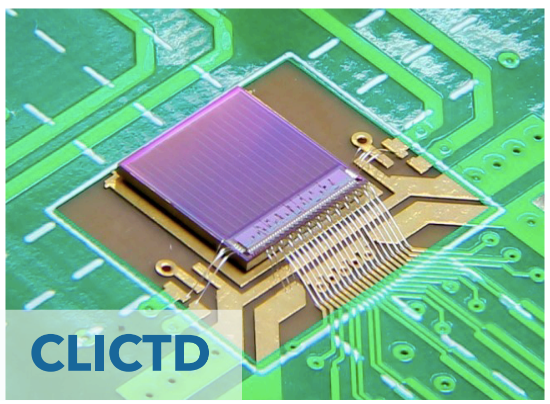
CLIC SILICON PIXEL DETECTOR R&D

Monolithic

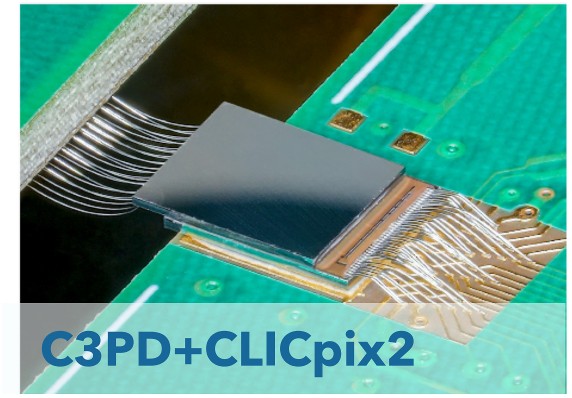

ATLASPix


Cracow SOI


CLICTD

Monolithic sensors with large (HV-CMOS) and small (HR-CMOS) collection electrodes are investigated

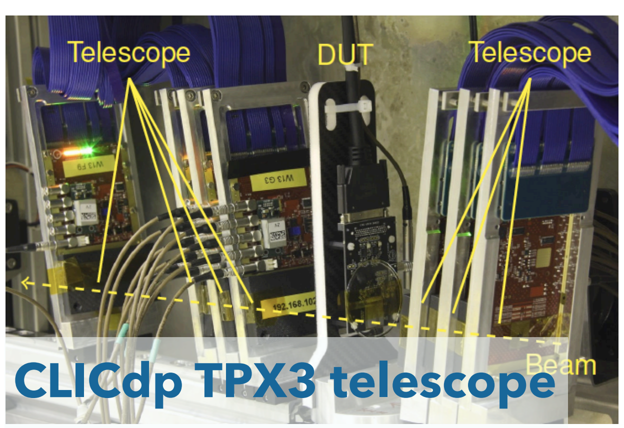
Hybrid


C3PD+CLICpix2

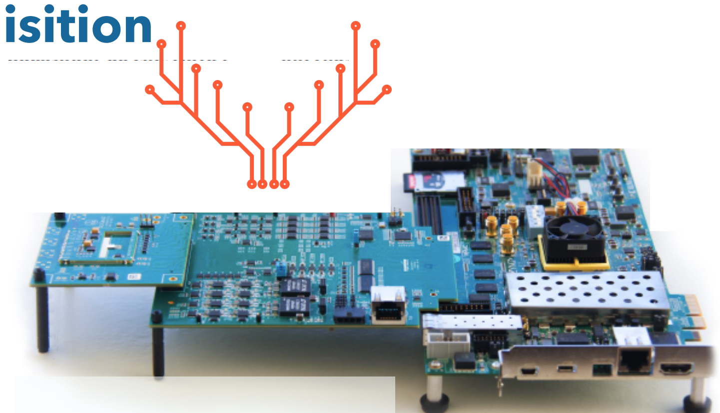
Different interconnection technologies, sensor and ASIC development


CLICpix2 + planar sensor

Beam Tests and Data Acquisition

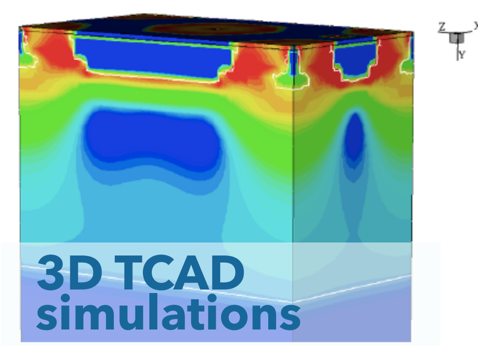


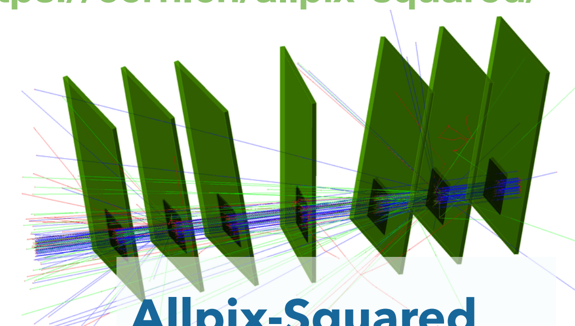
CLICdp TPX3 telescope


Caribou Versatile DAQ
https://gitlab.cern.ch/Caribou

Simulations

https://cern.ch/allpix-squared/


3D TCAD simulations


Allpix-Squared MC simulations

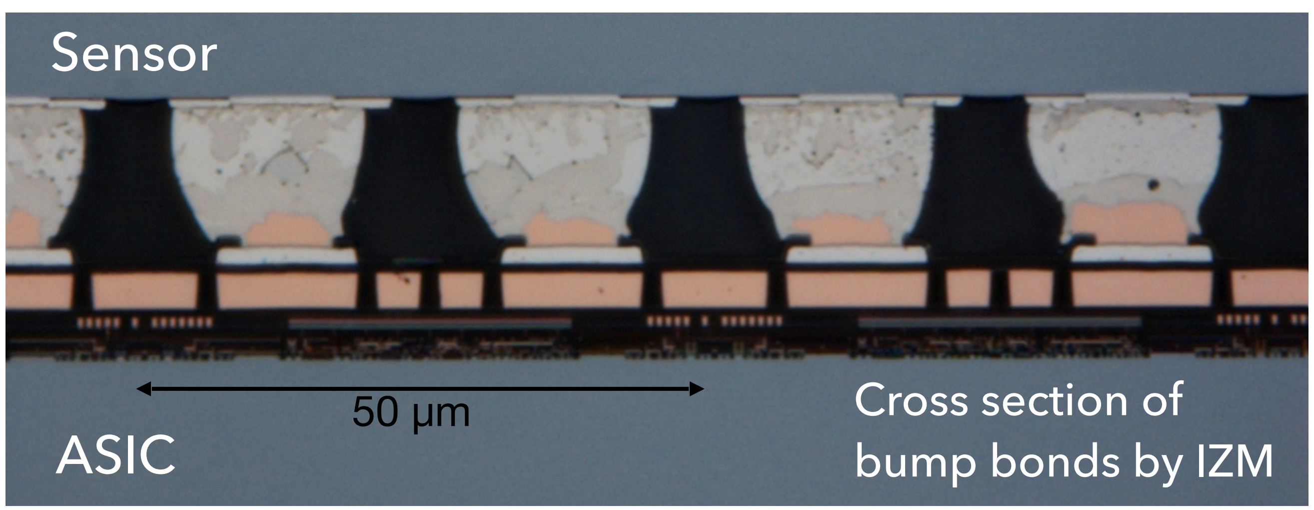
Mechanics (air cooling, light-weight supports), detector assembly

Detector technologies for CLIC, CERN-2019-001

HYBRID FINE-PITCH PIXEL DETECTOR

CLICpix2 readout ASIC:

- 65 nm CMOS process
- Pixel pitch 25 µm x 25 µm (128 x 128 pixels)
- Bump-bonded to planar silicon sensors of thickness 50 µm - 200 µm
- Simultaneous 5-bit ToT + 8-bit ToA readout
- Part of Timepix/Medipix family

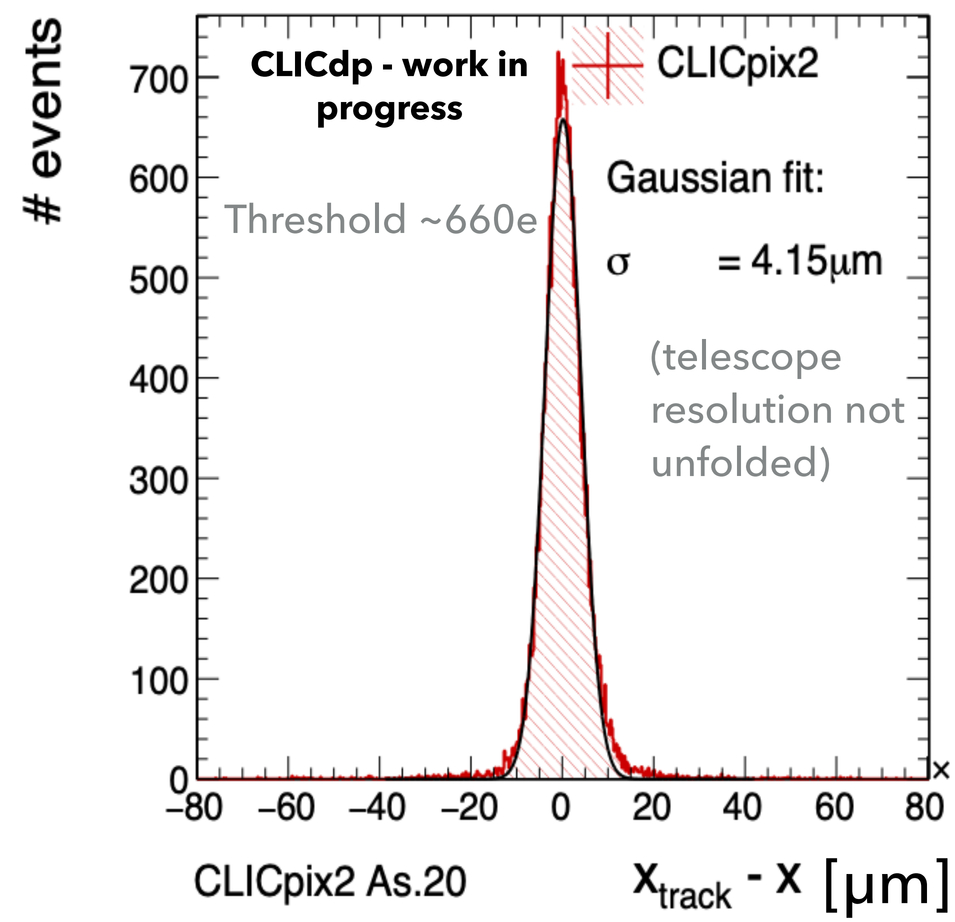


- Challenging single-chip bump-bonding process with pixel pitch of 25 µm performed by IZM
- Interconnect yield of up to 99.6% found in laboratory testing (test-pulse, source, etc.)

JINST, 15(03), C03045

- Positional resolution of ~3.2 µm for sensor thickness of 130 µm (too thick for vertex detector)
- Resolution degrades for thinner sensors
- Timing resolution of ~4 ns
- Hit detection efficiency up to 99.97%

Designed to meet requirements of CLIC vertex detector



- Low yield of well-connected assemblies
- Alternative inter-connection technologies* are investigated https://indico.cern.ch/event/858640/

*more details in back-up

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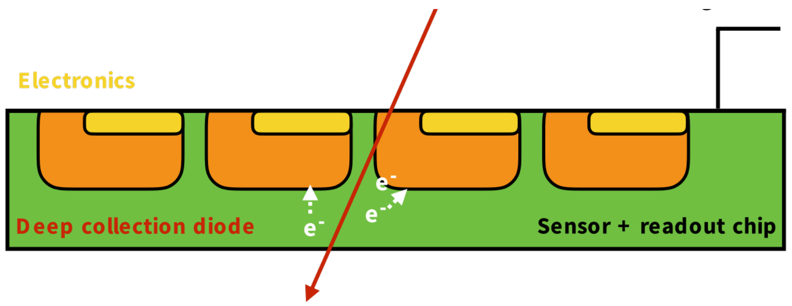
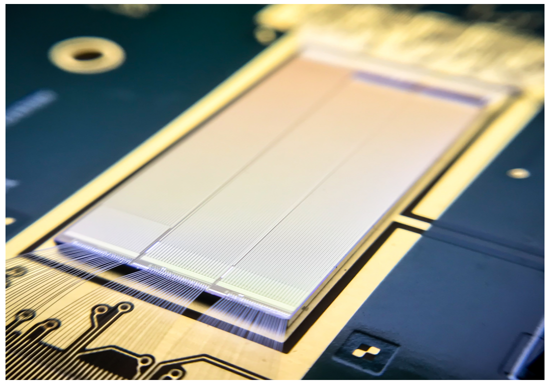
MONOLITHIC SENSOR TECHNOLOGIES

High-Voltage (HV) CMOS MAPS

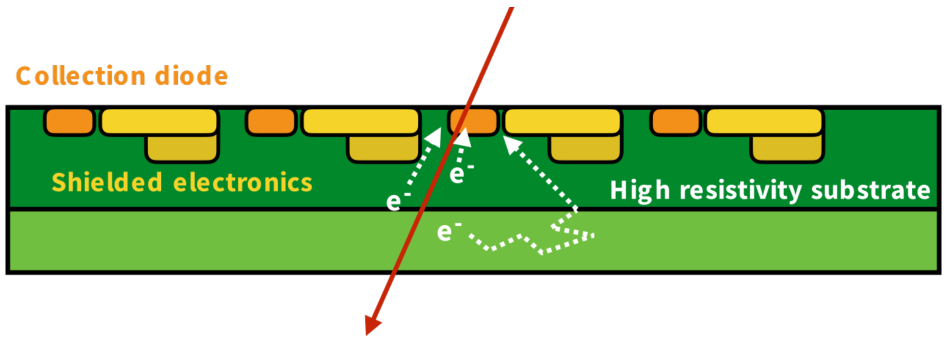


- **Large collection diode**
- High bias voltage of up to O(100V)
    - Large depleted volume and high electric field
    - Fast charge collection via drift

ATLASpix_simple



High-Resistivity (HR) CMOS MAPS

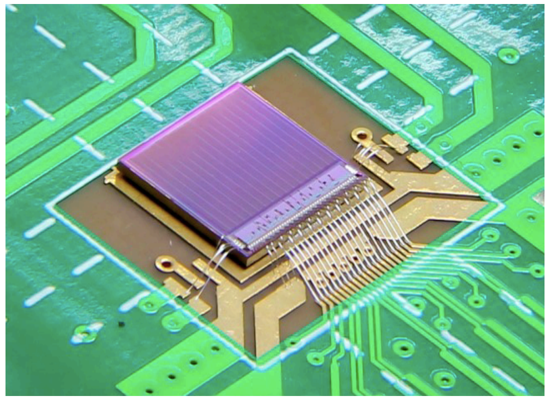


- **Small collection diode**

  ➡ Complex inhomogeneous field inside the sensor

- Low sensor capacitance
    - High signal to noise ratio
    - Low power consumption

CLICTD



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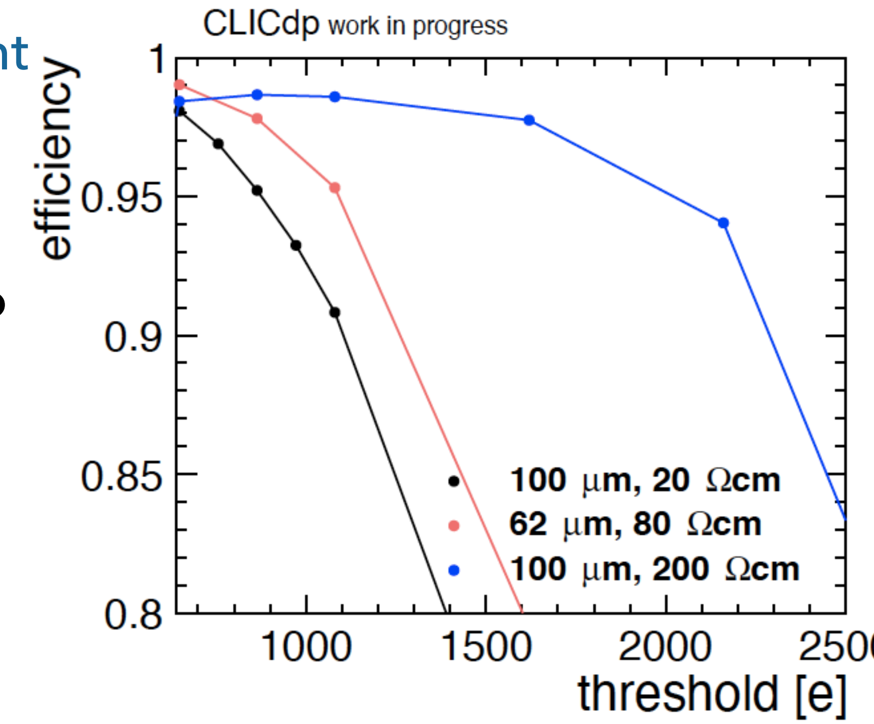
LARGE COLLECTION ELECTRODE CMOS

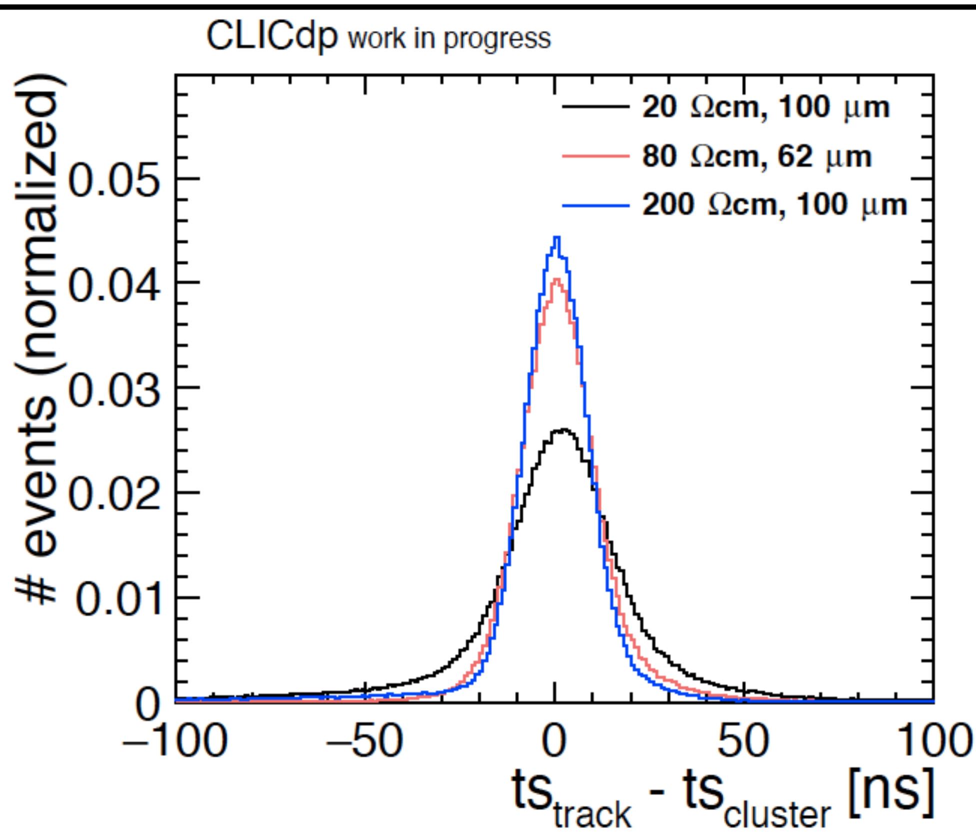
HV CMOS ATLASpix:

ATLAS EXPERIMENT

- High-voltage monolithic active pixel sensor
- Pixel pitch 130 μm x 40 μm (25 x 400 pixels)
- Designed for ATLAS ITk upgrade with CLIC requirements
- Simultaneous 6- bit ToT + 10-bit ToA readout (8 ns bins)

- Larger resistivity increases efficient operation window due to
  - Larger depleted volume (depletion depth < 20 μm) leading to higher signal/noise ratio
  - Increased electric field leading to less charge sharing
- Efficiencies >99% achievable





- Larger resistivity increases timing resolution
- Best result after time walk correction: $\sigma_{\text{Gauss}} = 6.8$ ns

  (200 Ωcm, 100 μm, bias voltage = -50 V, threshold = 480 e-)
- Outlook: New submission with modified pixel layout to improve spatial resolution
  - Common development with LHCb and CEPC

➡ First measurement results are expected this autumn/ winter

CLICdp-Conf-2020-005

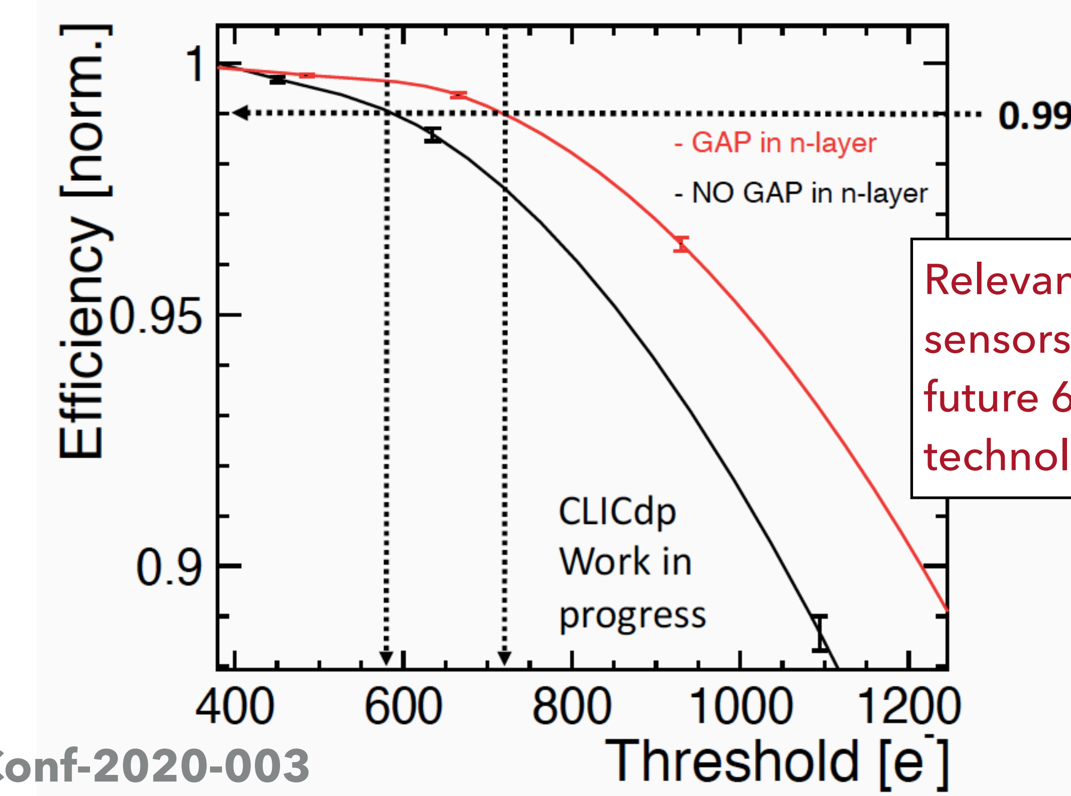
SMALL COLLECTION ELECTRODE CMOS

CLICTD:

- 180 nm CMOS imaging process
- Channel pitch: 300 μm x 30 μm (16x128 channels)
- Sub-pixel pitch: 37.5 μm x 30.0 μm
- Analogue front-end of 8 sub-pixels are grouped together in one digital front-end (= detector channel)
- Frame-based readout with 40 MHz
- 8-bit ToA (10 ns ToA bins) + 5-bit ToT (combined ToA/ToT for every 8 sub-pixels in 300μm dimension)

- Full lateral depletion in 30 μm epitaxial layer
- Gap in n-type implant in beam direction:
  - Speed up of charge collection
  - Improved timing resolution
  - Reduced charge sharing

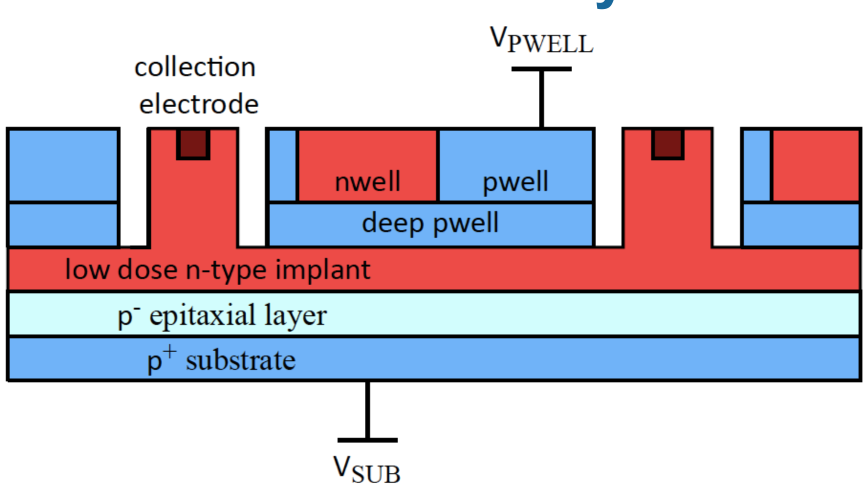
- Spatial resolution: ~ 5.5 μm (after standard eta-correction)
  - Timing resolution: ~ 6 ns (after time-walk correction)
    - Hit detection efficiency: > 99.8% (up to 400 e-)



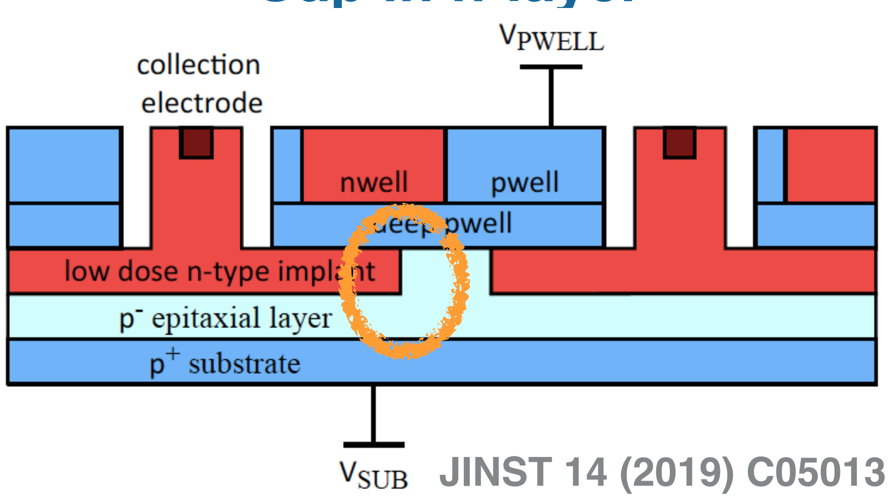
Relevant for thin sensors (e.g. in future 65 nm CMOS technology)

CLICdp-Conf-2020-003

Continuous n-layer



Gap in n-layer



JINST 14 (2019) C05013

SENSOR TIMING SIMULATIONS

- Sensor simulations from 3D TCAD (electrostatic field, weighting field, doping concentration) are imported into MC framework Allpix-Squared:
  - High statistics + accurate sensor modeling

NIM A 964 (2020) 163784

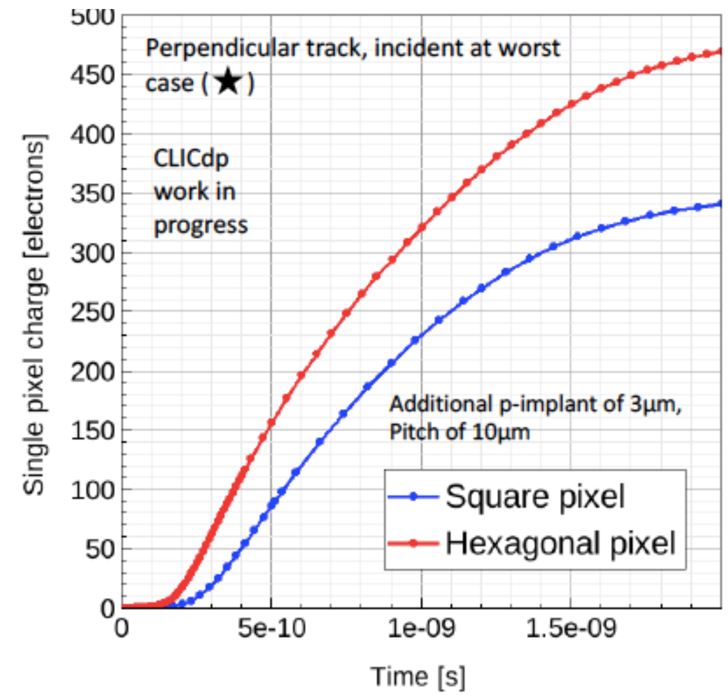
https://cern.ch/allpix-squared/

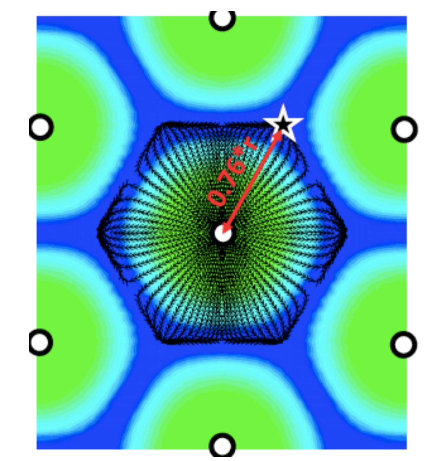
NIM A 901 (2018) 164-172

- In pixel timing resolution plots show optimized timing performance for modified pixel designs
- Optimization studies are essential for future sensor design in CMOS 65 nm technology

Outlook: ATTRACT FastPix (Hexagonal pixel design)

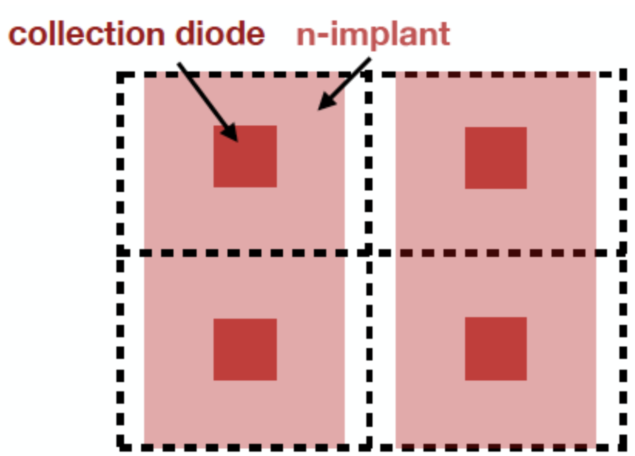
- Reduce minimal distance to collection diodes
- Reduce number of nearest neighbors





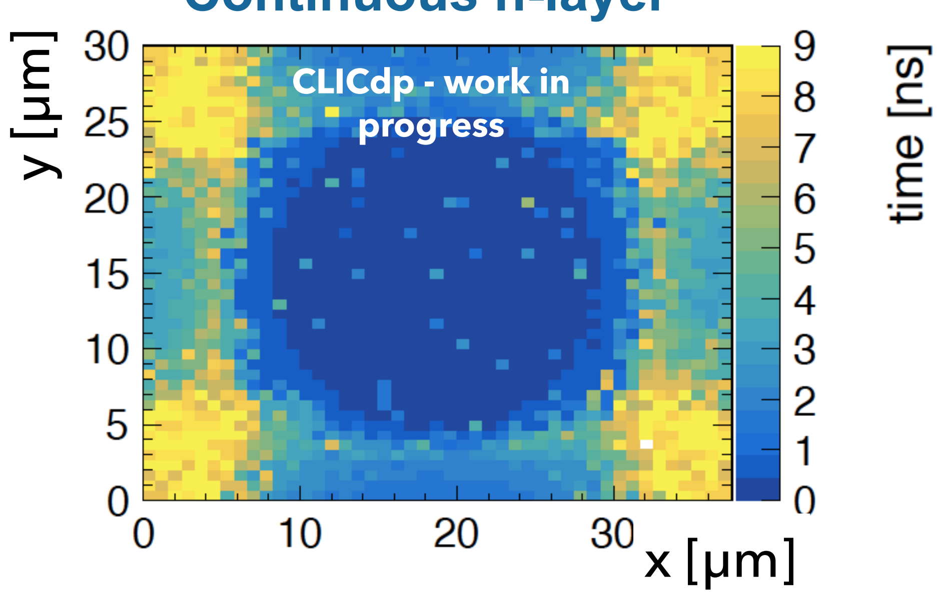
T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

CLICTD pixel layout

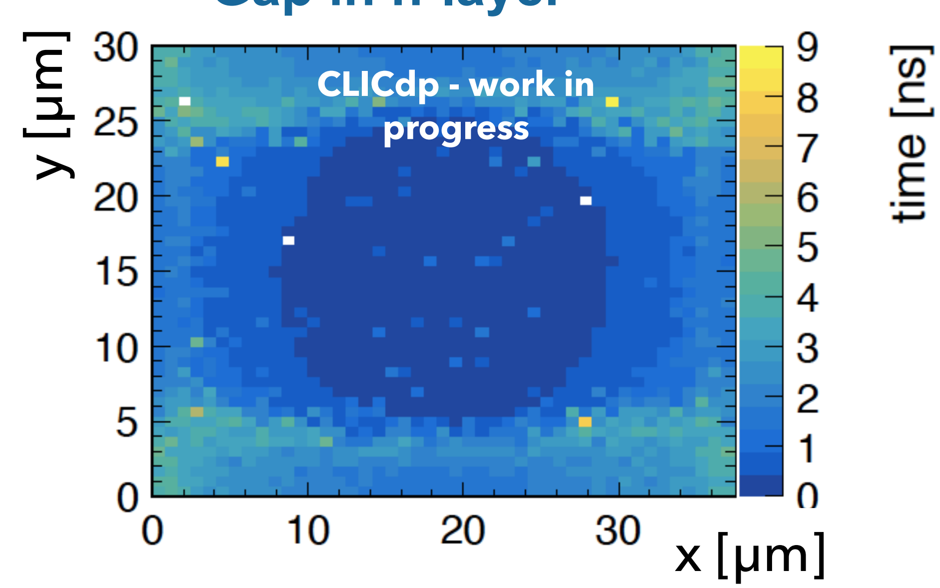


CLICdp-Pub-2020-003

Continuous n-layer



Gap in n-layer



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SUMMARY AND OUTLOOK

- Broad silicon detector technology R&D comprising hybrid and monolithic sensor designs -> several milestones in detector technology R&D achieved

➡ R&D relevant far beyond CLIC -> overcome today's challenges to develop tomorrow's detector

➡ Strategic **R&D programme** for future experiments (covering detector hardware, electronics, software, etc)

See talk from E. Rivera **CERN-OPEN-2018-006**

EP R&D

Part of the measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany)

- Alternative interconnect technologies are investigated
- Future monolithic sensors in CMOS technology are planned

Thank you!

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168

AIDA 2020

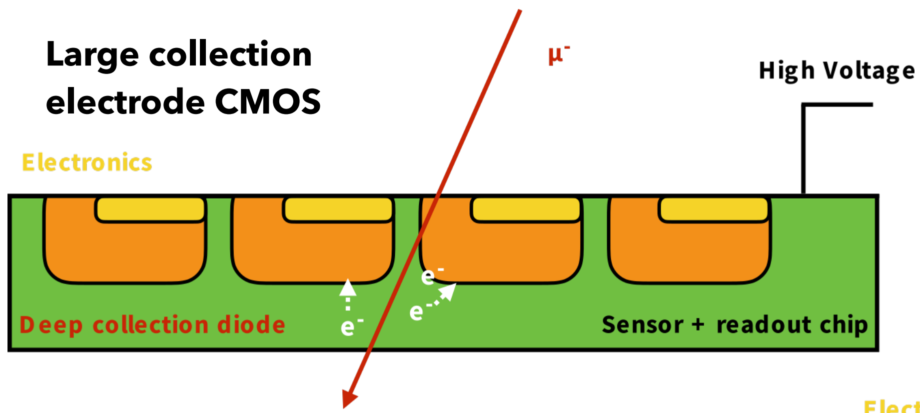
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

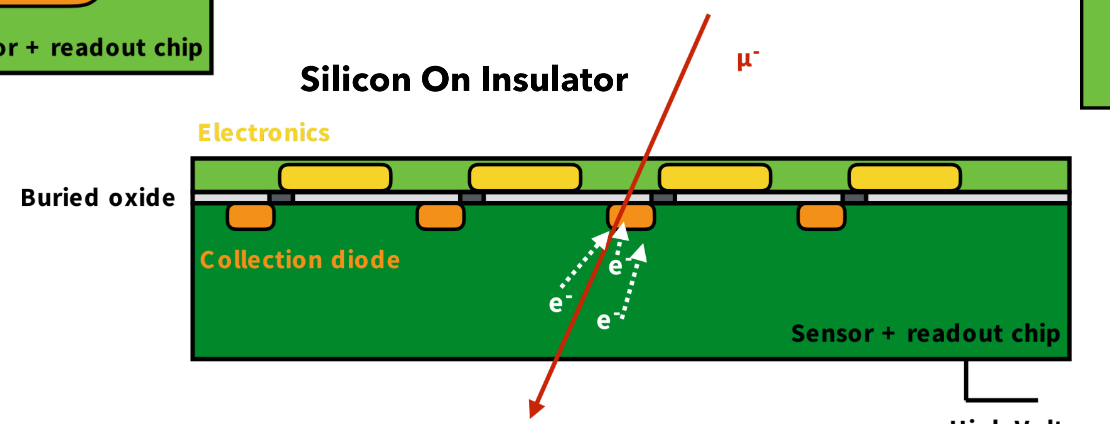
BACK-UP

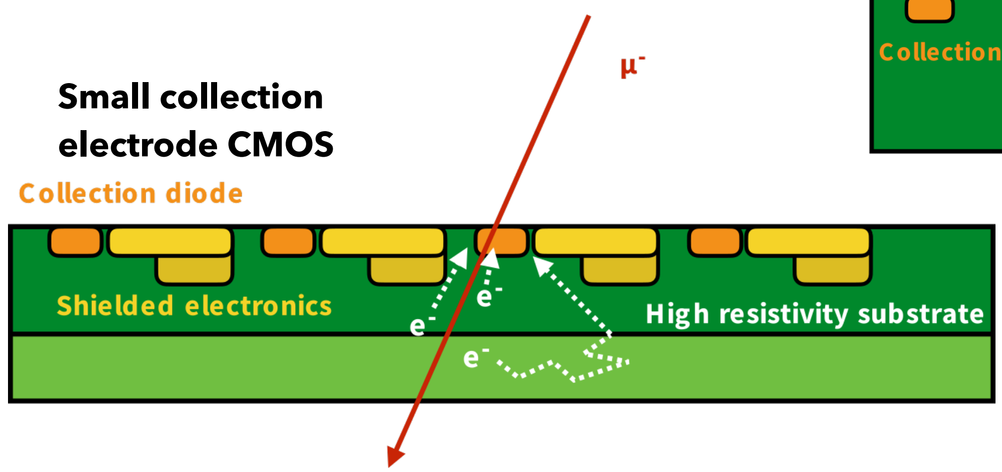
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

SILICON PIXEL DETECTOR TECHNOLOGIES

Monolithic

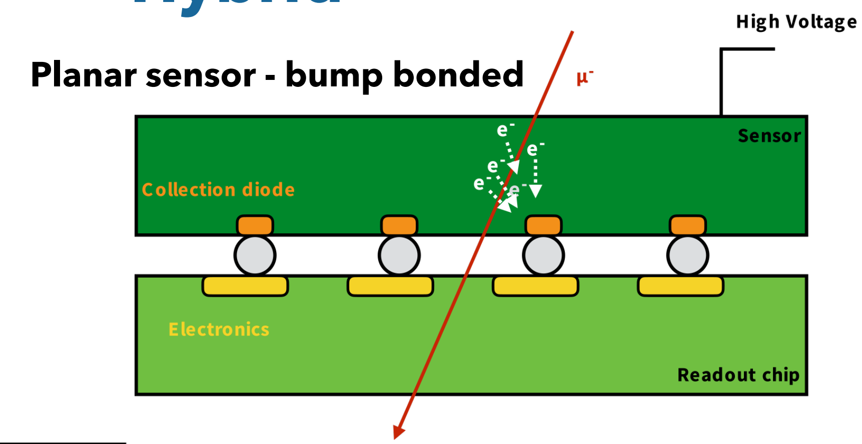


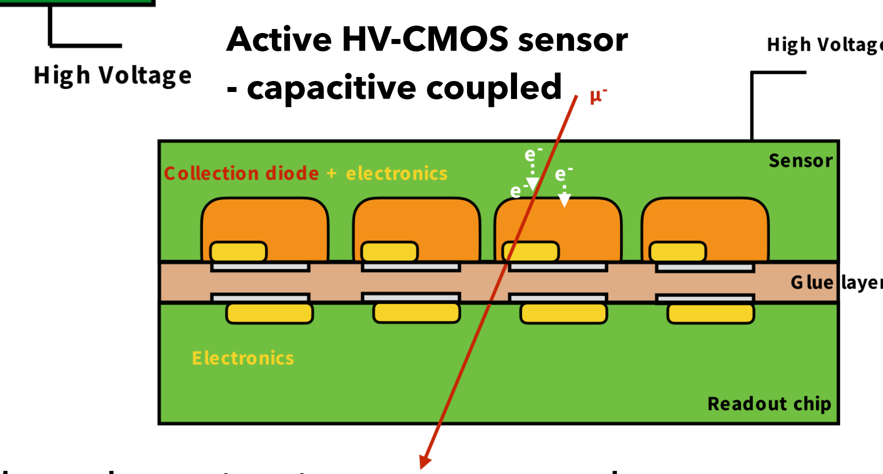




- Readout circuit integrated into active sensor -> no interconnects and low material content
- Profits from CMOS imaging industry -> large-scale production possible
- Considered for CLIC vertex and tracker
- Challenges: interaction between readout circuitry and sensor

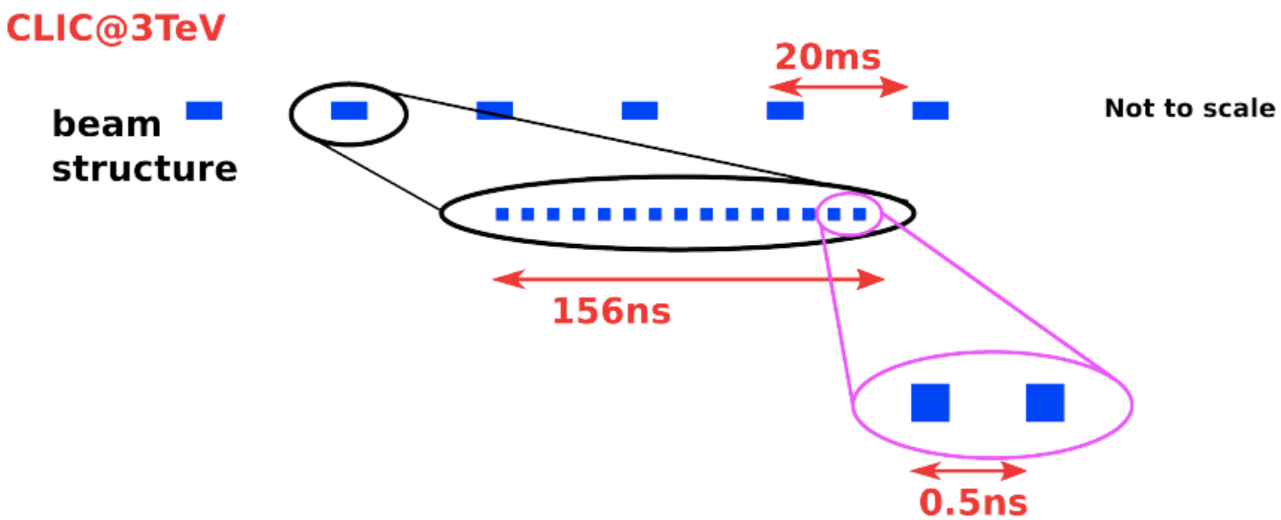
Hybrid





- Sensor and readout circuit are separated -> Independent optimization of both components
- Complex readout fits into small pixel size (also profits from advanced CMOS processes with very small feature size) -> interesting for vertex detector
- Challenge: interconnects for small pixel size

POWER PULSING



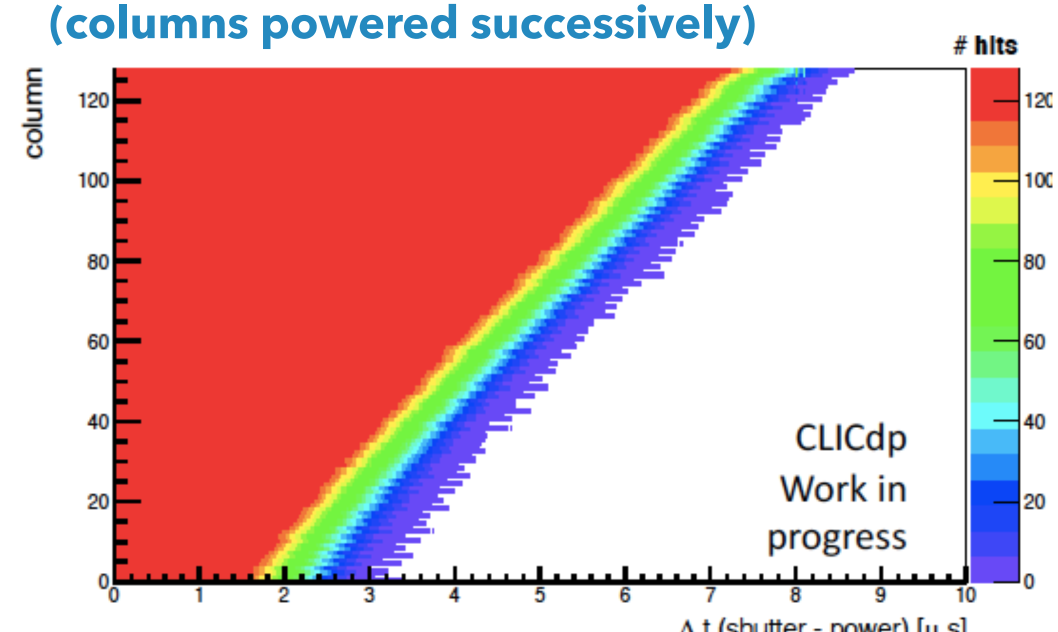
- Low duty cycle of CLIC accelerator bunch trains (repetition rate: 50 Hz) allow for **power pulsing**

- Detector components are switched to low power state between bunch trains
  - Reduction of average power consumption
  - Reduction of heat dissipation -> air cooling possible

CLICpix2 performance (analogue power-pulsing)

- Analogue preamp and discriminator are power pulsed
- Switching of power states induces power on response
  - Time until chip is quiet depends on how low power-off state is
- Average power consumption dominated by power-off state
- Power reduction by 5x
- Improvements by factor of x80 expected if more DACs are power pulsed (implemented in CLICTD)

Power on response for different delays (columns powered successively)



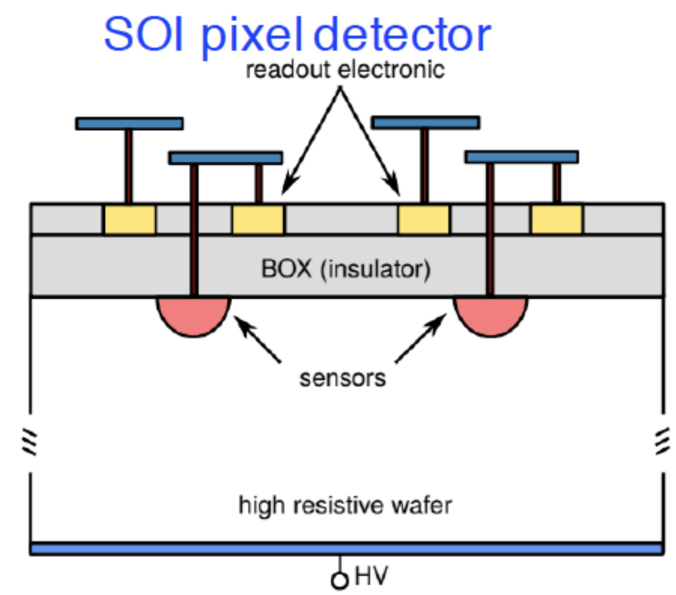
CERN-STUDENTS-Note-2019-212

AGH CRACOW SOI DEVELOPMENTS

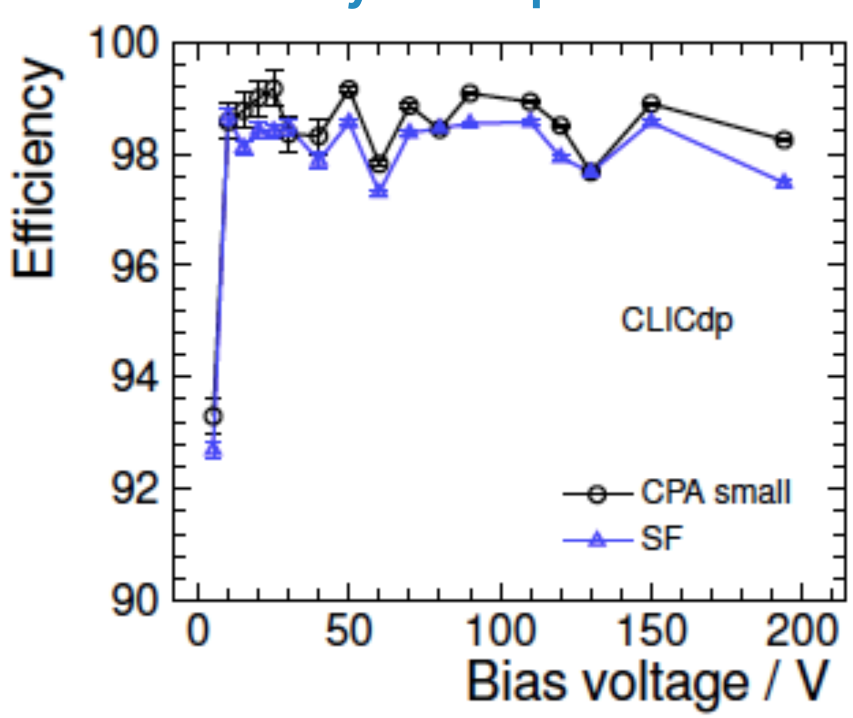
Cracow SOI test chip

- Silicon-On-Insulator (SOI) 200 nm technology
- Various geometries and technology splits
- Pixel pitch: >= 20 μm x 20 μm
- Single SOI and double SOI
- 300 μm wafer thickness

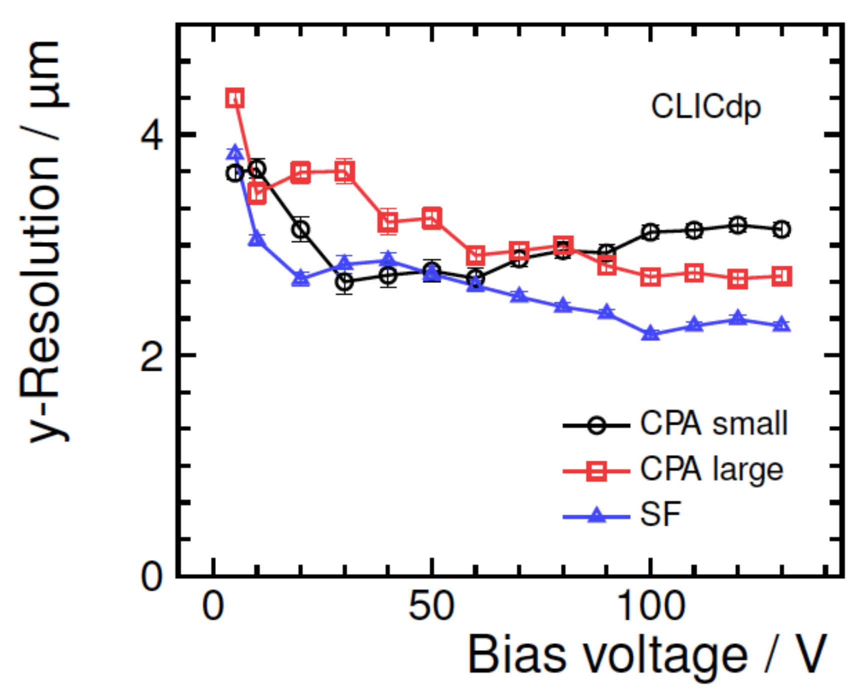
- High resistivity sensor wafer
- r/o electronics on low-resistivity electronics layer separated by buried insulation oxide layer



Efficiency of 500 μm-FZ-n SOI



Spatial resolution of 500 μm-FZ-n SOI



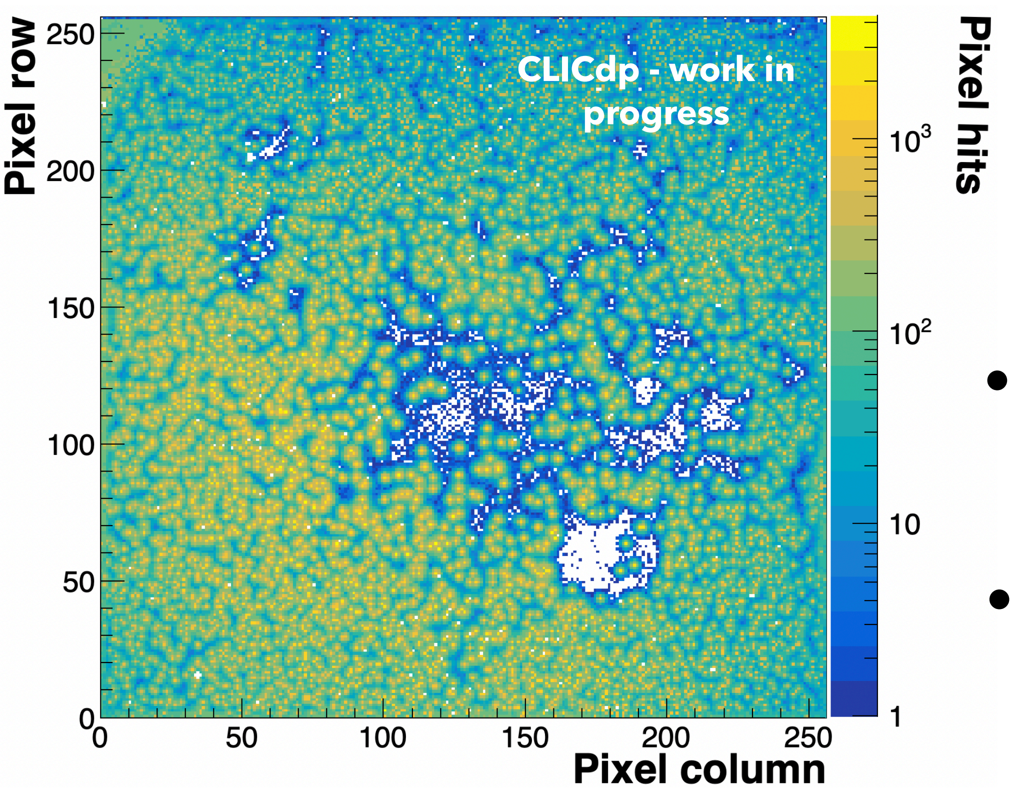
- Efficiency > 99%
- Spatial resolution: 2 - 5 μm

NIMA 901 (2018) 173–179

ANISOTROPIC CONDUCTIVE FILMS

ACF hybridization

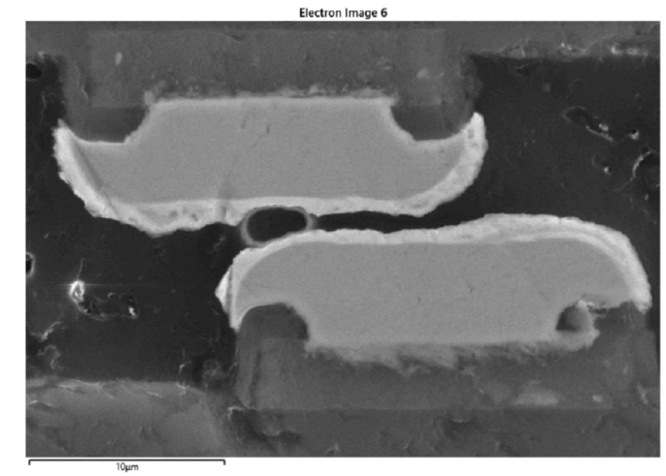
- Alternative to bump bonding, widely used in display industry
- 3 µm polymer spheres plated with Ni-Au embedded in adhesive film
- ENEPIG Under Bump Metallization (UBM) - Electroless nickel electroless palladium gold immersion



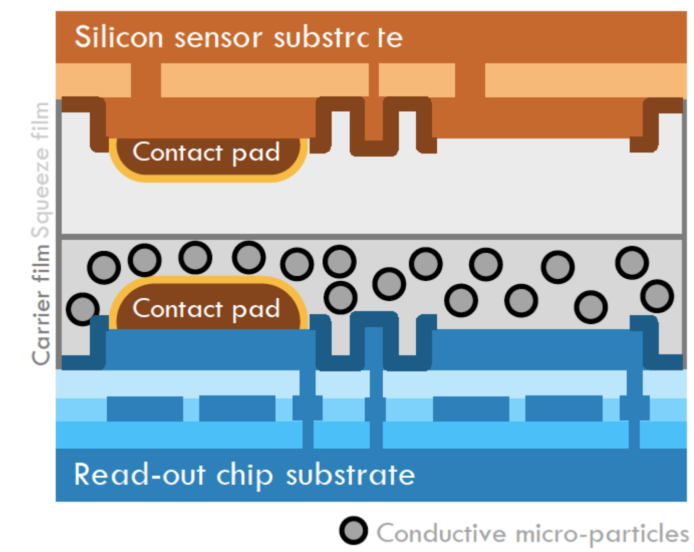
- µ-particles get crushed between UBM pads during thermo-compression

➡ Anisotropic electrical connection (in direction of compression)

- Challenging multi-parameter optimization of the hybridization process
  - Film thickness, applied force, #spheres/area etc.



TPX3-to-TPX3 SEM cross-section measurement



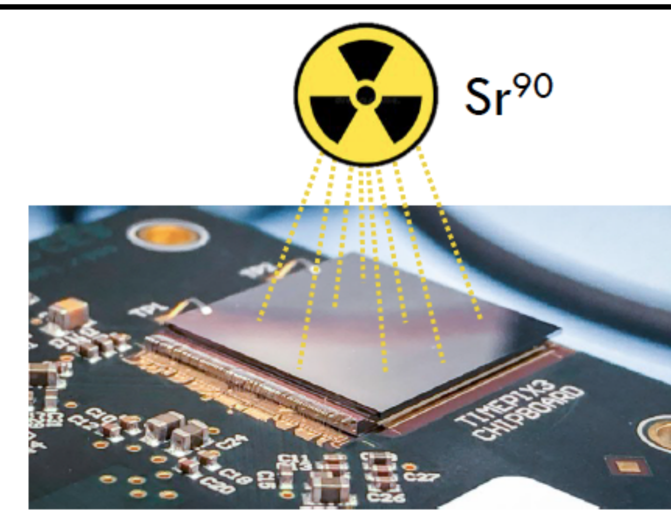
conpart

J APPL PHYS 119. (2016): 245102

- Timepix3 + planar Si sensor

(55 µm x 55 µm pitch, 256 x 256 pixels)

- Pixel matrix illumination with an Sr90 radioactive source



- Beam test with charged particles planned for coming months

https://indico.cern.ch/event/858640/

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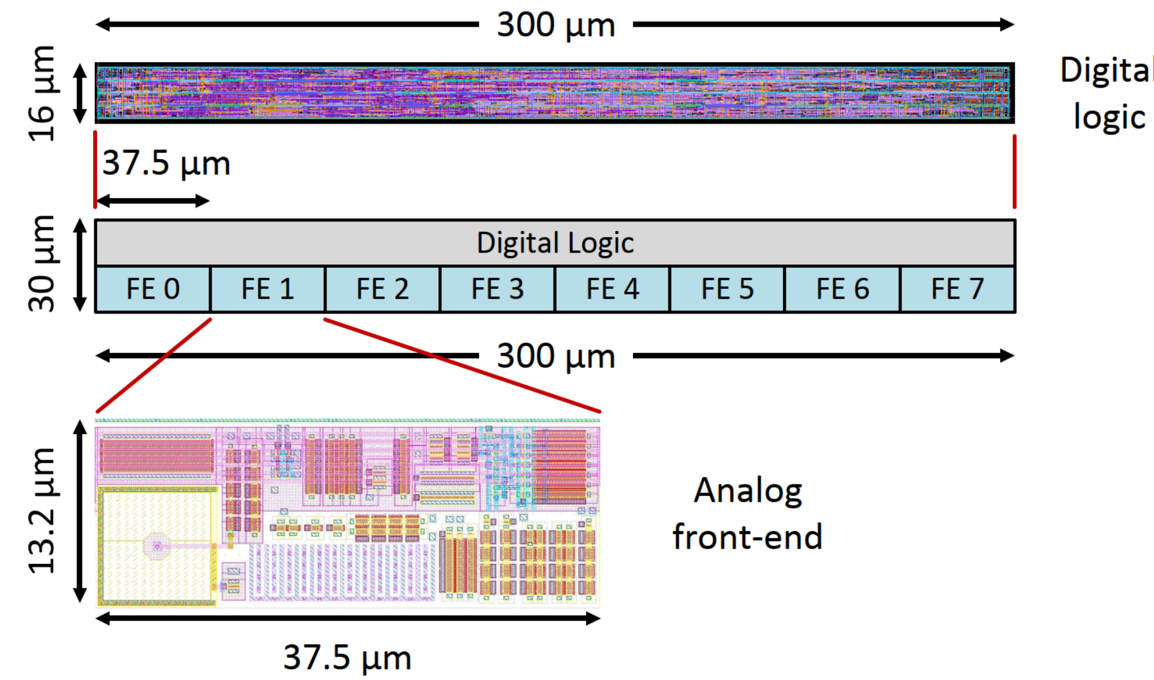
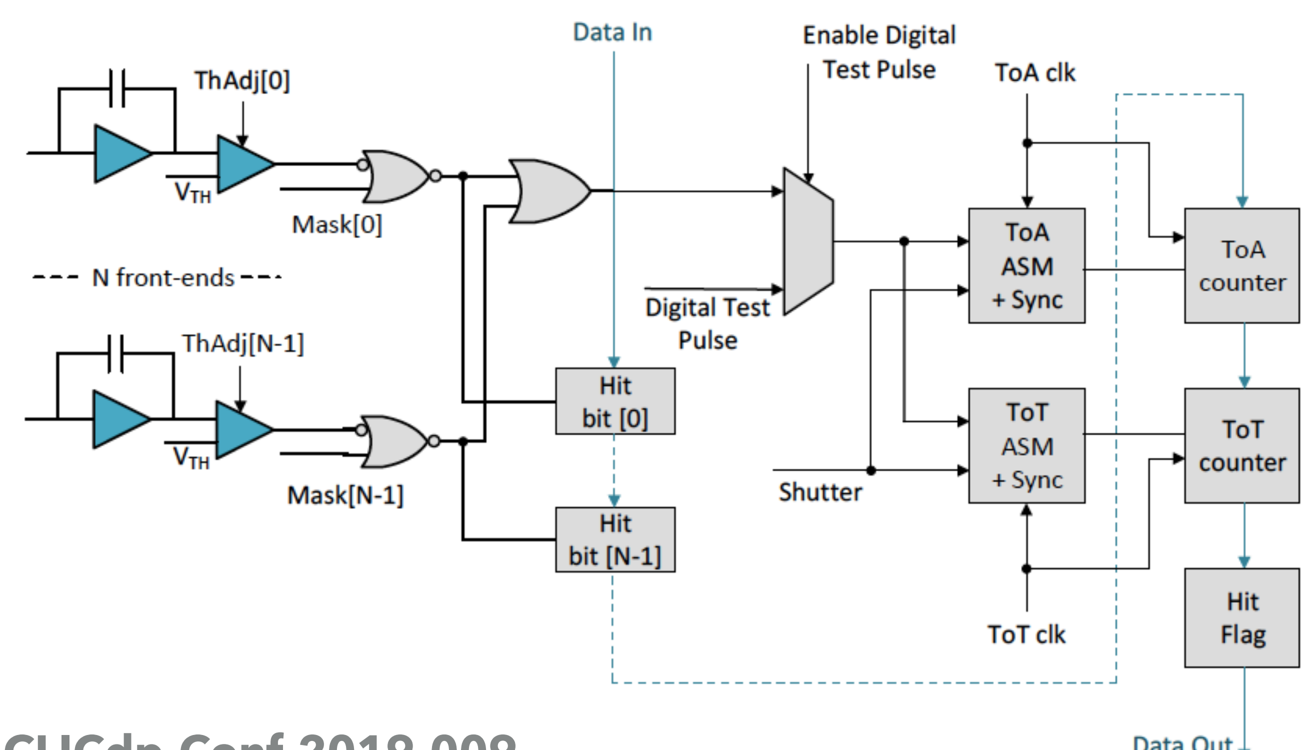
CLICTD - FRONT-END DESIGN

- Matrix size: 3.84 mm x 4.8 mm divided into 128 rows and 16 columns
- Detector channel: 300 µm x 30 µm with each channel segmented into 8 pixels
  - ➡ Save space for digital circuity while maintaining charge collection speed and low capacitance
  - ➡ Sub-pixel information combined with OR-gate (binary hit information for sub-pixels available)



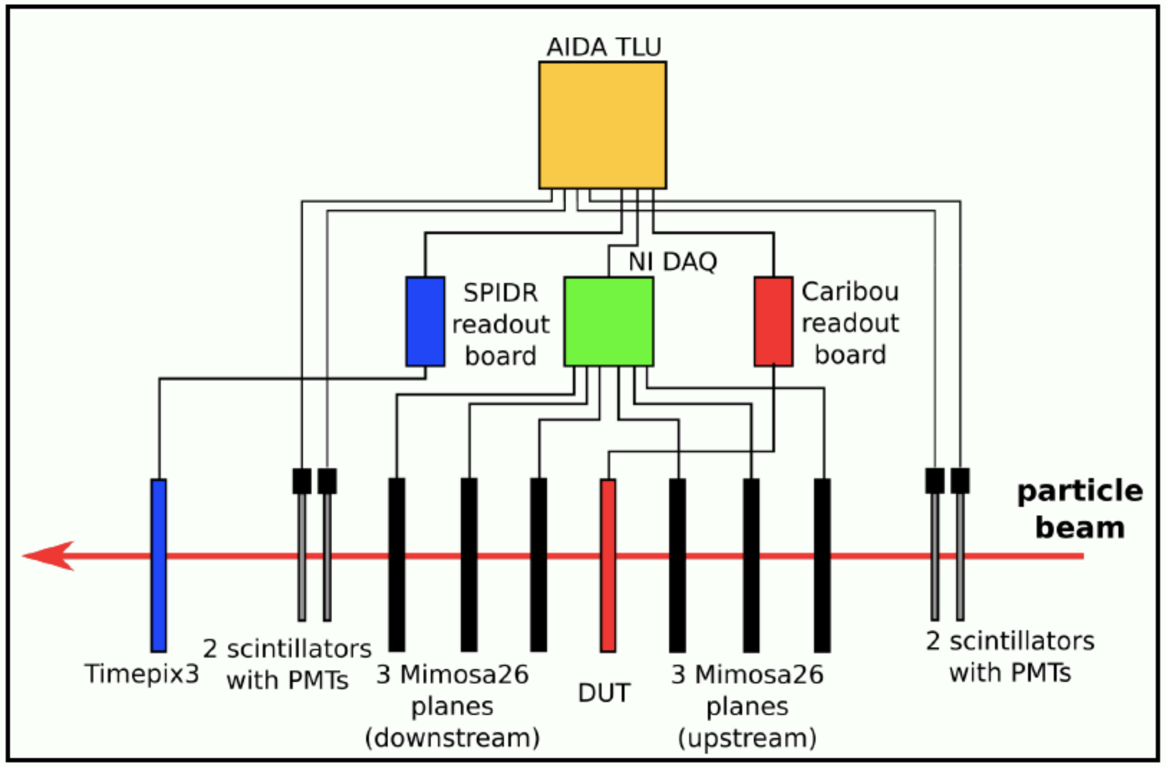


CLICdp-Conf-2019-009

Read-out

- Frame-based read-out with 40MHz
- Measurement modes:
  - 5-bit Time-over-Threshold (ToT) +8-bit Time-of-Arrival (ToA)
  - 13-bit long ToA
  - 13-bit photon counting
- 100MHz ToA clock -> 10 ns ToA bins

TEST-BEAM MEASUREMENTS AT DESY



6 MIMOSA planes:

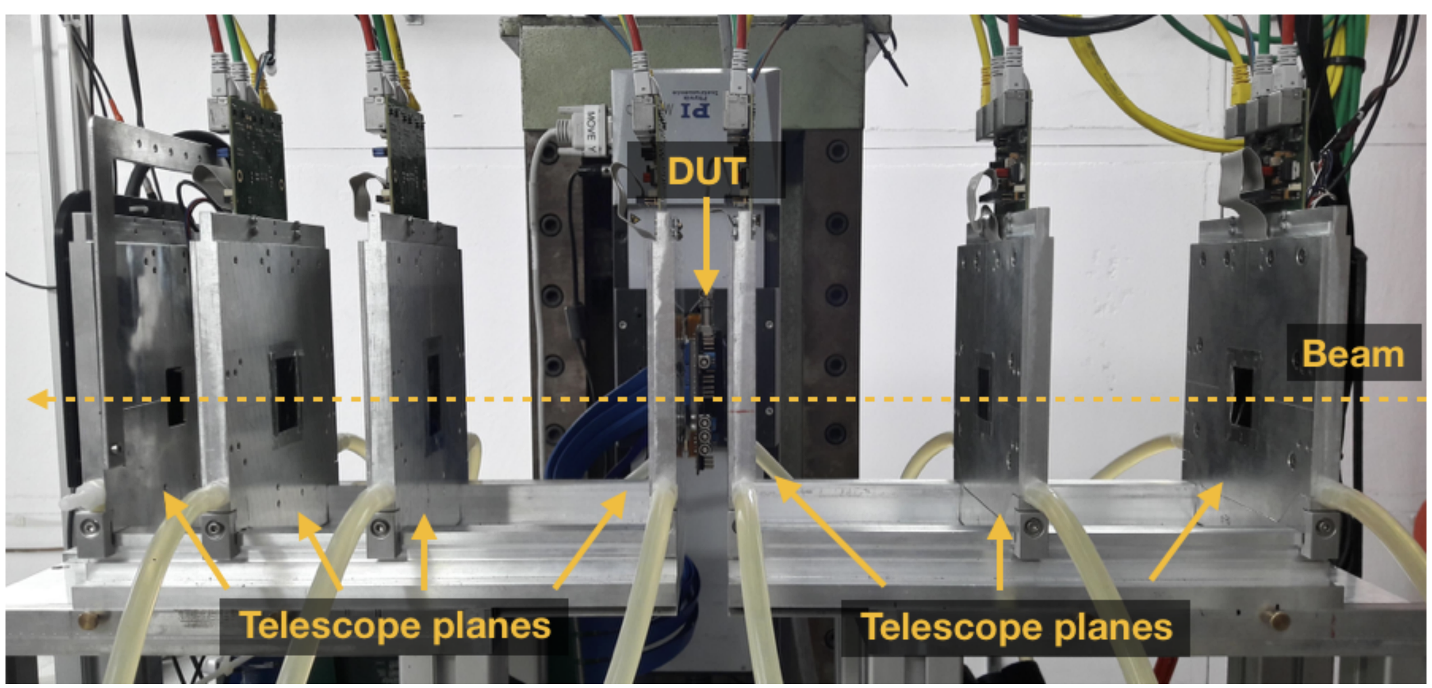
- High spatial resolution (~2 μm)
- Timing resolution > 100 μs

Timepix3 plane:

- Timing resolution: 1 - 2 ns (not calibrated)

4 scintillators:

- Triggers MIMOSA rolling shutter r/o



Corryvreckan test-beam reconstruction

- Versatile test-beam reconstruction framework for offline event building
- Modular approach, highly flexible and configurable
- Features 4D pattern recognition, Millepede alignment algorithm and General Broken Line algorithm for tracking

https://gitlab.cern.ch/corryvreckan/corryvreckan

CARIBOU DAQ SYSTEM

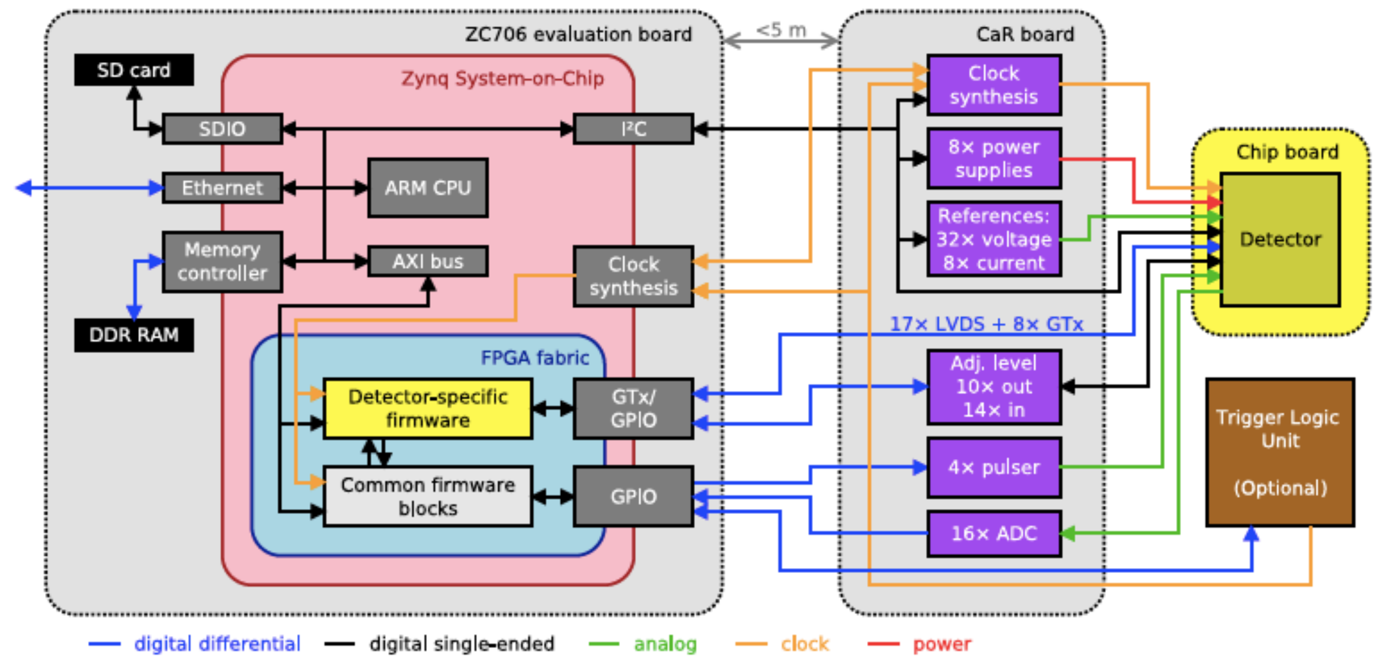
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Caribou

https://gitlab.cern.ch/Caribou

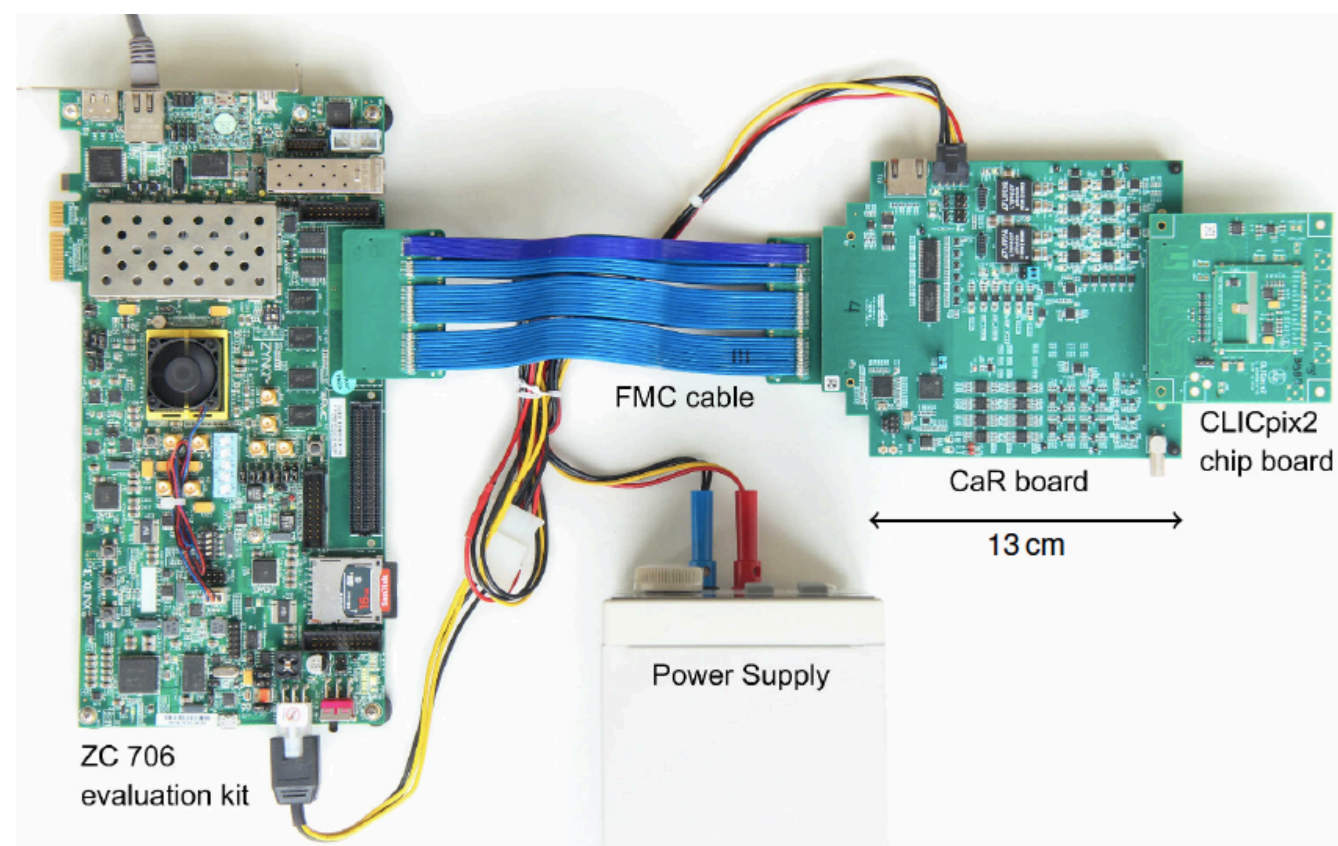
Versatile data acquisition system based on programmable hardware

- Caribou provides common hardware and software cores, only detector-specific part is modified
- Successfully used for ATLASPix, ATLASPix2, ATLASPix3, CLICpix2/C3PD, H35Demo/FEI4, RD50-MPW1



System-on-Chip (SoC) board

- Embedded CPU for DAQ, user interface, operating system (Linux)
- Field programmable gate array (FPGA) for detector control and data processing



Control and Readout (CaR) interface board

- Physical interface from SoC board to detector chip
- Voltage regulators, ADCs, pulse/clock generator

Application-specific detector carrier board

- Only detector chip and passiv components