Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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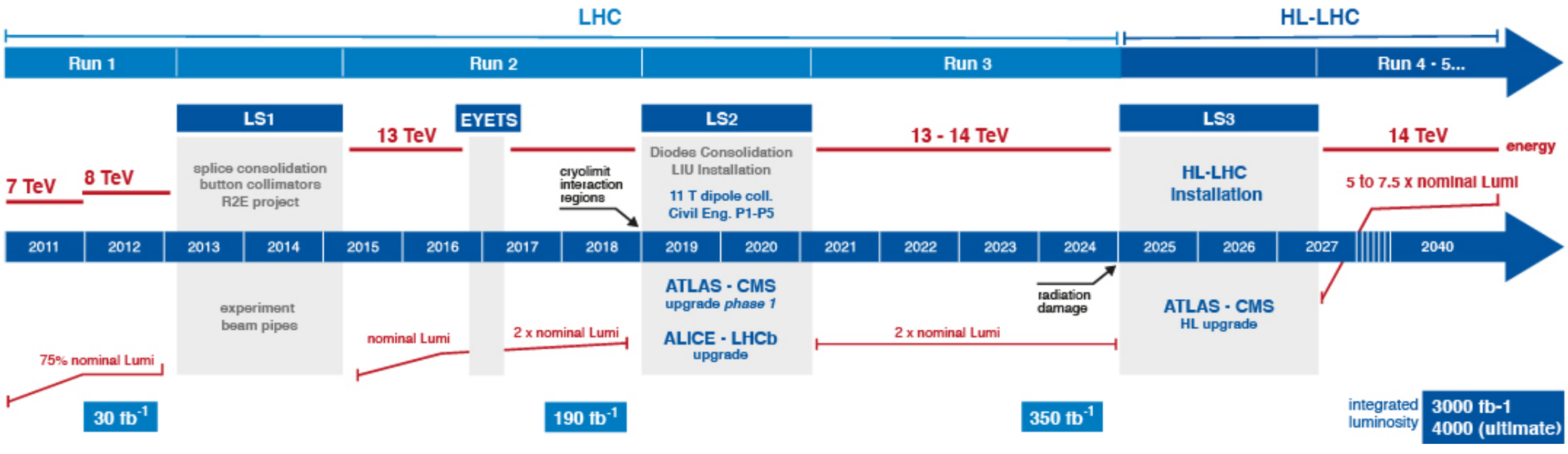
July 30th 2020 - ICHEP Conference - Virtual

HL-LHC



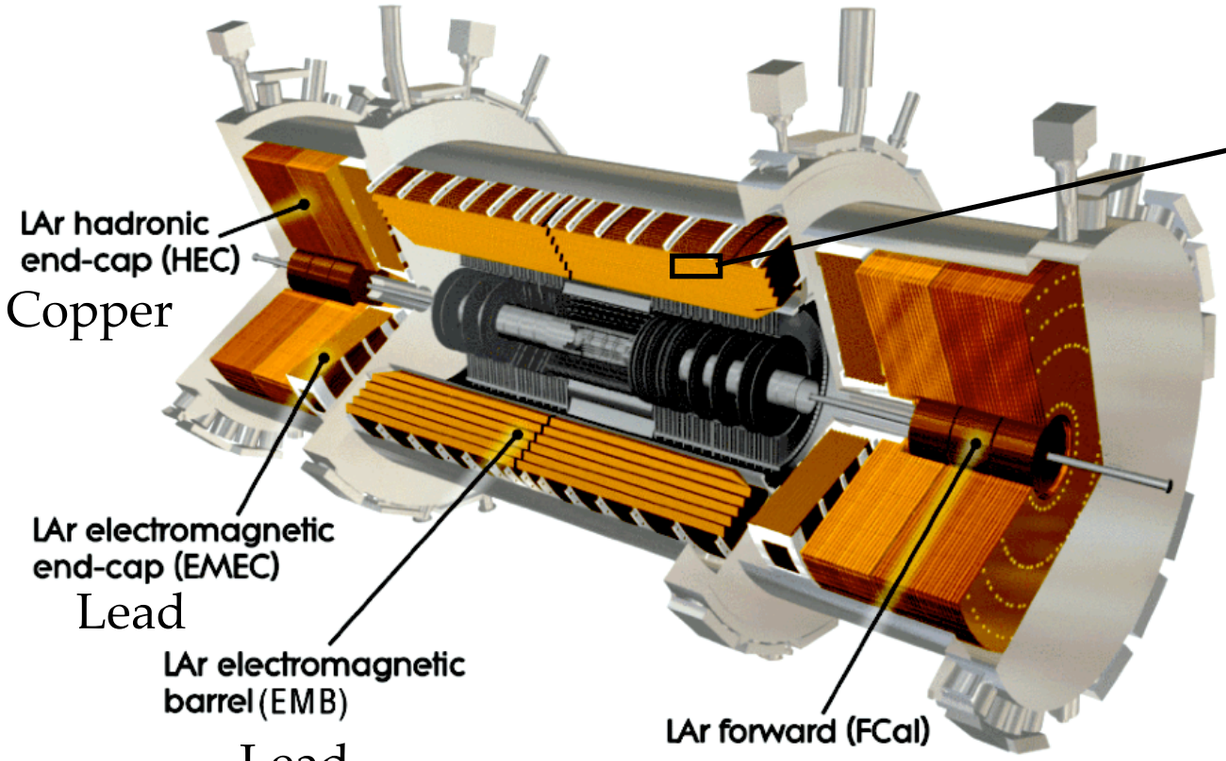
- **Full calorimeter readout electronic chain upgraded (physical detectors kept in place)**

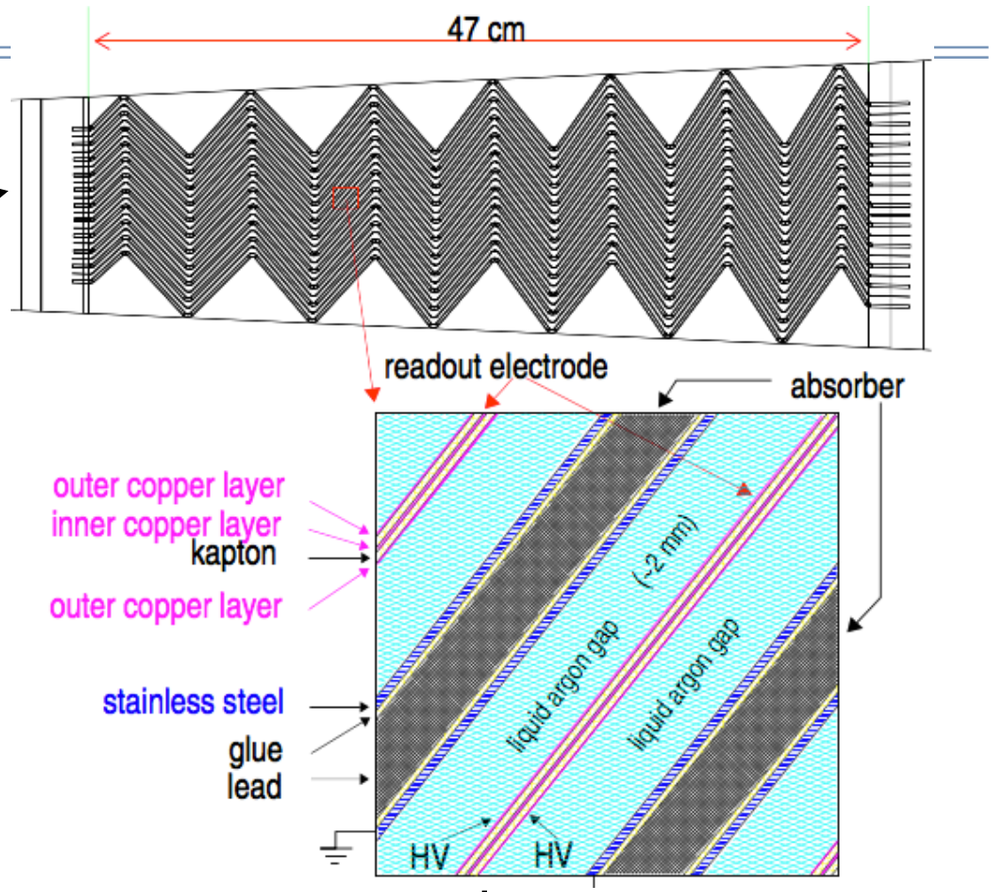
- **Why upgrading ?**
  - **Very large pileup (~200)**
  - **Current electronic not qualified for 4000 fb^{-1}**
  - **Incompatibility with future ATLAS trigger scheme**
  - **Technological progresses**

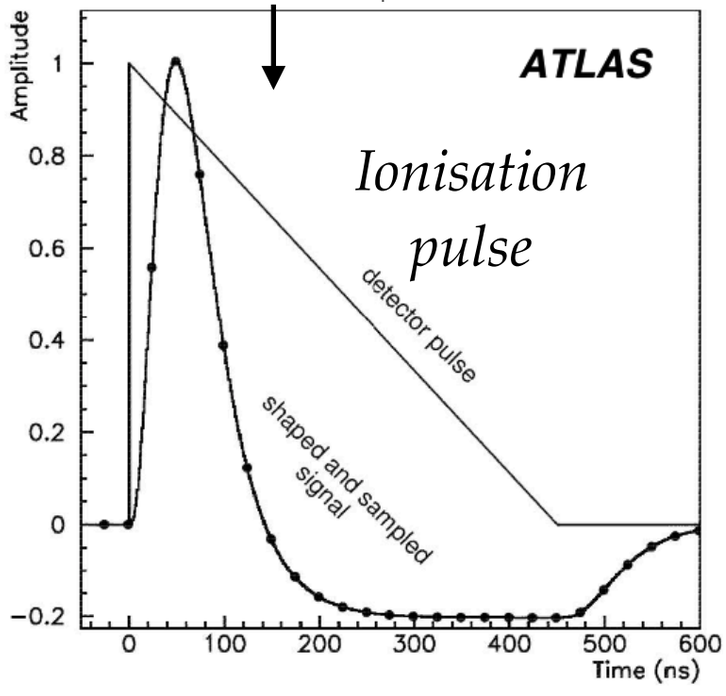
- **Goal:** maintain and enhance physics reach during HL-LHC (per-mil linearity at EWK scale, 16-bit dynamic range, low electronic noise)

- **Installation during the 3rd long shut-down of the LHC.**

The Liquid Argon Calorimeters

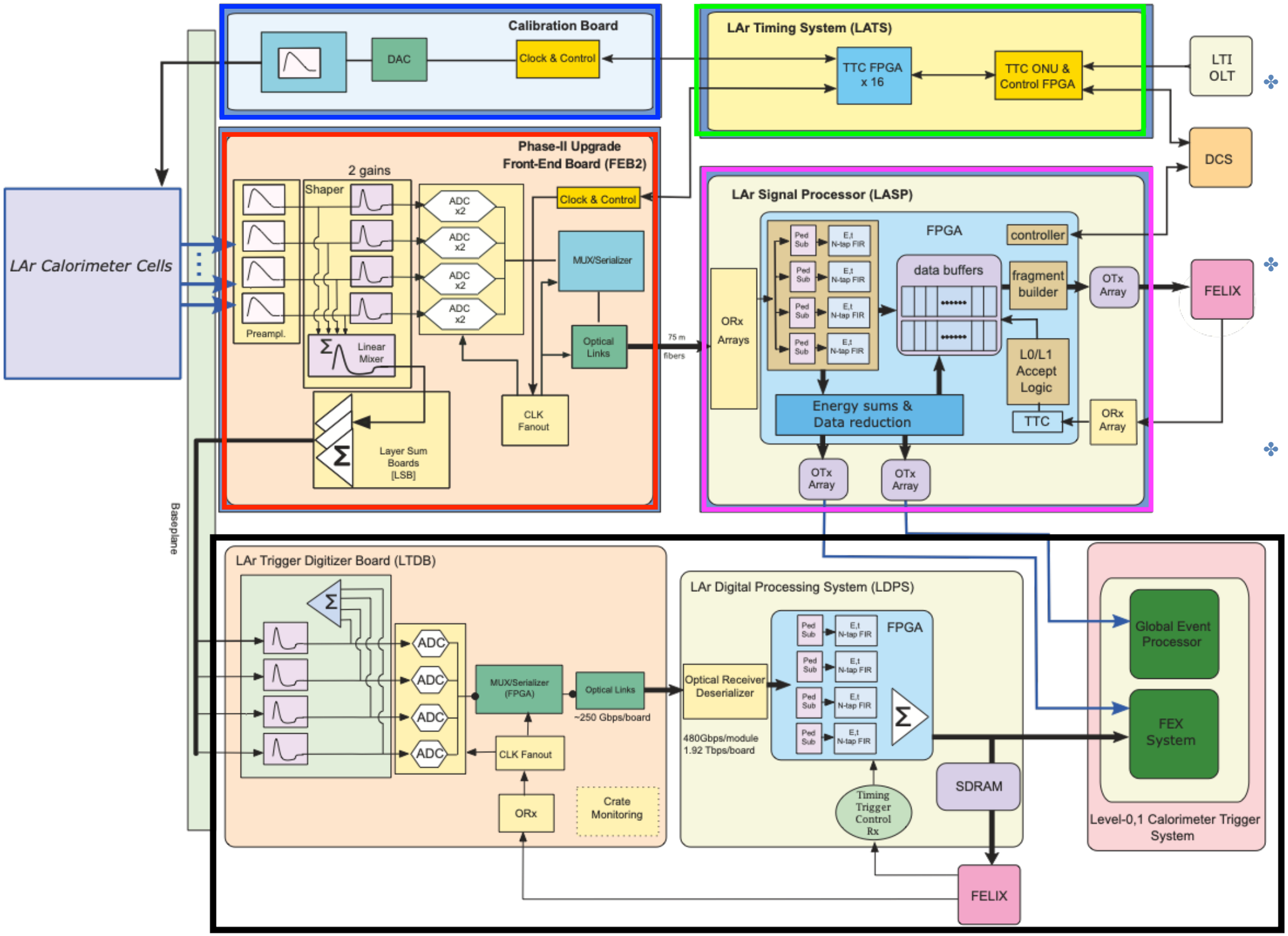






- Liquid Argon Sampling calorimeters with fine granularity
  - ~180 000 cells
- ~50 MeV to 3 TeV, ~0.8-1% constant term
- **In operation since installation in 2006**

LAr Phase II: upgrade of the readout electronics

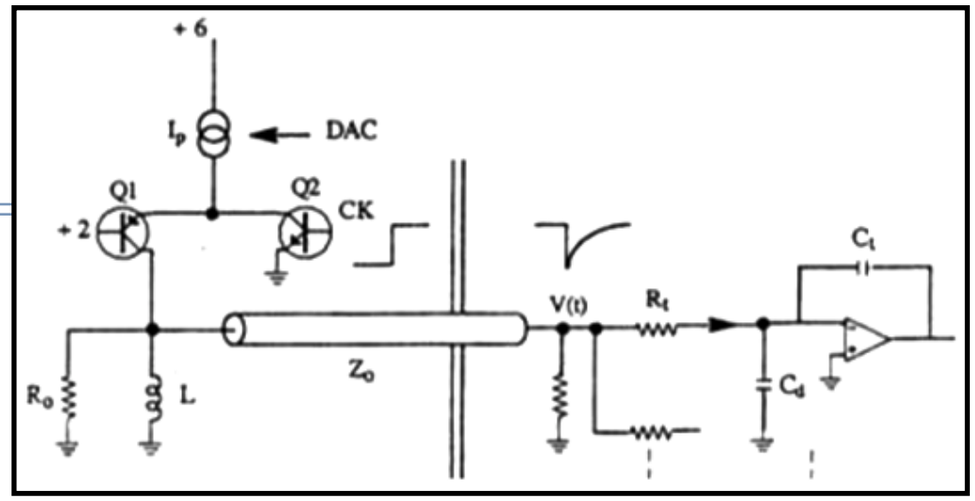


- Change the entire front-end: **1524 new Front-End-Board (FEB2s)** in existing FEC
- Change the calibration system: **130 new Calibration Boards** in existing FEC
- Off-detector:
  - **380 new LAr Signal Processor (LASP)** (replace ROD)
  - ~20 new LAr Timing System boards

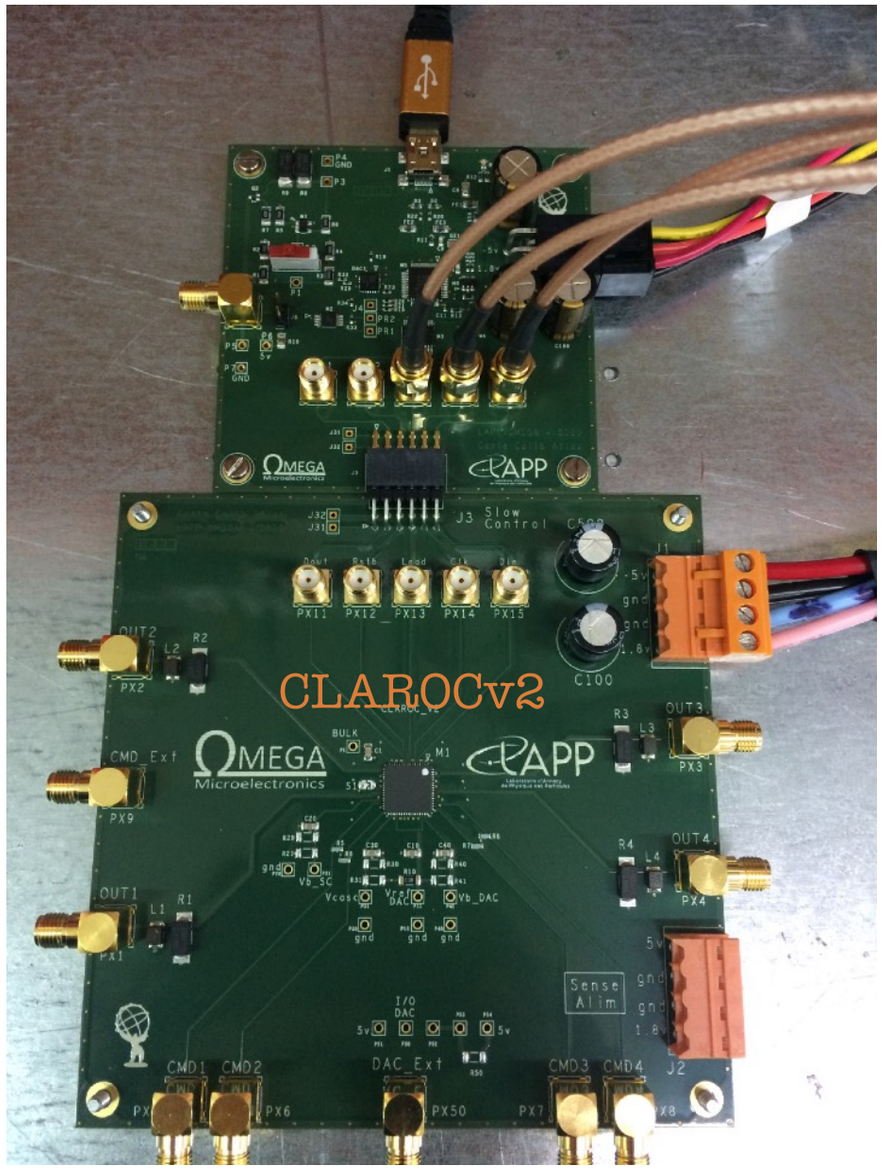
Installed during Phase-I. See Pavol Strizenec's talk. Remain operational during HL-LHC

On-detector **Off-detector**

Calibration system

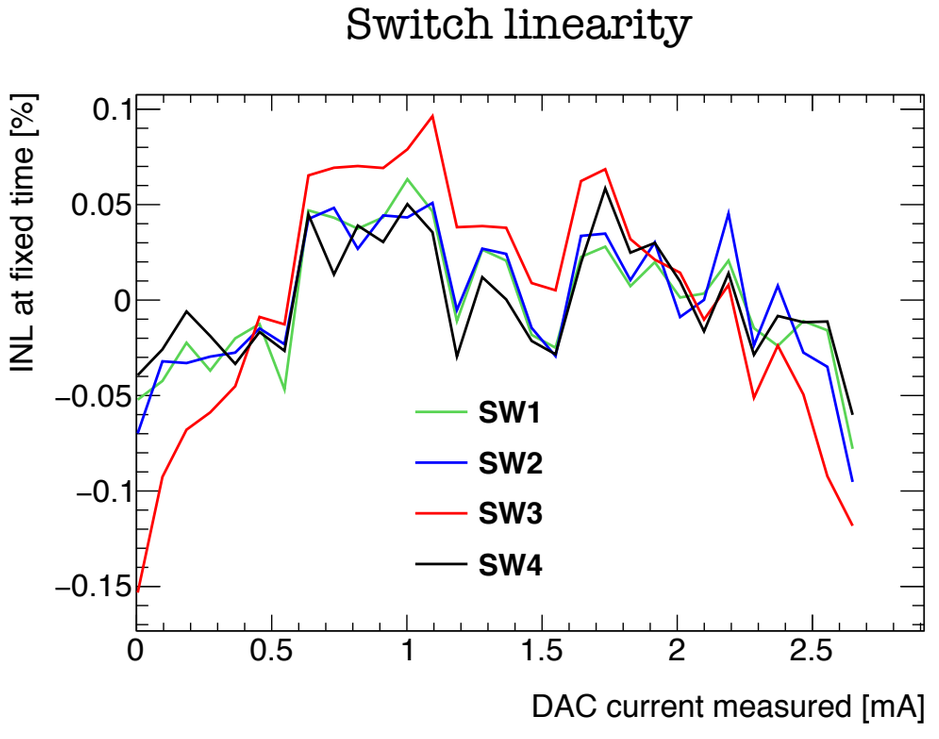


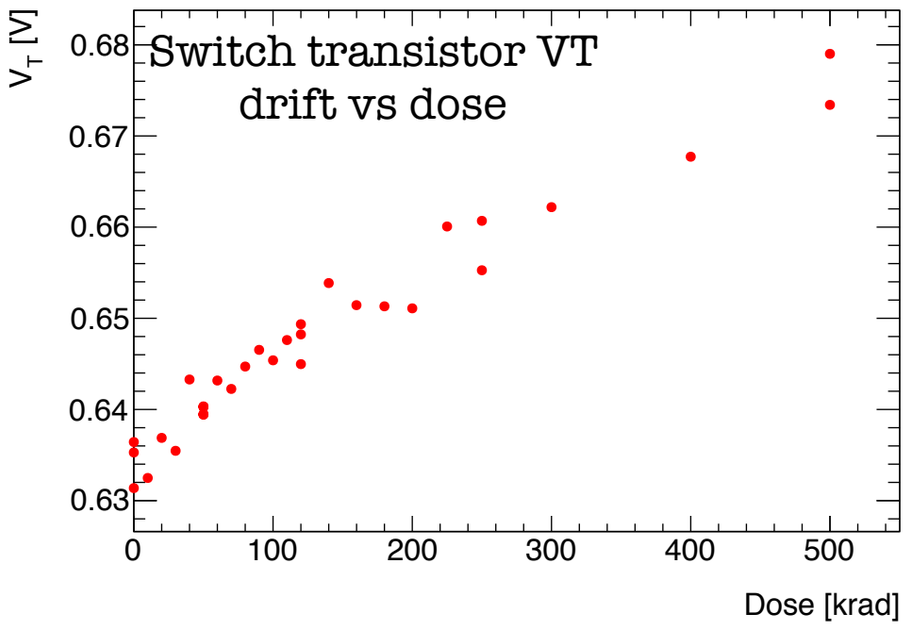
- **Inject exponential pulse of known amplitude (DAC) on the detector cell, to probe electronic response (µA)**
- **Requirements:**
  - Integral non-linearity (INL) <0.1%. Uniformity <0.25%, 16 bit dynamic range, Pulse rise time <1 ns
  - Radiation-tolerant to 1.8 kGy
- **CLAROCv2 (Calibration of Liquid ARgon Output Chip) :**
  - Custom HF switch + DAC 16-bits in XFAB HVCMOS 180nm, 4 different channels
  - Chip + test boards received in January 2020
- **Tests in laboratory test bench:**
  - Excellent linearity of HF-Switch part and DAC 10-bits (0.05%)
  - 13-bits DAC (10 bits+thermometers) and 16-bits DAC (13-bits + current mirrors) have larger INL (~0.4%) due to bit mismatches.

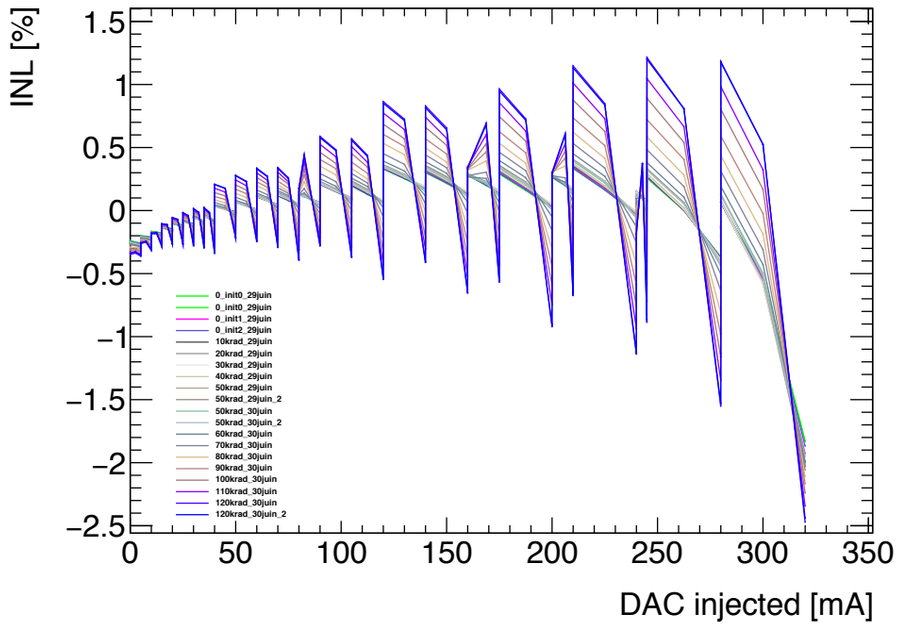


Calibration system

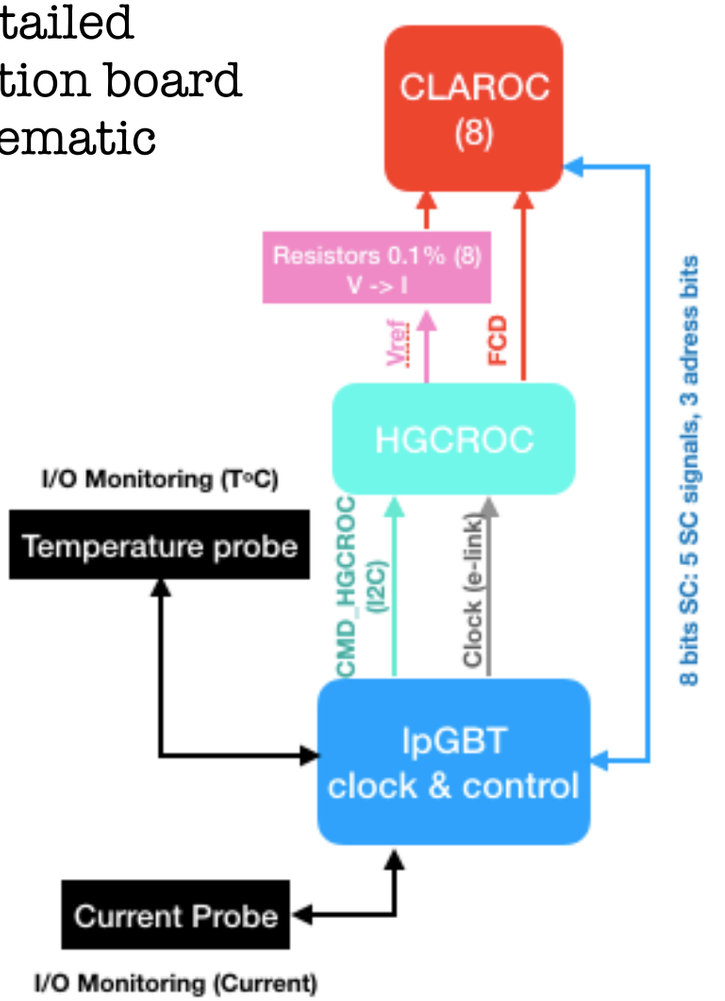
- **Tests under X-ray irradiation, up to 10kGy TID**
  - HF switch and current mirror stable
  - DAC 10 and 13-bits degraded after 0.5 kGy
    - will need to go for another technology (TSMC 130nm)
- **Next steps:**
  - **Submission of 2 ASICs by the fall**
    - HF switch +mirrors in XFAB 180nm
    - DAC in TSMC 130nm with improved linearity
  - **First prototype of 32-channels calibration board by the end of the year**







Detailed calibration board schematic



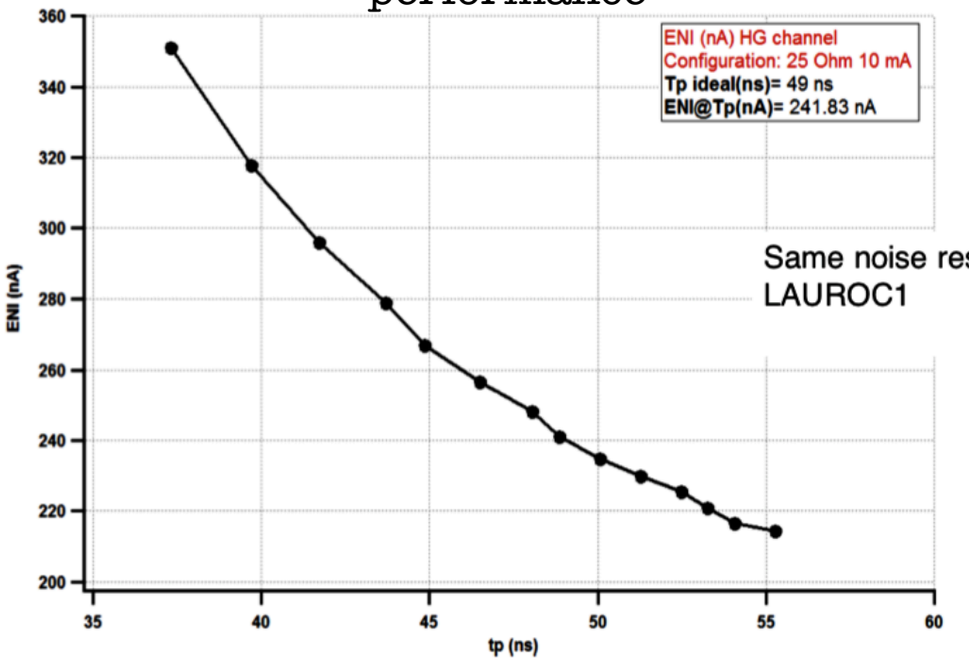
Front-end: analog processing

- **Requirements:**
  - **Performs pre-amplification, splitting in 2 gain scales** HG and LG with ratio HG/LG of 23±5 and ENI <120-350 nA
  - **CR-RC² shaping of ionisation signals**
  - **Summing of channels for L0 trigger** with linearity <2%,
  - **Radiation tolerance** up to TID =1.8 kGy.

- **2 types of ASIC under tests (CMOS TSMC 130 nm)**
  - **LAUROCv2 (Liquid Argon Upgrade Read Out Chip)**
    - Dies received in January 2020: 4 channels, 2 gains each, I²C for slow control (200 tunable parameters)
    - INL of 0.2% over 80% of dynamic range, within specification. HG/LG ratio a bit over spec, need adjustment of CR/RC² settings
    - Next steps : protons irradiation to test SEE
- **ALFEv1:**
  - 2 boards with packaged ASIC available, tests started end of June.
  - Design of ALFEv1b with all features ready this summer, simulated performance within specs.
  - Irradiation tests will be done

LAUROCv2 test board

LAUROCv2 noise performance



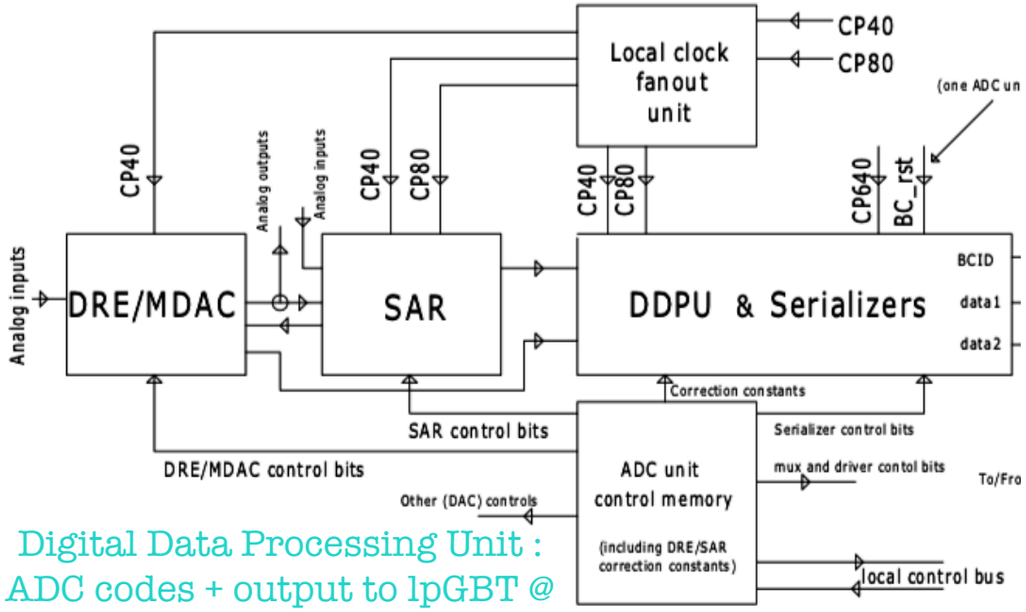
Same noise result as LAUROC1

Front-end: digitization

- **Requirements:**
  - Digitize preamplifier and shaper outputs at 40 MHz, 14-bit dynamic range and >11 bit precision
  - Radiation tolerant up to 1.8 kGy

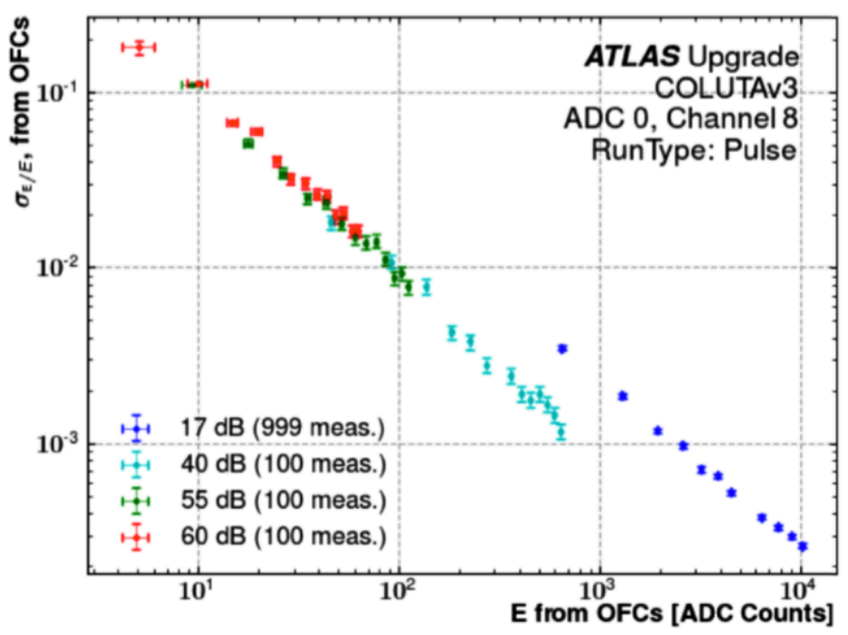
- **2 types of ASIC under tests**
  - **COLUTAv3: Full custom ASIC in TSMC 65nm, I²C interface**
    - 4 Dynamic Range Enhancer (DRE) + 4 Multiplying DAC (MDAC) @14bits + 12-bit pipeline Successive Approximation Register (SAR) ADC
    - Performance under study: LAr pulses with resolution within spec in almost full dynamic range, very small cross-talk
    - Next step: proton irradiations for SEE testing
  - **ADESTO/S3-IP-Block: reuse ADC IP core developed by Adesto/S3 company for CMS ECAL, in TSMC 65 nm**
    - 2nd version reviewed by CERN and Adesto/S3, submitted in May with modifications on I²C, improved power distribution, improved analog/digital separation
    - Test boards under design, dies back from foundry by end of 2020

COLUTAv3 schematic

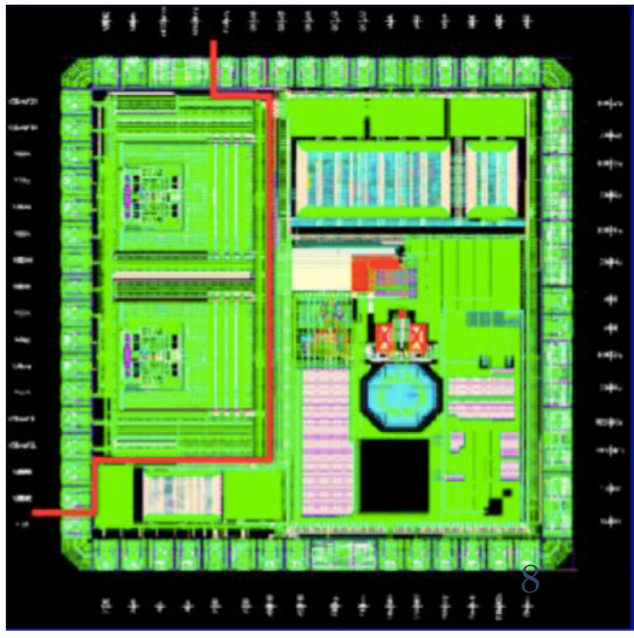


Digital Data Processing Unit : ADC codes + output to lpGBT @ 640 Mbps

COLUTAv3 energy resolution performance



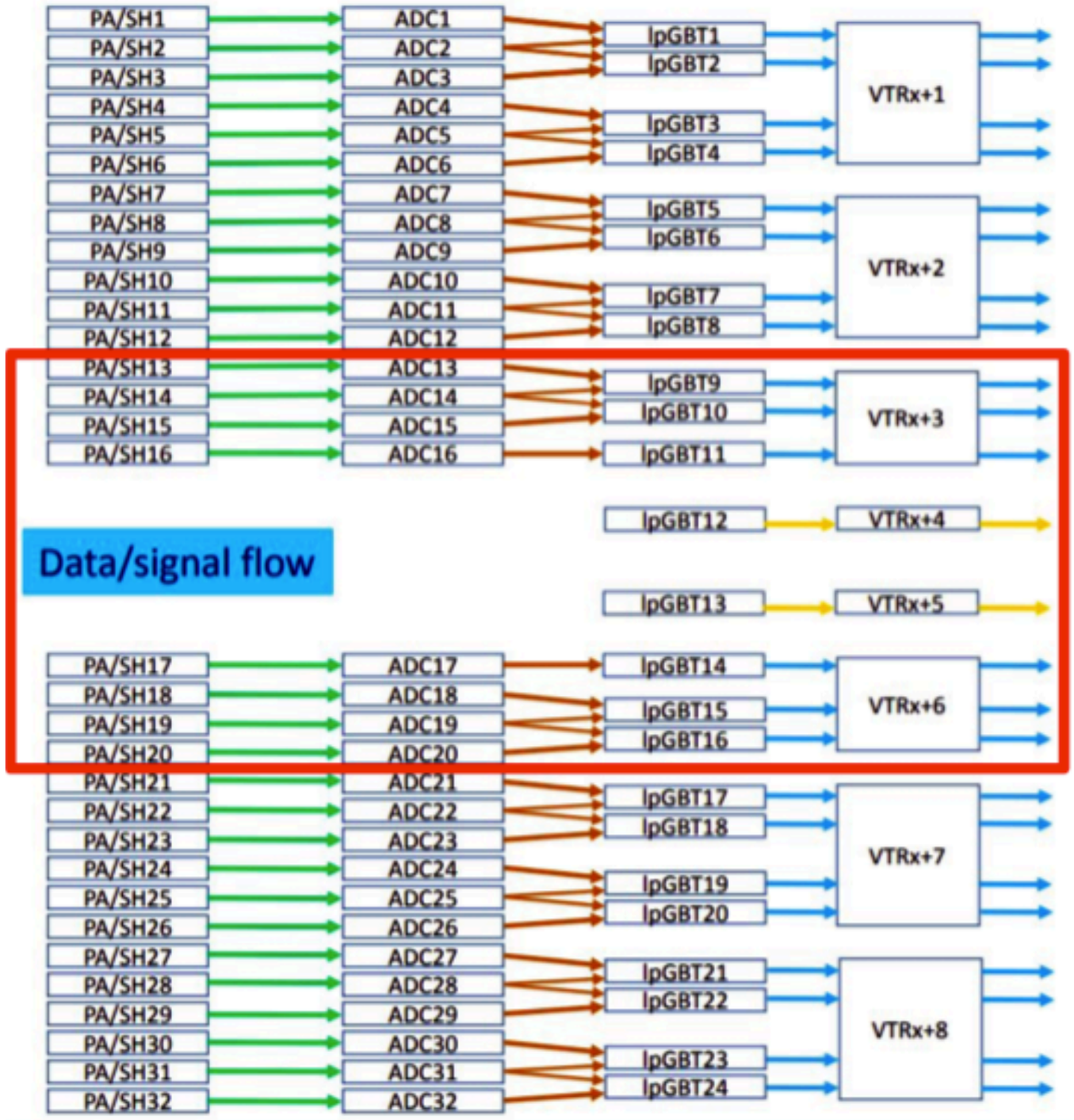
Analog/digital separation ADESTO/S3 IP Block



Front-end board and Layer Sum Board

- **Front-End-Board (FEB2): final board integrating preamplifier, shaper and ADC chain, 128 channels**
  - Slice test board design ongoing, 32 channels, with redundant control links and different options for powering:
    - 8 LAUROCv2 +8 COLUTAv3 +8 lpGBTv1 + 2/3 VTRx
  - Fabrication to start soon, tests will begin in Fall
  - Full FEB2 Prototype in 2021
- **Layer Sum Board (LSB): sums analog readout data from preamp-shaper for L0:**
  - Simulation and schematics ongoing, test board this summer
  - Radiation testing of op-amp will follow

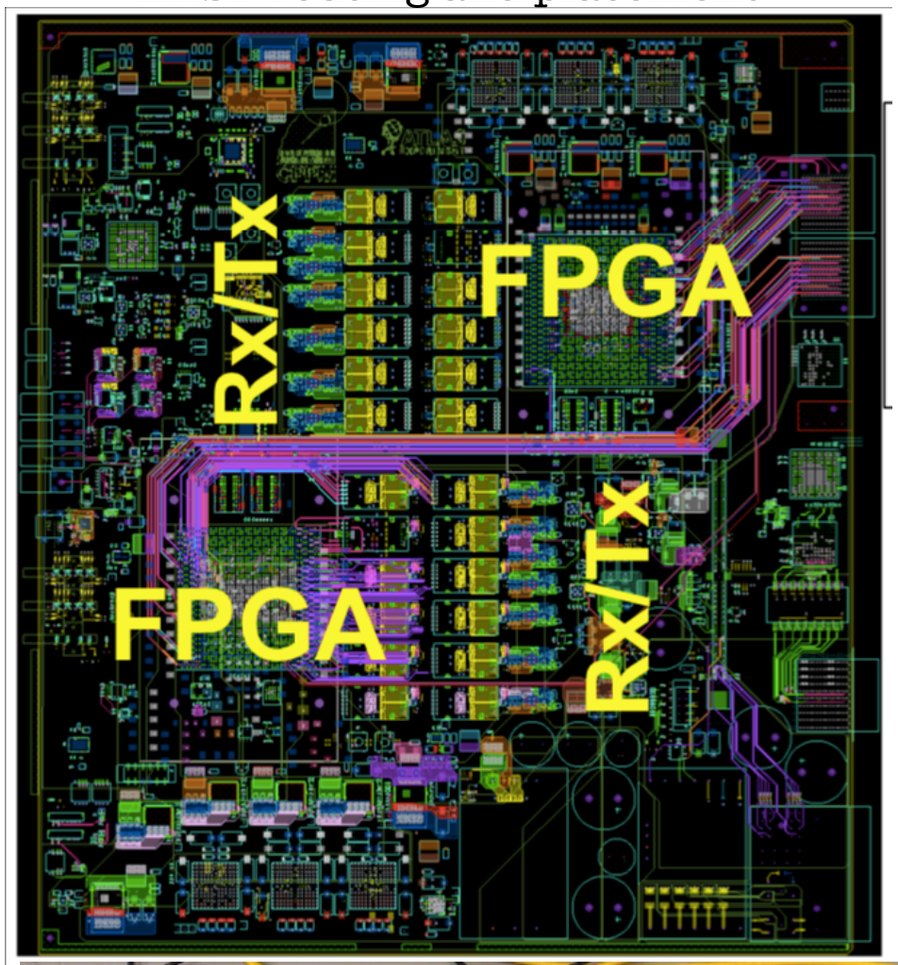
FEB2 and Slice test board schematics

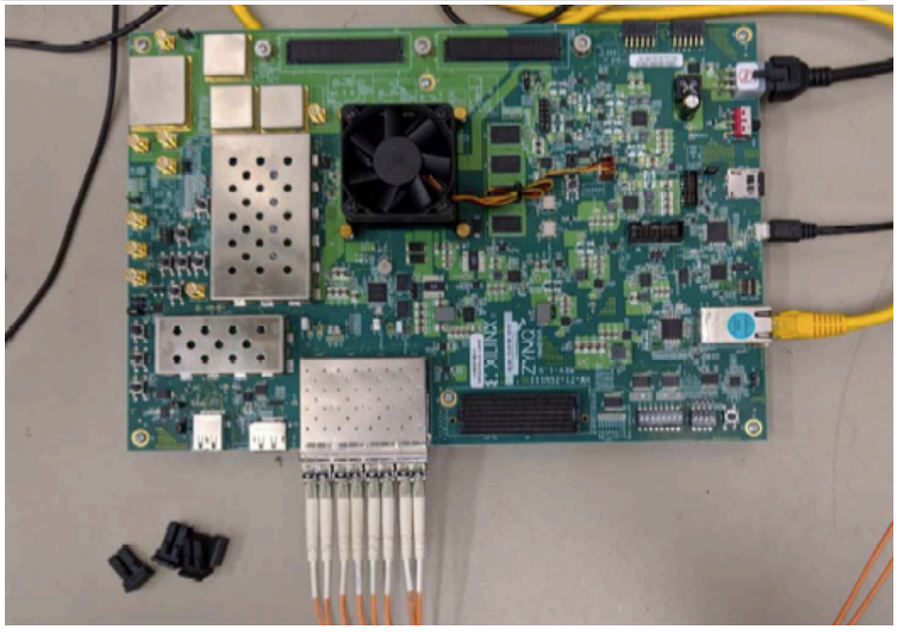


Off-detector: LAr Signal Processor

- **LAr Signal Processor (LASP): apply digital filtering to digitised waveforms, calculate energy and time, transmit to trigger and DAQ**
  - **Finalizing layout for ATCA LASP test board, routing 90% complete, ready late 2020**
    - 2 processing FPGA (Stratix 10), one control FPGA (MAX10) and 12 Firefly transceiver modules
  - **Mezzanine test boards for Arria10 and Stratix10 devkits (INTERMEZZO):**
    - Production of 6 boards launched after production of 1 board that has been checked.
  - **Firmware work well organised around git functionalities**
    - First version released in June.
- **SRTM (Smart Rear Transition Module)**
  - Complements the LASP with data monitoring, providing electro-optics and processing.
  - Test cards will allow to tests all LASP/SRTM connector interfaces, soon to be submitted
  - Firmware tested on devkit

LASP routing and placement



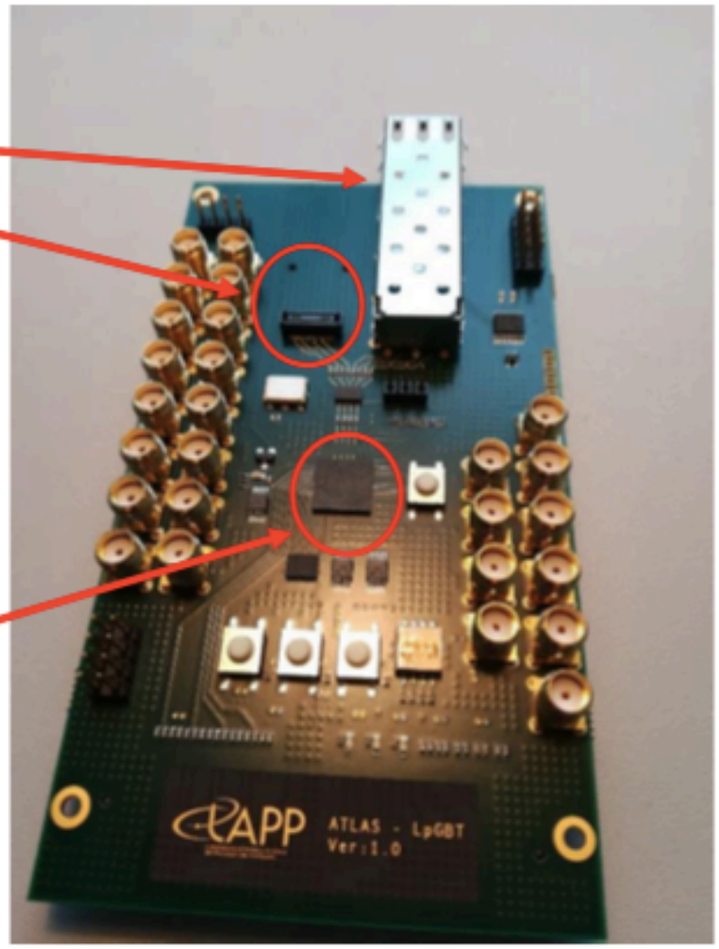


SRTM firmware test on devkit

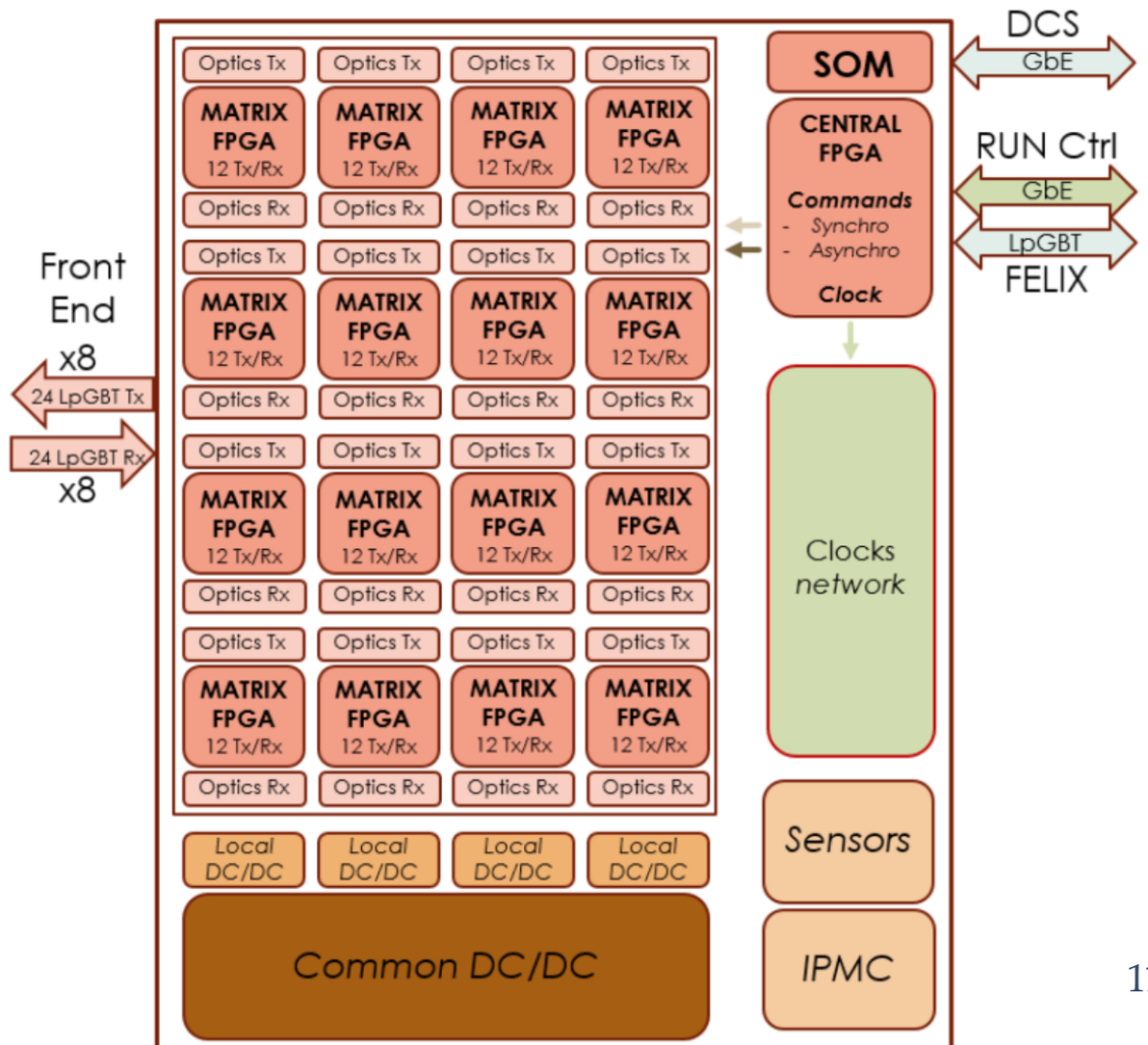
Off-detector: LAr Timing System

- **LATOURNETT: distribution of trigger timing and control signals + configuration and monitoring of FEB2 and calibration boards.**
  - **Design in early stage, specification review in the fall**
  - **Firmware development ongoing on FPGA Cyclone10 DevKit**
    - test of communication with lpGBT mezzanine test card

Test on Cyclone10 devkit



LATOURNETT board schematic



Summary

- **Most of the ASICs developed for the ATLAS LAr HL-LHC upgrade are in final pre-prototype stage**
  - Proton irradiation testing is in most case the last step toward validation of the technology
- **Integrated board designs are starting: FEB2, calibration board, off-detector boards.**
  - slice test will be done with a FEB2 pre-prototype with 1/4 channels that allows to test powering/all ASICs/data flow/communication end of 2020
- **Pandemic situation has caused a few month delays in several parts of the project**
  - Especially irradiation testing have been delayed
- **But still on track for an installation during 3rd long shutdown and solutions found to continue testing the devices**
  - Remote access to data acquisition, test bench moved to people's homes