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Upgrade of the ATLAS Muon Trigger for the HL-LHC

Tuesday, 28 July 2020 17:45 (15 minutes)

The present Level-1 Muon Trigger System of the ATLAS experiment will be upgraded for the HL-LHC to the Level-0 (L0) Muon Trigger with increased trigger latency of 10 ms and output rate of 1 MHz. The longer buffers in the front-end allow for more complex processing of the data, maintaining a high trigger efficiency even at highest event rates. For this purpose, the Sector Logic (SL) boards processing data from the RPC and TGC trigger chambers, is complemented by the NSW and MDT Trigger Processors processing respectively the information from the NSW trigger chambers and the MDT precision tracking chambers. To operate the future L0 Muon Trigger, the entire front-end electronics for the RPC, TGC and MDT chambers will be upgraded to cope with required rates and latencies. All RPC and TGC hit data will be transmitted from the front-end boards to the SL and the MDT hits to the MDT Trigger processors in a trigger-less mode over high-speed optical links. The low-resolution coordinates of the muon track hits supplied by the RPC, TGC and NSW trigger chambers will be used as a seed for the MDT Trigger Processors. These seeds provide Regions of Interest (RoIs) and bunch crossing identification. The MDT Trigger Processor assigned to a given sector of MDT chambers then only considers the MDT hits in a RoI, allowing for a large reduction of the relevant data volume. Hits in a RoI, together with the coarse track direction supplied by the trigger chambers, are fed to the MDT Trigger Processor to reconstruct a muon track segment in each MDT chamber and combine the segments into a muon track with significantly improved transverse momentum resolution. The much higher accuracy of the MDT hit coordinates (˜0.1 mm) compared to the ones supplied by the primary trigger chambers (20-30 mm), leads to a reduction of the single muon trigger rate by about a factor 3. The MDT Trigger Processor returns the measured pT to the SL for the final muon trigger decision. Upon a L0 trigger accept, it also transmits the MDT hits to the read out system (FELIX) for the final storage. The realisation of the MDT Trigger Processor imposes several technical challenges. To maintain the latency budget, the communication with MDT front-end electronics, the SL and the read out system must be performed via a large number high-speed optical links. The identification of track segments in the RoI also needs fast processors and firmware, which is robust against all possible hit patterns. A hardware demonstrator of the MDT Trigger Processor, based on state-of-the-art FPGA and SoC technology, is currently under production. It is implemented as an ATCA board consisting of two separate modules, the Service Module responsible for the board infrastructure and the Command Module for the data processing. The presentation will cover the description of the new L0 Muon Trigger System and the status of the firmware and hardware development for MDT Trigger Processors.

I read the instructions

Secondary track (number)

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