Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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Outline

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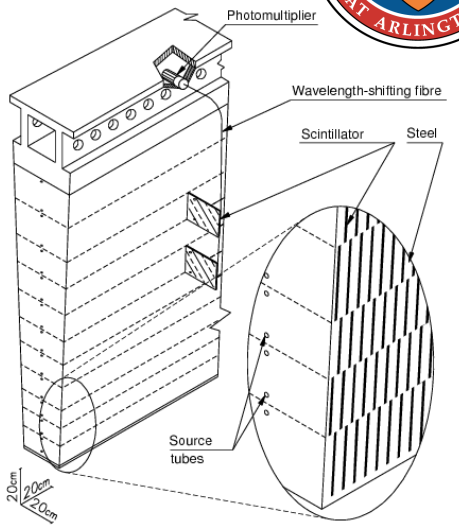
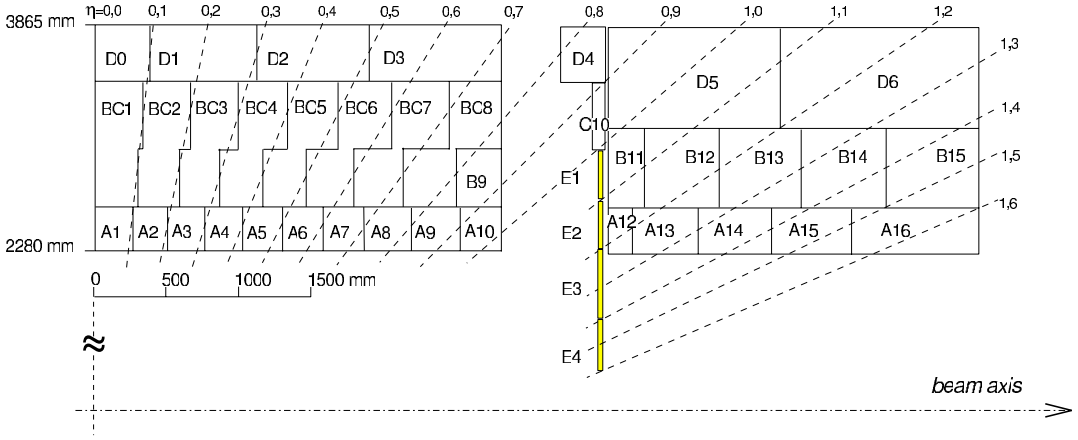
- Overview of Tile Calorimeter Upgrade for HL-LHC
- Expected performance
- Tile Calorimeter Components
- Test Beam Results
- Demonstrator Insertion
- Summary

ATLAS Tile Calorimeter

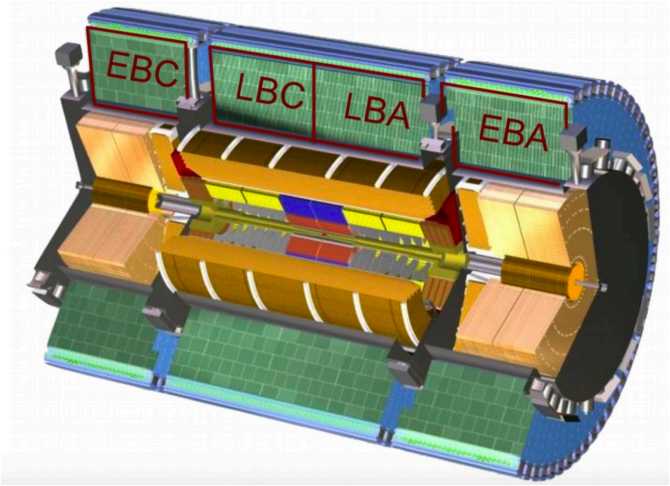
- Tile Calorimeter is a hadronic sampling calorimeter with steel absorbers and plastic scintillators
- Charged particles produce light in plastic scintillators
- The light is delivered to PMTs through WLS fibers
- Readout is grouped into pseudo-projective geometry cells (each cell is read out by two PMTs)
  - Around 5,000 cells and 10,000 PMTs
- Calorimeter is composed of one long barrel and two extended barrels



Tile Calorimeter wedge module



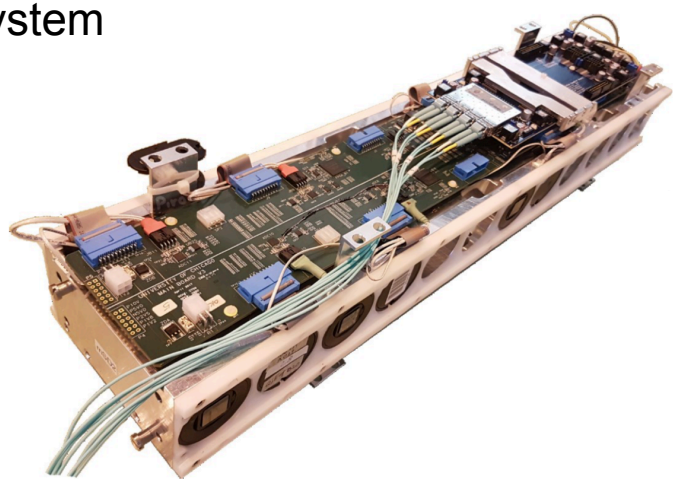
Map of Tile cells: showing tower structure



Drawing of Tile Calorimeter

Overview of Tile Cal Upgrade

- Complete replacement of front-end electronics to provide continuous readout of all channels at 40 MHz (fully digital trigger readout)
- New back-end electronics compatible with new trigger and DAQ system
- Replacement of around 10% of PMTs associated to the most exposed calorimeter cells
- High voltage regulation done remotely in the counting rooms
- Low voltage is being regulated locally on front-end electronics using POL regulators
- Increased radiation hardness of electronics for high luminosity environment
- Using mini-drawers inside the modules to improve accessibility and robustness of the system

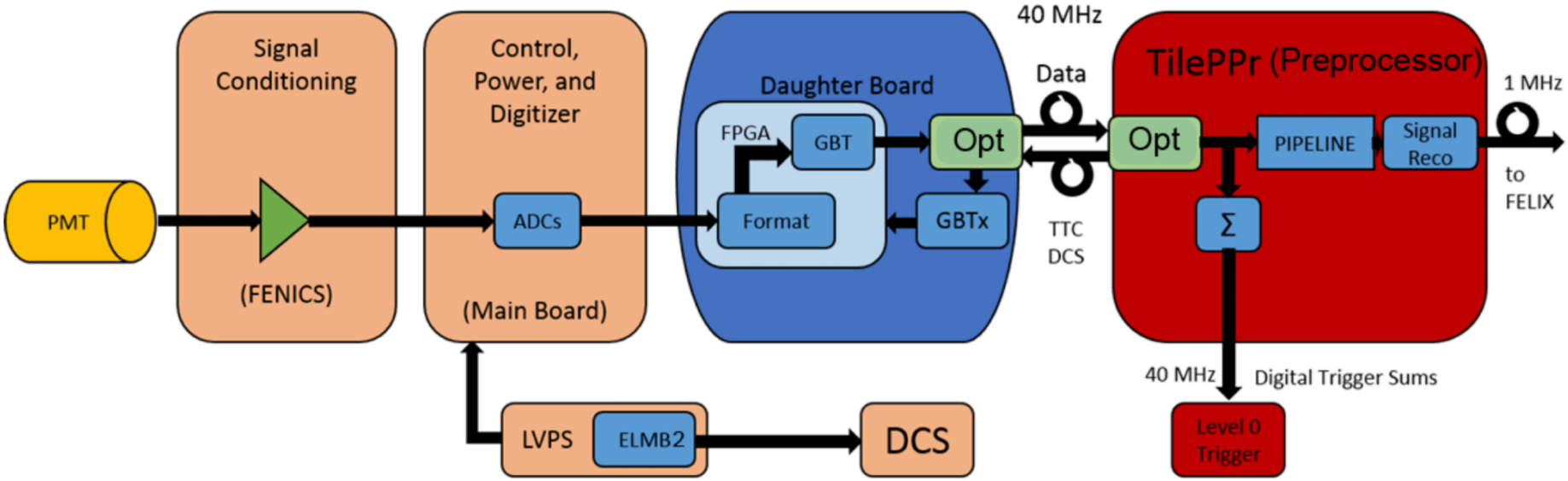


One Mini-drawer of the TileCal

Expected Performance

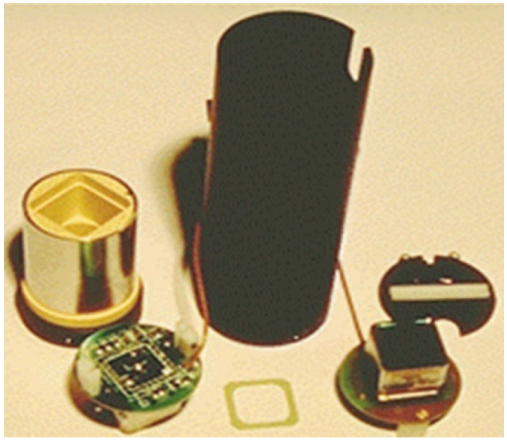
- A fully digital trigger system with higher granularity and precision, compared to the current system will be used
  - All data will be sent to trigger system at 40 MHz
  - The system requires 2048 optical links at 9.6 Gbps from on-detector electronics to the counting rooms
- The effective dynamic range of digitisation will be increased from 16 bits to 17 bits
- On-detector electronics must be tolerant to radiation effects
  - Specially, for on-detector FPGAs, sensitive to single event upsets, triple redundant scheme is considered
- Many redundancy levels have been considered
  - Mini-drawers are logically split into two sides, and each cell is read out by two independent PMTs
  - In case of a failure, the dead region would be one-eights compared to the current system
- Ageing and significant degradation of some of the PMTs is expected
  - 768 PMTs covering the most exposed cells will be replaced

Readout Electronics

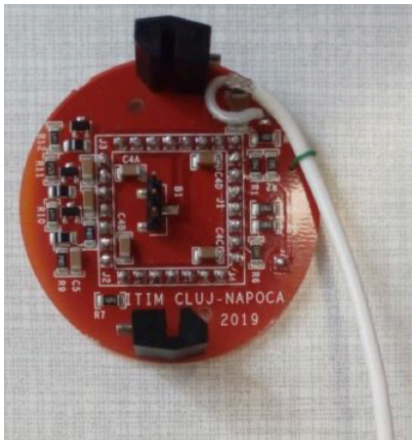


PMT Blocks/HV Dividers

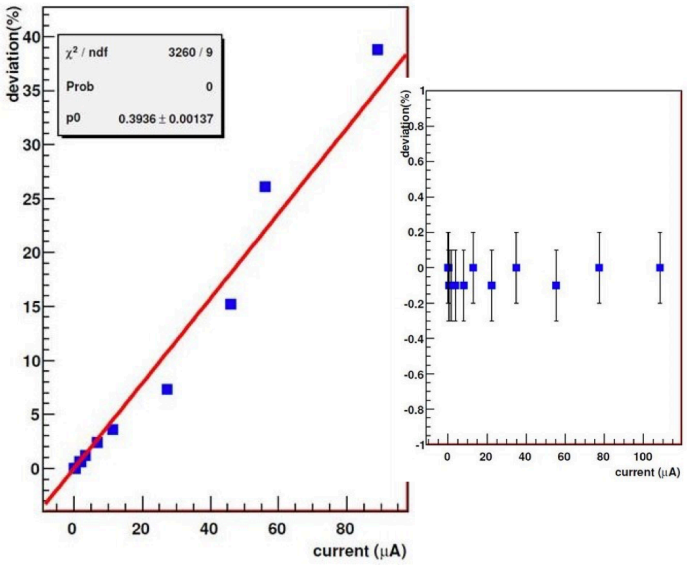
- PMTs are located inside the PMT blocks, converting the light to electric signals
  - Around 10% of the PMTs will be replaced due to ageing
- HV dividers are sitting on the end of PMTs, dividing the input HV and provide voltages for PMT dynodes
- Active dividers are replacing passive dividers to provide better linearity for HL-LHC
  - Active dividers contain transistors and diodes in addition to passive components
  - The DC current can go from a maximum of ~8 μA in LHC to 40 μA in HL-LHC
  - Nonlinearity in passive dividers could go up to ~15% (below 1% for active dividers)



PMT block and associated components



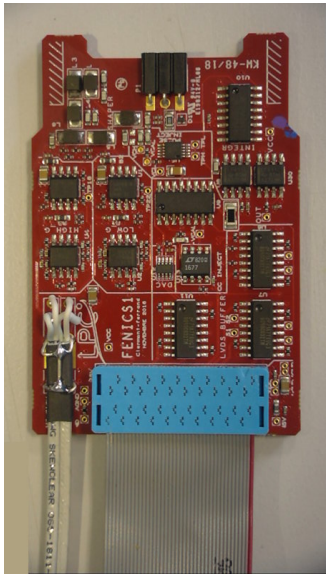
Latest version of active divider



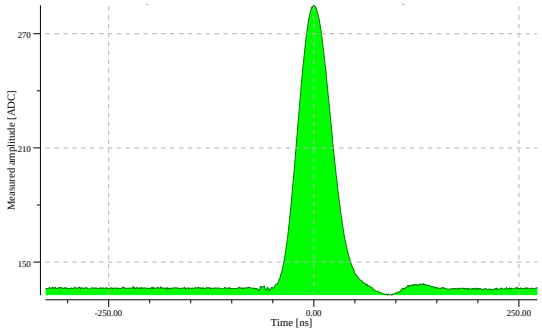
Experimental comparison of nonlinearity for passive dividers (left) and active dividers (right)

FENICS

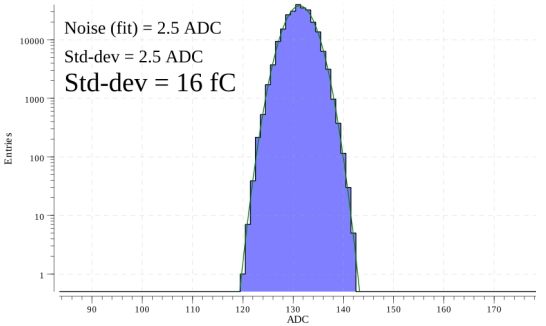
- Located on top of active dividers, are FENICS boards, which
  - Shape PMT pulses and prepare them for the ADCs on mainboard by 2 gains
  - Provide slow integrator signal for calibration and luminosity
- The gain ratio of the outputs of FENICS is 40 (gains of 0.4 and 16)
  - Selected gains provide a saturation limit of 1050 pC (1 TeV) for the low gain signal
- FENICS boards are replacing the old 3-in-1 cards, which also had analog trigger output signal
- Pulse shaping and noise levels of FENICS are shown



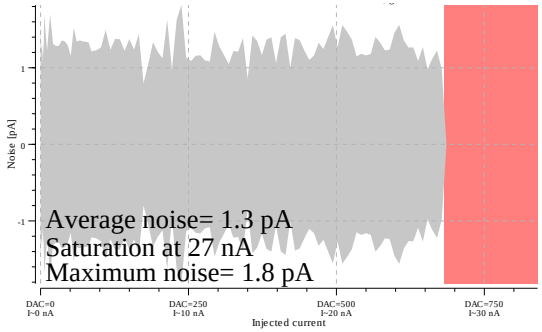
FENICS board



Low gain output of FENICS for a signal with 37.4 pC PMT charge



Distribution of pedestal for high gain

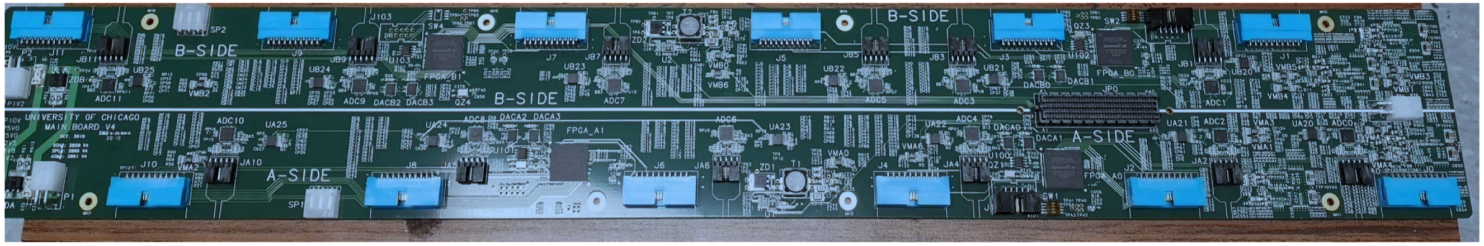


Noise as a function of injected current in integrator with highest gain (150 MOhm)

Mainboard and Daughterboard

- Located inside modules of detector, the mainboard hosts a daughterboard. It receives data from FENICS, digitises it, and passes it to the daughterboard
- Two 12 bit ADCs provide a dynamic range of 17 bits for signals
- The mainboard was used in the test beams and its new version was designed, providing voltage and current monitoring for counting rooms
- Located on top of the mainboard, daughterboard formats the data (including DCS (Detector Control System) data), and sends it to the back-end electronics through optical links
- The optical modules on daughterboard provide a data rate of 9.6 Gbps for the total 4096 optical links (2048 + 2048 for backup)
- After using the daughterboard in several test beams, the new version is being designed with new FPGAs (Kintex Ultrascale), triple mode redundancy, and improved routing from mainboard ADCs
- Both mainboard and daughterboard are composed of 2 identical sides to provide redundancy

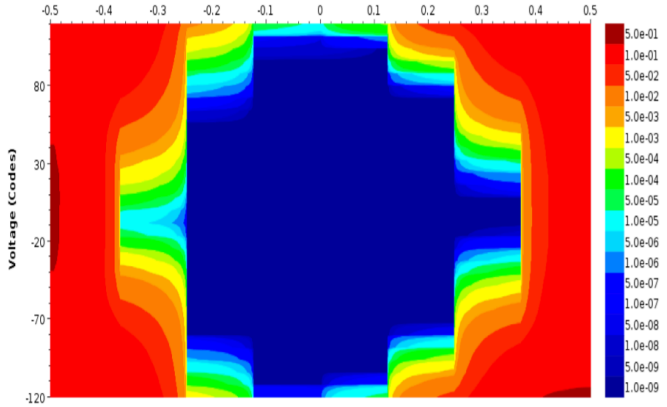
Daughterboard with two identical and redundant sides



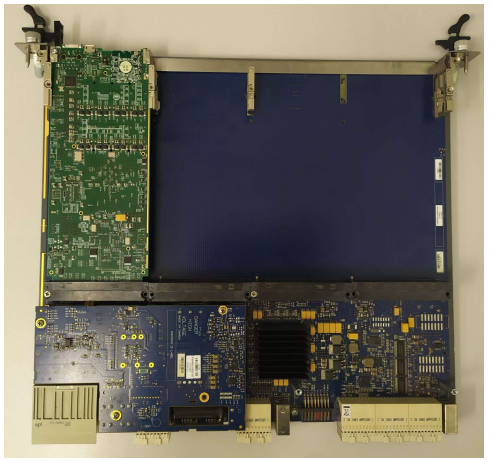
Mainboard (Each side is corresponding to 6 PMTs out of 12 PMTs of 6 cells)

Preprocessor

- Located in counting rooms, preprocessor (PPr) receives data from detector and computes each channel energy and time
- Unlike current system with on-detector data pipelines, the pipeline buffers are moved to PPr (closer to trigger system for lower propagation delay)
- PPr is composed of CPMs (Compact Processing Modules) hosting by an ATCA carrier board
- After successful tests of PPr prototype in the test beams, which was under development since 2015, first CPMs were made in 2019 and tested successfully using a motherboard
- A custom ATCA carrier is also designed to host the CPM and provide connection between the CPMs and Trigger and Data AcQuisition interface board (TDAQi)



Performance of the designed CPM: Eye Diagram of FireFly optical transceiver at 9.6 Gbps

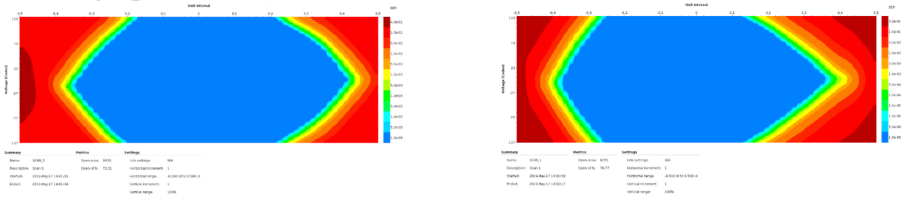


One CPM hosted by ATCA carrier

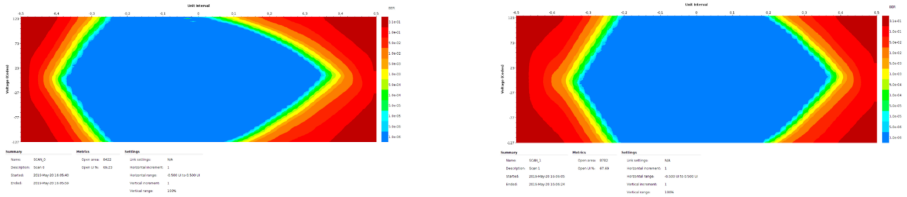
TDAQi

- Sitting inside an ATCA crate, TDAQi receives channel energies from the PPr and computes cell energies and quantities to be passed to the Level 0 trigger
- Digital trigger sums in TDAQi are replacing analog trigger sums, which was being done on-detector
- First version of TDAQi was made in 2018 and was used to do several tests
  - Before that, PPr prototype was performing TDAQi tasks
- Tests were done to verify the performance of board using optical links (FireFly optical modules and SFPs)

FireFly @ 11.2 Gbps, PRBS31



SFP @ 9.6 Gbps, PRBS31

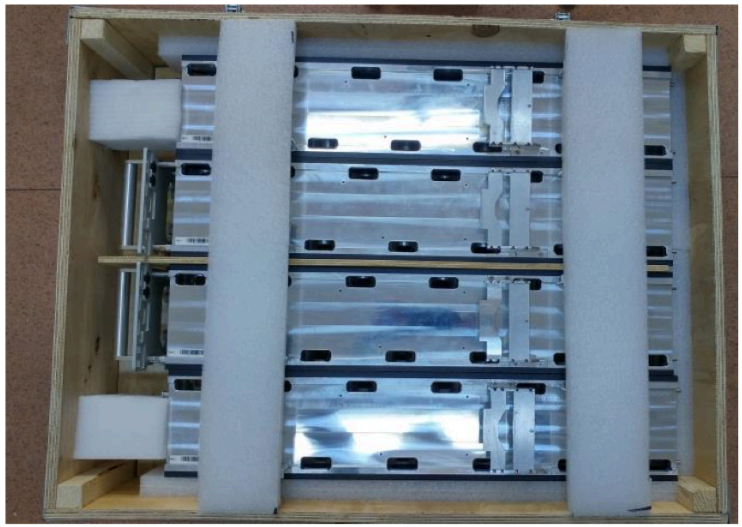


Performance of designed TDAQi: Eye diagram of optical modules

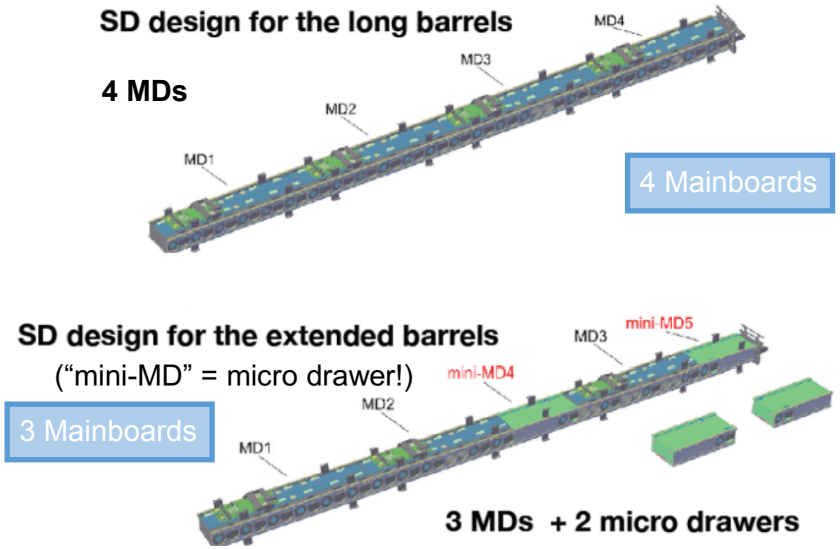
First version of TDAQi

Mechanics

- All of the front-end electronics are placed on mechanical structures called super-drawers, to be inserted inside the 3 meter long girders
- Mini-drawers have been designed with half of the length of the current drawers, which provides more accessibility and robustness, and reduces the scale of a possible single point of failure
- Super-drawer design is different for long barrels and extended barrels, as the number of PMTs is less for the extended barrels
  - Tailoring design for extended barrel modules, will decrease the number of front-end electronic boards



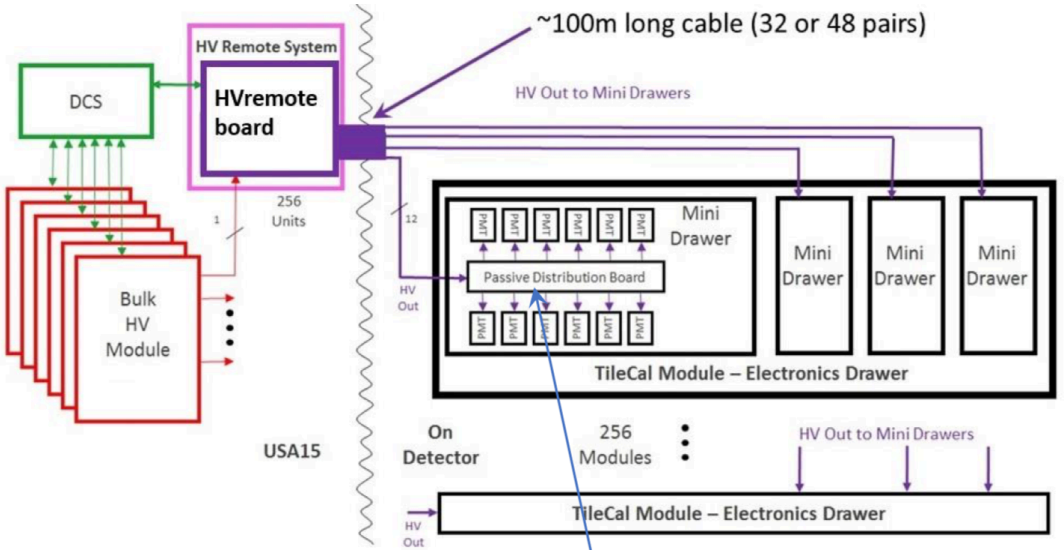
Recently produced mini-drawers



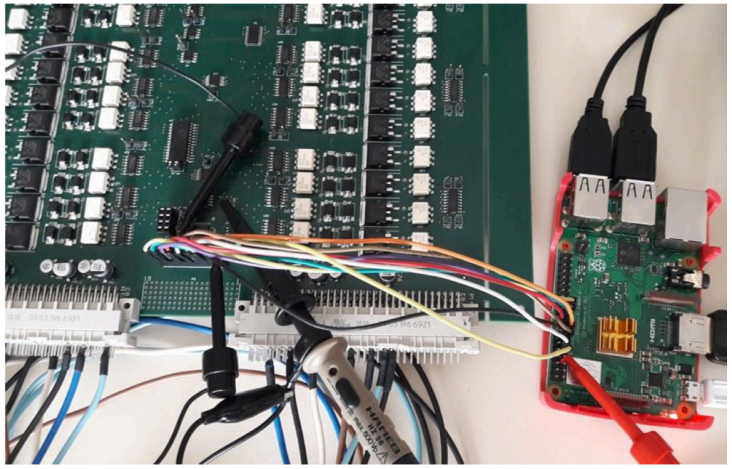
Composition of super-drawer for long and extended barrels

High Voltage Distribution System

- HV regulation boards in the counting rooms provide regulated high voltage for individual PMTs considering requirements like noise, ripple, and temperature dependence
  - Unlike current system, the regulation is being done remotely, which eliminates the radiation hardness requirements and provides much better accessibility
- Each board provide 48 outputs for individual PMTs in each module
- Prototypes with 24 output channels were used in the test beams and prototypes with 48 output channels were made afterwards



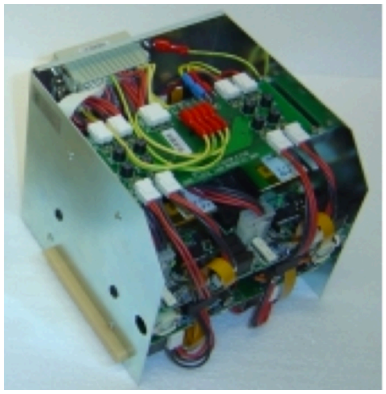
Block diagram of HV distribution system



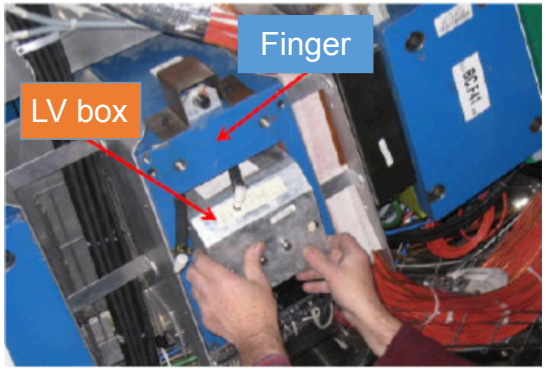
HV regulation prototype with 24 output channels

LV Distribution, Control, and Monitoring System

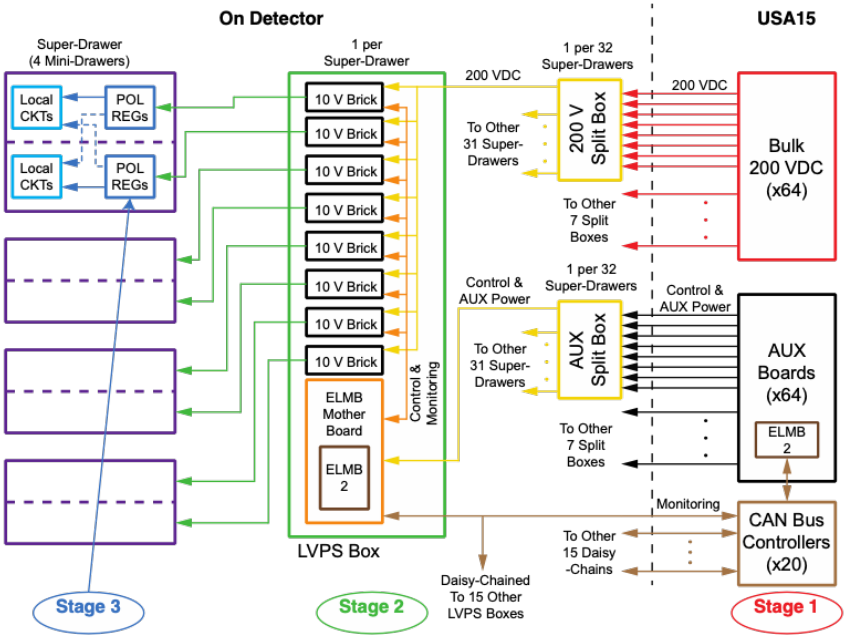
- Located inside the LV box in the finger of module, LVPS bricks convert the input 200 V to provide 10 V for the front-end electronics, which is then converted to different voltages by POL regulators (3 stage system, unlike current system)
- Monitoring of the bricks is being done by ELMB (Embedded Local Monitoring Board), hosted by an ELMB mother board inside the LV box
- Control of the individual bricks is being done via tri-state control signals by the off-detector Auxiliary board and through the recently designed robust ELMB motherboard



LVPS bricks and other components inside LV box



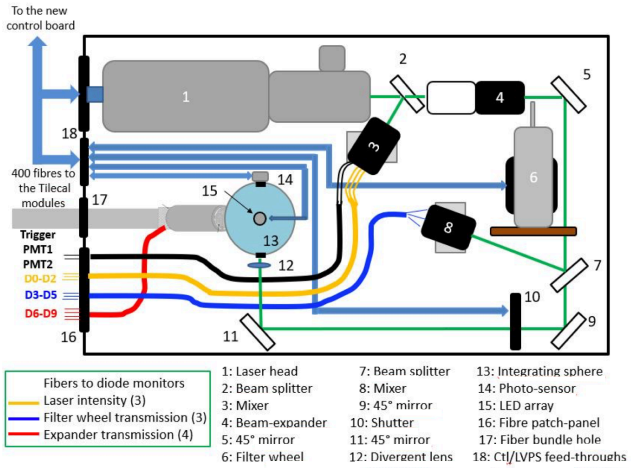
LV box inside the finger



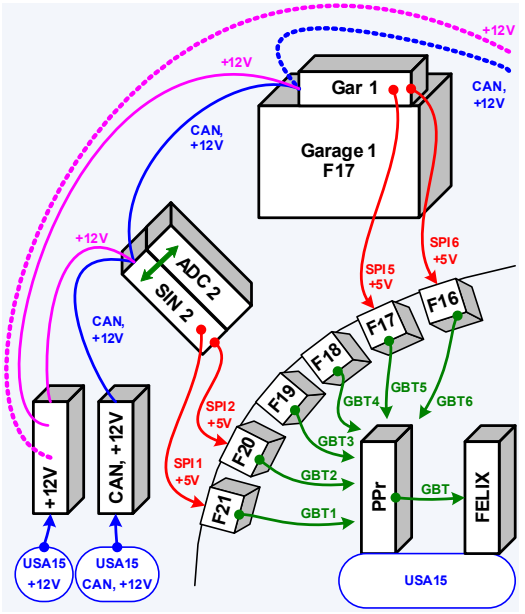
Block diagram of the LV distribution system

Calibration Systems: Cesium and Laser

- The two main calibration systems of TileCal are Cesium and laser, which are used to calibrate the scintillators and PMTs, respectively
- Cesium system, composed of a ^{137}Cs source, driven by a liquid through all tiles, to deposit known energy on the cells
- New control boards of the Cs system are designed with higher radiation tolerance and new type of interface with DCS through optical links
- Laser system, uses 400 clear fibres (~100 m long) routed to all PMTs, to feed the laser light to the modules
- In addition to new board for control and interface with TDAQ and DCS, the light mixer in the current system will be replaced by an integrating sphere to add controlled source of DC light to simulate minimum bias events



Layout of the proposed arrangement in the optics box of the upgraded laser system



Block diagram of the Cesium calibration system

Test Beam Results

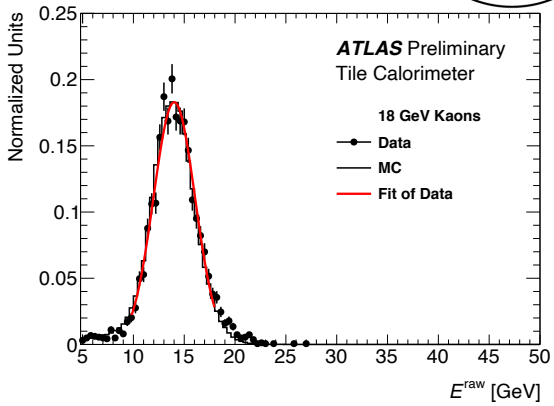
- Some results are shown, with SPS beams and data taken with prototype HL-LHC electronics
- Distribution of reconstructed energy is obtained for hadrons at different beam energies
- The shower energy E^{raw} is the sum of energy deposited in the calorimeter cells
- Lower mean energy is seen due to non-compensating nature of the calorimeter
- Energy response ratio and fractional resolution can be found for each particle at a specific energy, respectively, as

$$R^{<E^{\text{raw}}>} = \frac{< E^{\text{raw}} >}{E_{\text{beam}}}$$

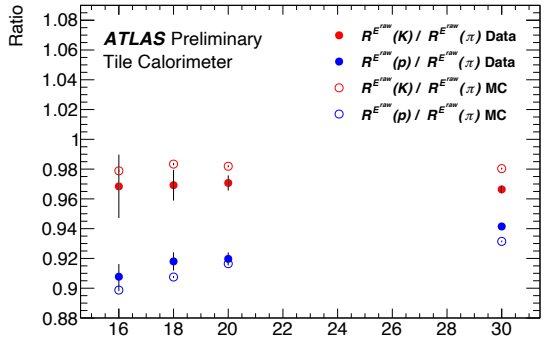
$$R^{\sigma^{\text{raw}}} = \frac{\sigma^{\text{raw}}}{E_{\text{beam}}}$$

- Measured kaon (proton) response is around 3% (8%) smaller than pion response
- Measured energy resolution of kaons (protons) differ by around 4% (12%) from that of pions

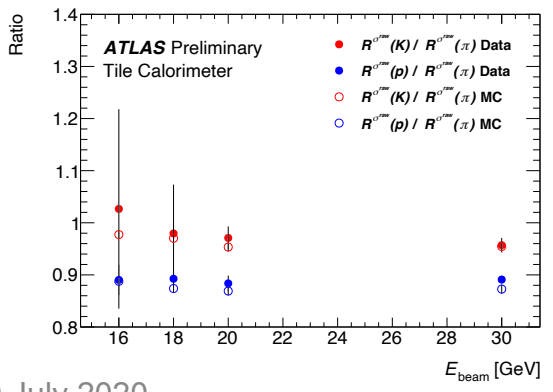
Distribution of energy for 18 GeV Kaons



Energy response ratio for hadrons



Fractional resolution for hadrons

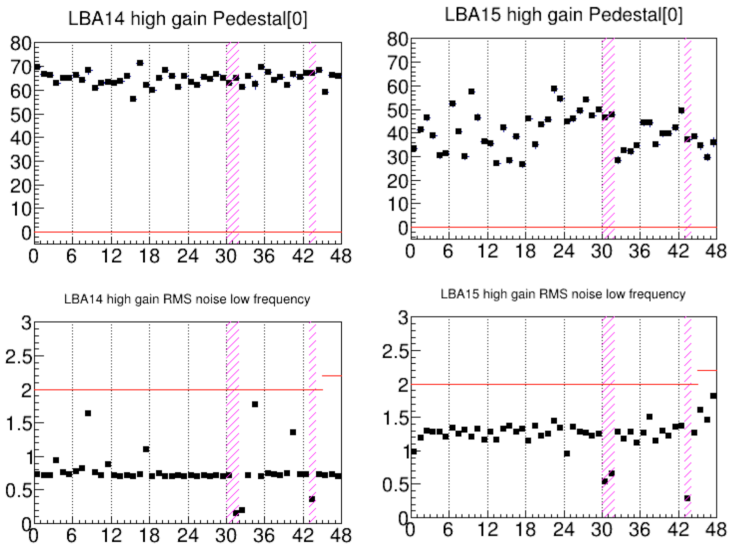


Demonstrator Insertion

- Demonstrator, a hybrid TileCal module with both analog and digital trigger signals was developed and used in several test beams
- It was inserted in the detector (single barrel module) in July 2019, composed of:
  - 4 mini-drawers in front-end: 45 PMTs with legacy 3-in-1 cards (instead of FENICS) and active HV dividers, mainboard, daughterboard, adder base boards + trigger adder cards (from the legacy system)
  - PPr demonstrator inserted in ATCA carrier in the counting rooms
  - HV remote system and upgrade LV system
- The demonstrator is now integrated in TDAQ
- Performance comparison shows lower noise in the demonstrator with respect to the legacy modules thanks to larger dynamic range

Demonstrator insertion in 2019

Noise comparison for demonstrator module (left) and legacy module (right)



Summary

- The design of the upgrade is based on the present (successful) experience
- Energy resolution and detector granularity will be preserved
- Readout resolution, sensitivity, and dynamic range are slightly improved
- Special attention is given to redundancy, reliability, and radiation hardness
- Fully digital readout will allow for using greatly enforced trigger capabilities
- Improved monitoring and calibration capabilities are also enforced
- Extensive tests of the design with the SPS beams since 2015 have been performed
- Hybrid demonstrator module is backward compatible with legacy modules and will be included in LHC Run 3
- The project has entered into component production phase