Implementation of large Imaging calorimeters

Vincent Boudry
Institut Polytechnique de Paris

for the CALICE collaboration

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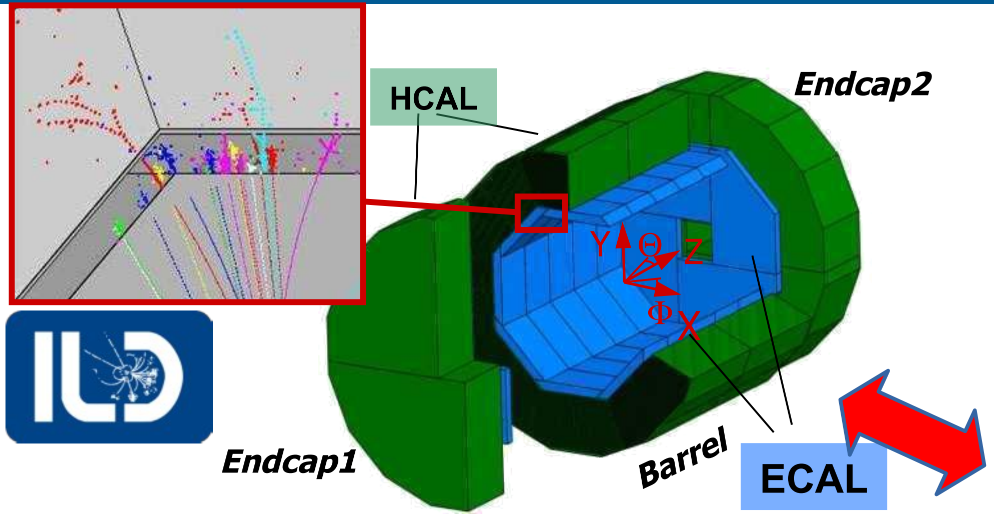
TNA support + WP14

Ultra-Granular Calorimeters for Higgs factories: ILD, SiD, CLIC-dp, CEPC-baseline, FCC

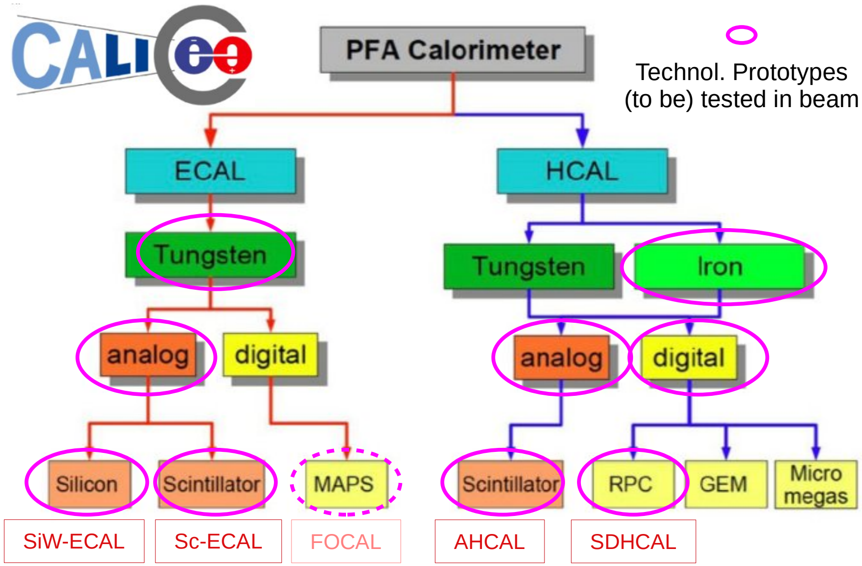


Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (*E, (θ,ϕ), t*)
- Particle Flow requirements:
  - Extremely high granularity
  - Compactness (density)

Highly-Granular Calorimeters:

- ECAL @ R = 150–180 cm, |Z|= 200 cm, Thickness~25 cm
  - cell size = 0.5 – 4 cm square (Si) or strip (Sc)
  - 25 – 50 Layers
  - 8 – 70M cells
- HCAL @ ECAL +3 cm, Thickness ~ 150 cm
  - Cell size = 1 – 3 cm, Gas (GRPC) or Sc



Electronics & DAQ

Ωmega ASICs:

- A set of ASICs adapted for all CALICE large scale prototypes
  - Gradual improvement
  - Purely digital DAQ
- adapted to ILC conditions
  - **low power** consumption using **power-pulsing (~1%)**
  - **low noise** pre-amp, dual gain 12-bits ADC, ns TDC
  - **self-trigger** with local storage, **delayed** digitization and **read-out**
  - **high integration** (36–64 channels), daisy **chaining** config and readout

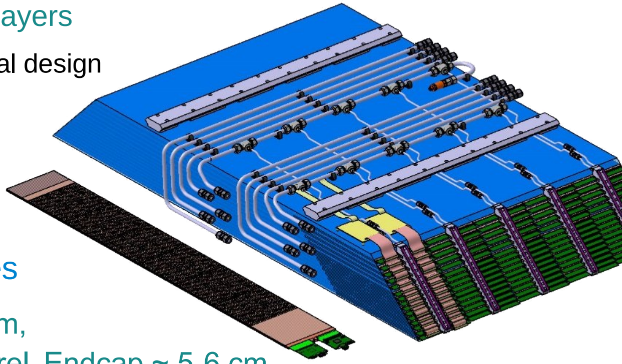
R&D:

- will required update for final ILC integration:
  - full zero-suppression, I2C bus, new technology
  - Improvement of Timing ? Learning from CMS-HGCAL ASIC
- new scheme for circular colliders (power, readout)

~3^{+} years of dev

Technical requirement on prototypes:

- Integration in cassettes 150 – 300 cm long
  - 12k – 27k cells (200–500 ASICs), power pulsed
  - sensitivity to mip signal (tracking)
  - uniformity, stability, linearity
- Reproducibility
  - Typically ~20–50 layers
    - will be ~ 10^4 in final design



DAQ:

- Low power,
  Small size interfaces
  - ECAL-HCAL = 3 cm,
    HCAL–Coil or Barrel–Endcap ~ 5-6 cm
- Single side readout

Pulsed Powering in 3–4T field…

- Passive cooling

Validation of prototypes: common goals

Scientific goals:

⇐ many already achieved with physical prototypes
(see next presentation from W. Ootani)

- Energy & Time measurements:
  - Linearity & Resolution to single e, π in 1–200 GeV (⇒ input to jet simulations for PFA)
  - Saturation effects
- 5D Shower profiles
- Particle Flow Algorithm (PFA) tests : shower separation, reconstruction, identification

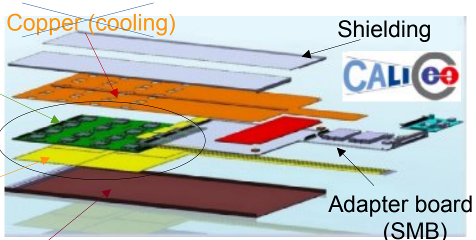
Technical goals:

- Operation of **scalable design** with **power-pulsing**
- **Low-Energy Calibration** with muons **(mips)** position scans, [**High Energy: e, π**]
  - **Signal-to-noise of trigger** (limited memories)
  - **Uniformity**: Efficiency, Mean response (Light Yield, Mip Peak, Multiplicity)
  - Input for **realistic digitization models** ⇒ input to simulation: prototype and Particle Flow
- **Scientific goals (again):** improved granularity, design, etc...
- Running as close as possible to **ILC mode** (200 ns BC), relaxed mode for practical reasons (typ. 4 μs BC)

Silicon-Tungsten ECAL

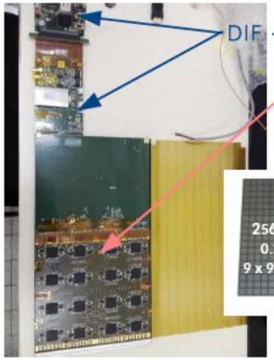
Prototypes for the ILD/ILC

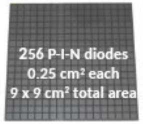
- cells of ~5×5 mm², density = 2.6k–3k cell/dm³
- Ωmega's Skiroc2/2a, 64 ch ASICs
- 25 μW/ch with 1% Power Cycle (0.3W for proto)

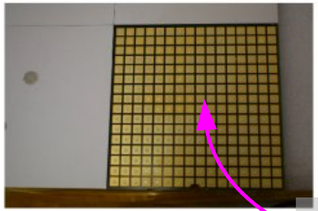


Technological prototype

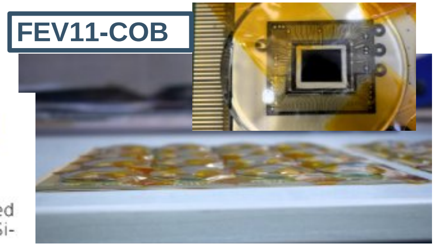
- "Physical prototype" (2005–11): 10k cells, ρ =1.5k cell/dm³
- S/N = $MPV_{mip} / \sigma_{Noise} \geq 10$
- Stacks with **15+7** layers of 1024 ch (15360 cells in a single readout)
  - mix of PCB versions (v10, 11, 12, 13),
    ⊗ packaged and on-board ASIC's
    ⊗ 320, 500, 650 μm Silicon wafers
  - New Integrated DAQ, 1st prototype toward ILD-like (≤3cm)

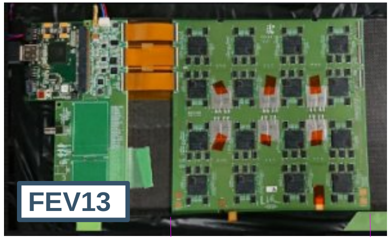




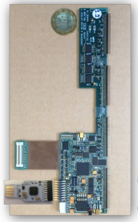


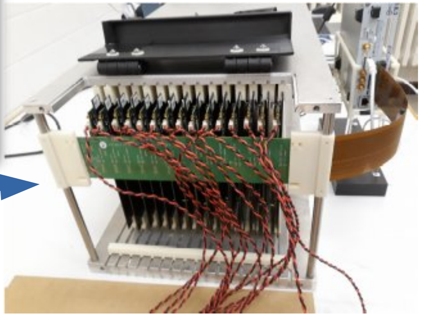
Glued, w floating GR

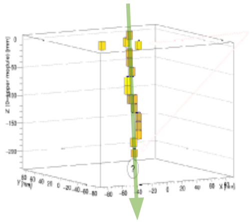


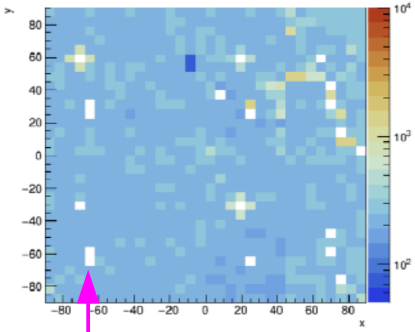


183mm









Noisy cells removed ~ 1–3 %

Silicon-Tungsten ECAL: Developments

Improvement in design

CERN 2015 “naked FEV11” (320 µm)

S/N_{ADC} ~ 16–17

Ring X-talk / 10 wrt Phys. Proto.

CERN 2017: 7 FEV11 (320 µm)

S/N_{ADC} ~ 20.3 ± 1.5

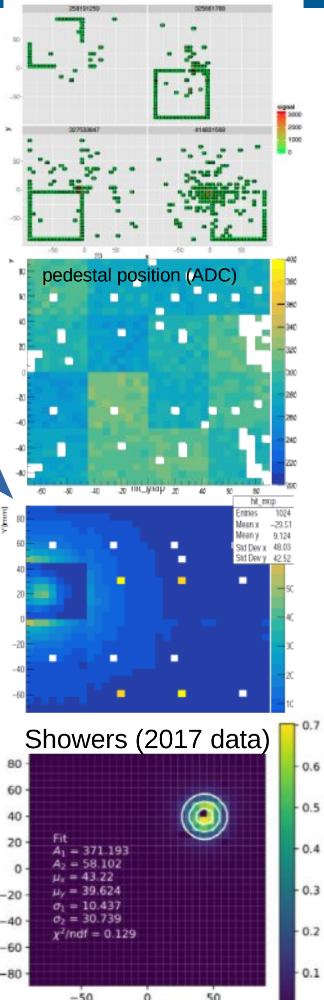
8% masking, 1T operation

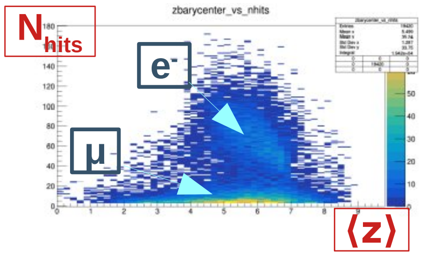
DESY 2018: 7 FEV11 + 1 FEV13 (650µm)

S/N_{ADC} ~ 30.3 – 40;

S/N_{TRIG} ~ 11.6±0.7 ⇒ Cut ~ 1/3 mip @ 4σ

CERN 2018: 6 FEV11 + 4 FEV13 + 24 X_0 W



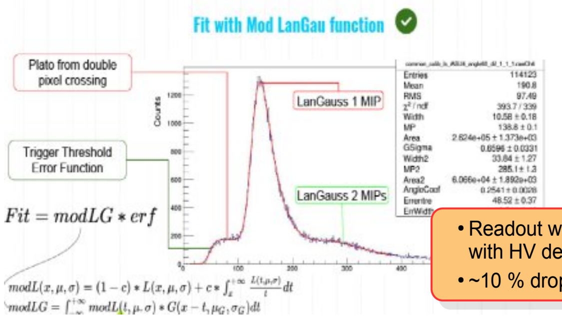


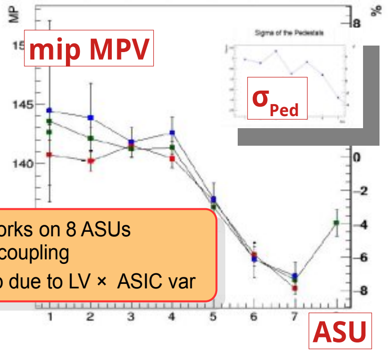
Ready for physical beam test

March 2020 † ⇒ Nov 2020 + 2021

Long Slab

– 8 ASU’s with baby wafers (2×2cm²)





R&D Highly Resistive Silicon Diodes:

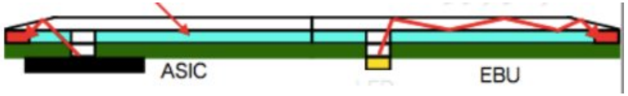
– Ref = Hamamatsu “Guard-Ring-less” design

– 6’’ Towards 8’’ (à la CMS-HGCAL) × 725µm ?

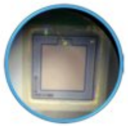
⇒ cost, design, perf.

Scintillator-Tungsten ECAL

Prototypes for the ILD/ILC & CEPC

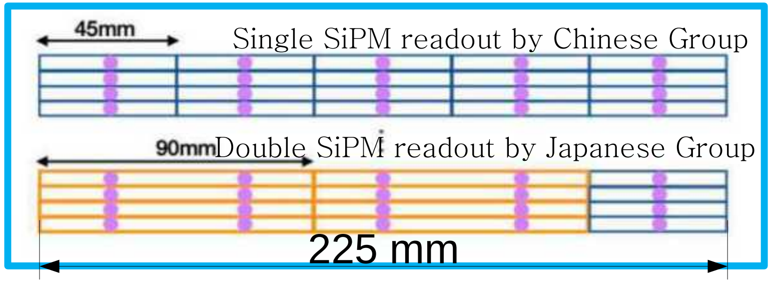


- Ωmega's Spiroc2e, 36 ch ASICs
- 25 μW/ch with 1% Power Cycle
- cells of ~5×45 mm², ρ = 450 cell/dm³



Baseline SiPM

Hamamatsu S12571-010P
- size: $1mm \times 1mm$
- pitch: $10\mu m$
- number of pixels: 10K



× 30

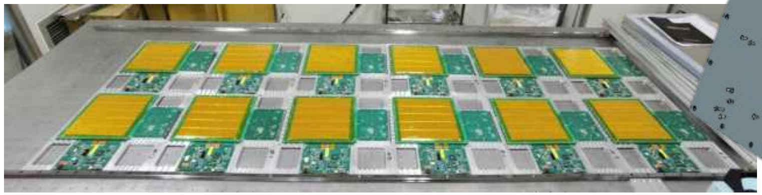
10μm & 15 μm SiPM

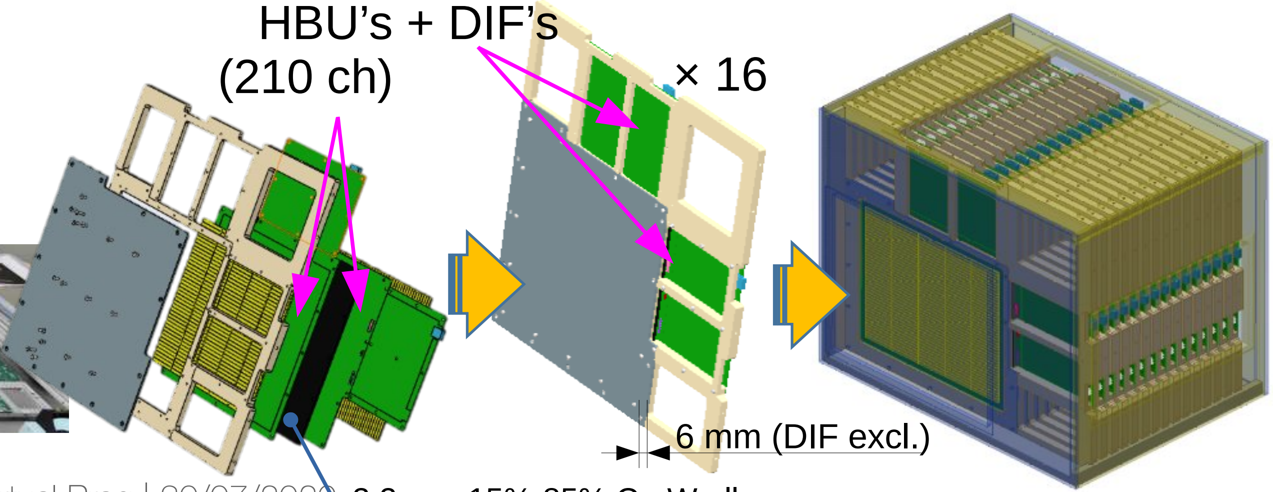
× 2

Technological prototype

"Physical prototypes" (2005–11, 2013–15)

- Stack with 32 layers ready
  - aging test made (48h @ 50°C)
  - being assembled

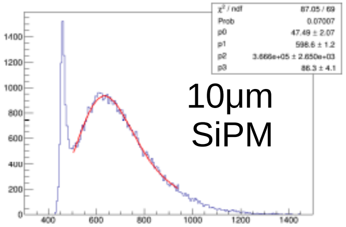


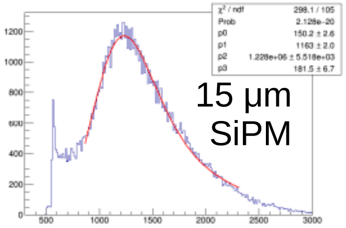


ScECAL: commissioning

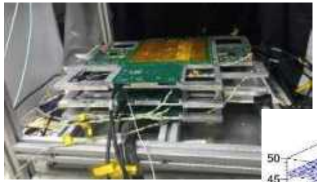
Sr90 Source

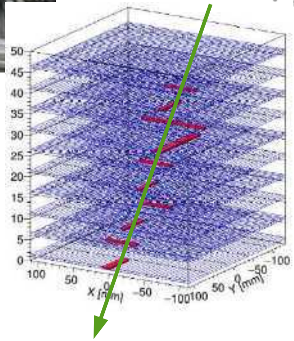
- 25 ns shaping
  auto-trig
  Landau ⊗ Gauss

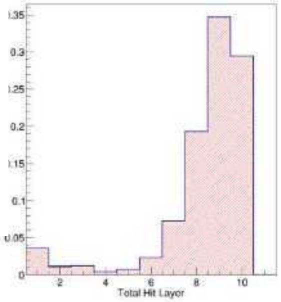




Cosmics test





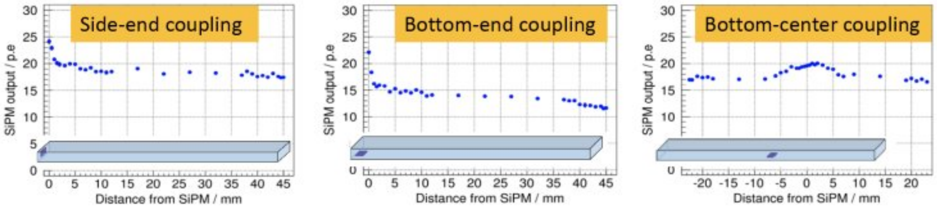


Beam tests

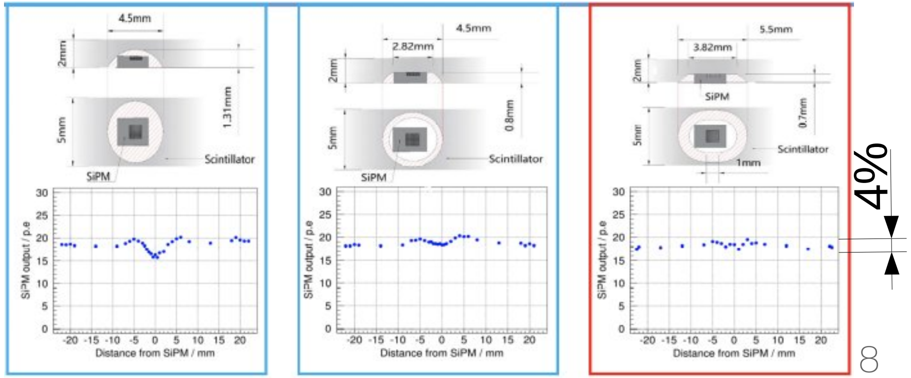
- DESY beginning of 2021 … if travel is permitted

R&D:

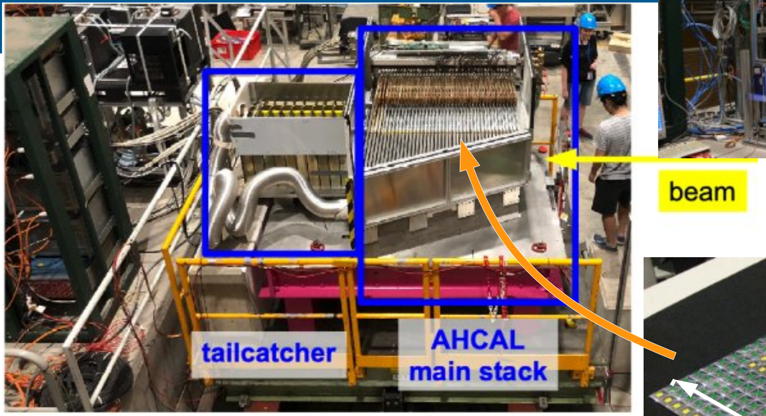
- Scintillator – SiPM coupling
  - non-uniformity ⇒ σ(E) ➚
  - SiPM position



- Groove form



Scintillator AHCAL



For ILC and CMS

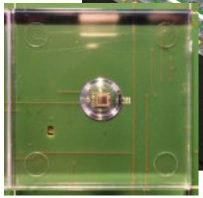
- ILC with Ωmega SPIROC2e
  - HL-LHC will be Ωmega HGROCv3
- 3×3 cm², density ~ 55 cells / dm³

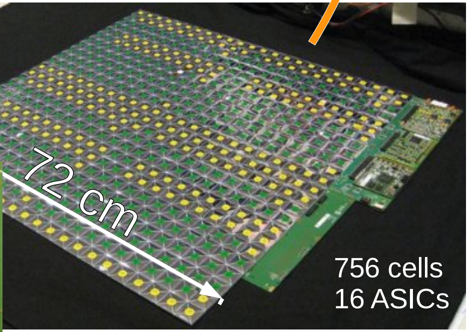
Technological prototype ≥ 2017

Physics prototype ~ 2006-11 (3×3 + 6×6 + 12×12 tiles)

- Uniform 3×3 cm² tiles (moulded) read by SiPM mounted on PCB
- 38 layers of 0,7×0,7 m², 22k cells
  - + additional layers of 6×6 cm²
- 2018: Stand alone tests and with CMS HGCAL
  - 4λ of stainless steel (1.7 cm ×38)

→ **Combined beam test with ECALs when ready**
→ **Stand-alone with full W structure**

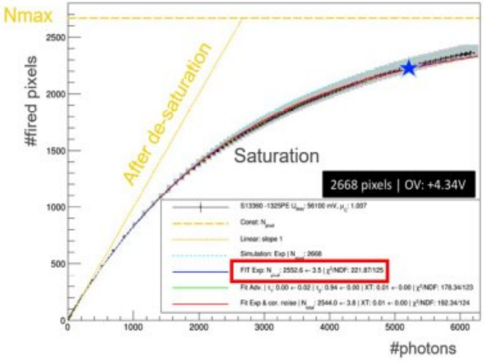




Online corrections: on SiPM's:

⇒ EM Lin & Resol.

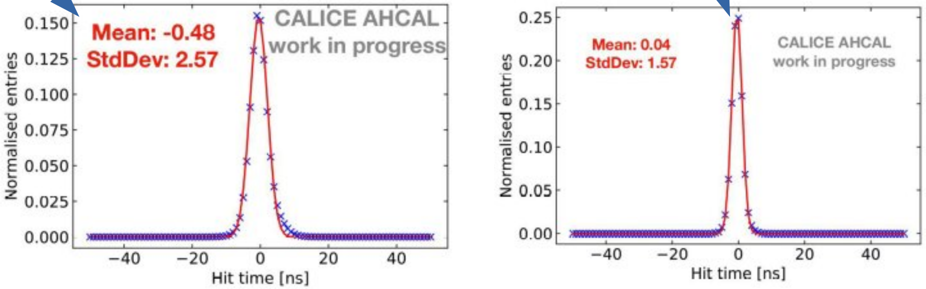
- Gain (Temperature, HV)
- Statistical saturation for $E_{hit} \geq 100$ mips ($N_\gamma \sim N_{pix}$)
  - Corrected for E≤350 mips



AHCAL analysis

New: Hit time correlation

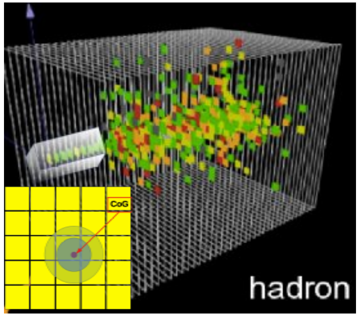
- Time profile from muons
  - SPIROC : double analog ramp → ADC
  - with clocks
    - at 250kHz (beam test mode) : σ ~ 2.6 ns
    - 5 MHz (ILC mode): σ ~ 1.6 ns

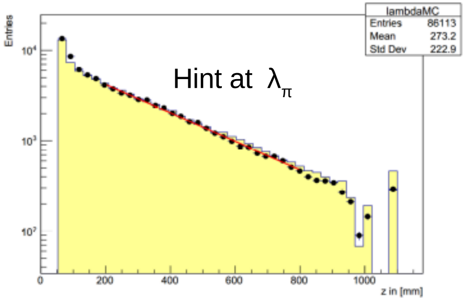


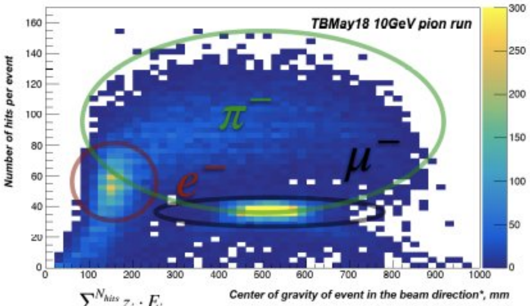
    - Goal: 1 ns in ILC mode

High Level Analyses:

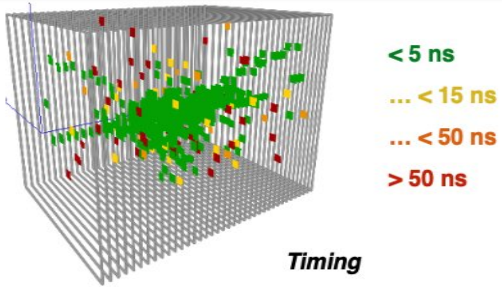
- Shower profiles & PFA tests (≥2011)
- Shower start, PID, $f_{neutrons}$ (time)



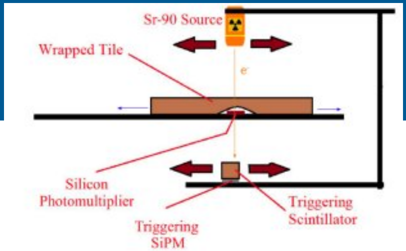


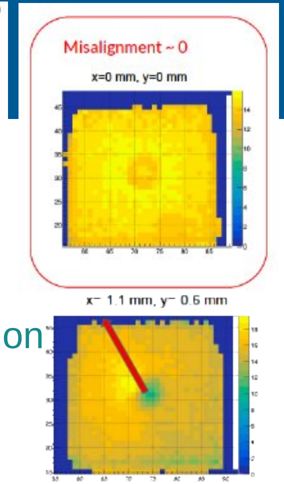


$$^* z_{CoG} = \frac{\sum_{i=1}^{N_{hits}} z_i \cdot E_i}{E_{sum}}$$



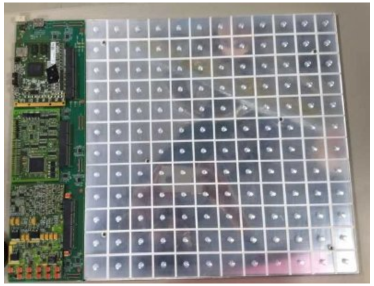
AHCAL developments



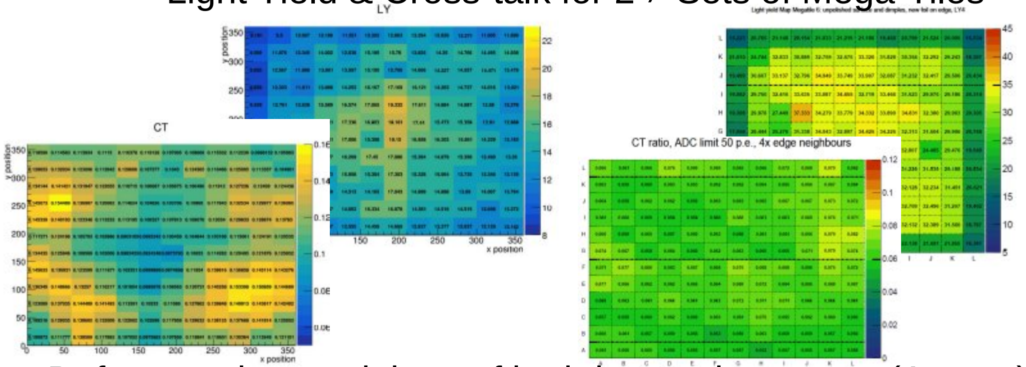


“MegaTiles” R&D:

- Single Scintillator tile with trenches of 3×3 cm²
- 2019 Beam test:
  - Light Yield, Mip resp, Optical Cross-talk
  - Larger Cross-Talk than in cosmics (mechanics)



Light Yield & Cross-talk for 2 ≠ Sets of Mega-Tiles

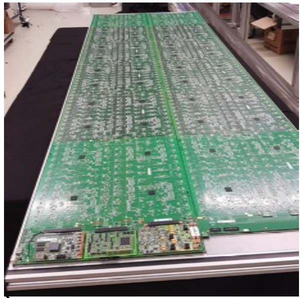


Defects understood; best of both in next beam test (August)

R&D

- Scintillators optimisation
  - Measurements ⇒ Realistic Simulation
- SiPM/MPPC evaluations
- ADC consumption (KLAUS Chip)

Long Layer



- 2×6 HBU’s OK in lab...
  - Goals:
    - 3×6 HBU’s (ILD) … in a test structure (absorbers)

CMS HGCAL:

- 1st PCB test in beam in August

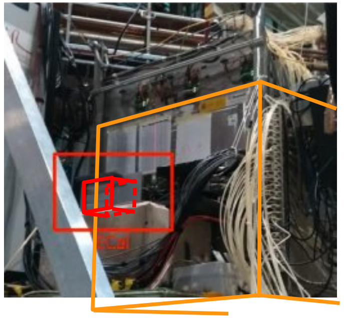
SDHCAL: Semi-Digital Gaseous HCAL

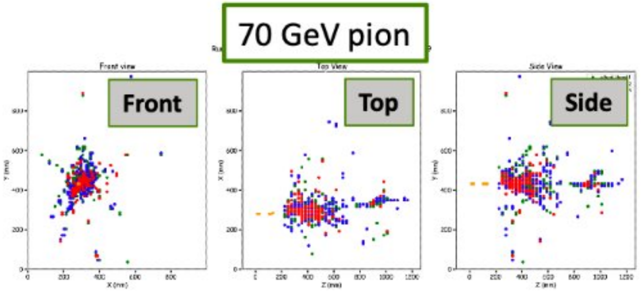
Technological prototype ≥ 2011

- Single and multi-gap thin GRPC's
- Cells of 1×1 cm², ρ = 380 cells/dm³
- Ωmega HARDROC2
- 48 layers of 1×1 m², 460k cells, $6\lambda_I$ (2 cm Stainless steel)

Semi-Digital calorimetry: 3 thresholds

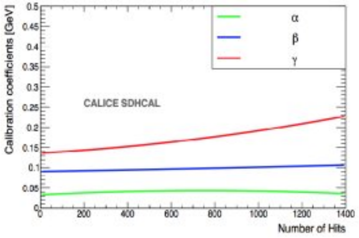
- Uniformity: efficiency & multiplicity
- Threshold optimisations (typ. 1/2 mips, ~5, ~15 mips)
  - and calibration by scans
- Energy measurement:
  - Linearity & Resolution to single e, π, p
  - Simulation: **complex digitization**
    - Large number of overlapping effects in avalanches / readout / time
    - Now, reasonable ≤ 40 GeV e, π

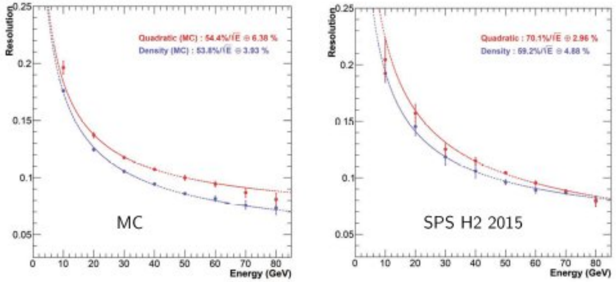


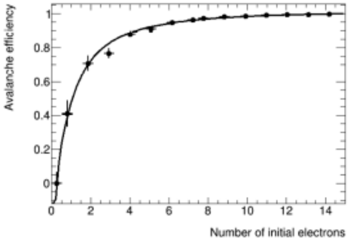


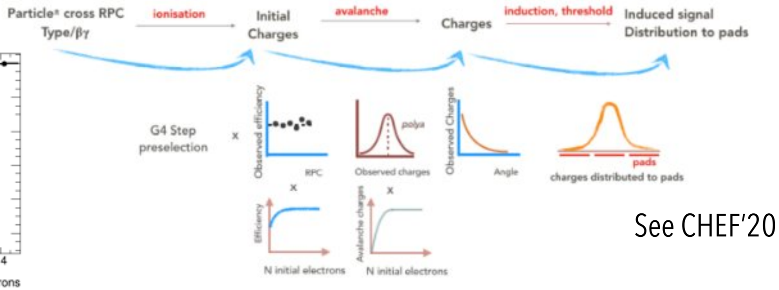
$E_{Dens} = \alpha\, B1 + \beta\, B2 + \gamma\, B3$; B_i = Neighbours ≥ thr. i

$E_{Quad} = \alpha(N_{tot})\, N_1 + \beta(N_{tot})\, N_2 + \gamma(N_{tot})\, N_3$









See CHEF'2019 for details

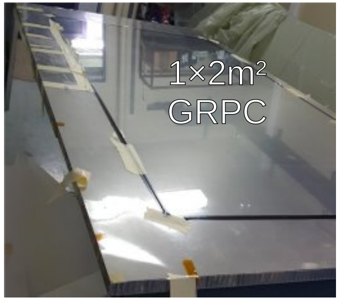
SDHCAL developments

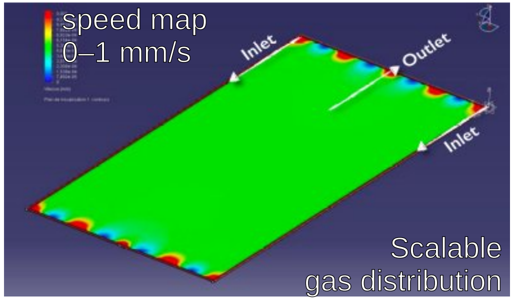
Large cassettes: 1×1 m² → 3×1 m²:

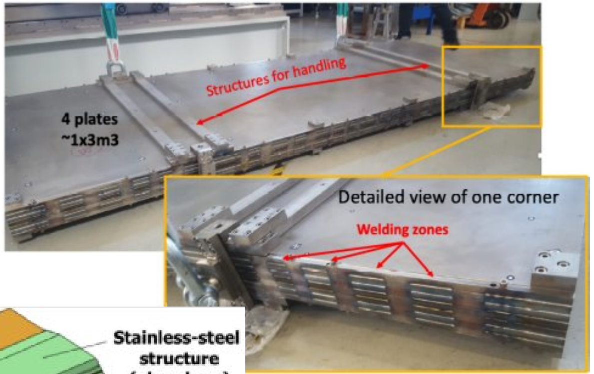
- 432 ASICs HardRoc3:
  I2C, full zero-suppression,
  dynamic range ×3 (15 → 50pC)

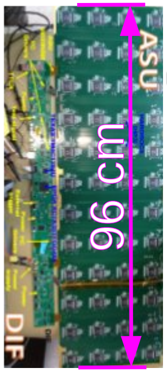
Main goals:

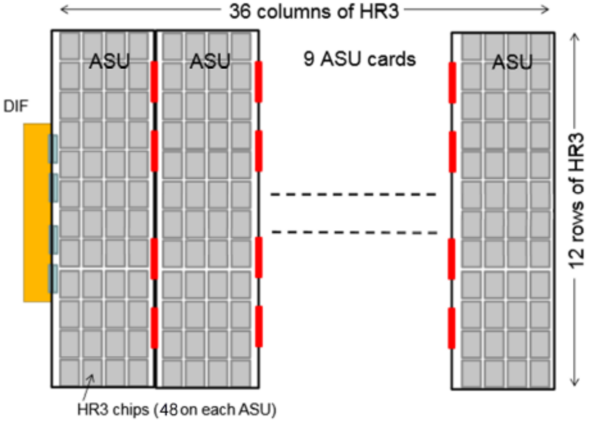
- Sensors: Large uniform GRPC's
- Large & flat PCBs: 32×96 cm²
  - glued on single GRPC chamber
  - interconnections (in 3T field)
- Mechanical assembly
  - Electron
    Beam
    Welding

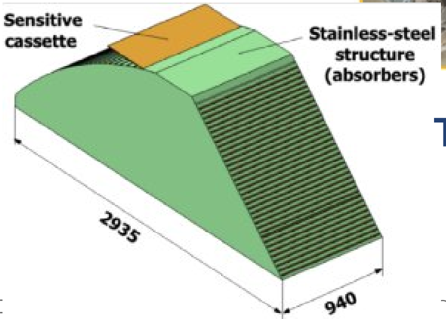












Timing:

Ωmega PETIROC ASIC (20 ps) jitter ⊕ Multi-gap GRPC (60 ps)

Take Home

New version of full technological prototypes getting ready for large BT campaign

⇒ Large knowledge base from previous prototypes & campaigns

within ILC timeline (≤ 5 years of R&D)

Wealth of information, partly explored:

- Digital calorimetry
- in-shower software compensations
- new particle ID variables
- Timing in Calorimeters

Ideal ground for new analysis techniques (Multivariate Analyse, AI)

Many "small scale" R&D

⇒ Model of needed precision (Mechanics, Physics)

CALICE: 15 years of R&D

- have allowed some projects to get a boost
  - CMS HGCAL, Atlas HGTD
- Collaborative approach to realise and compare various ideas & solutions
  - Sharing of information & expertise
    - BT knowledge, DAQ, Simulation & Analysis Tools, …
  - Started as ILC (as in ca**ILC**e)
    - no more directly experiment related
      Higgs factories, and beyond (FOCAL, CMS-HGCAL)
    - New Topics: timing in calorimeters, Dual Readout, ...
      - Session @ Collab meeting for Outreach.

Vibrant and open community...

Extras

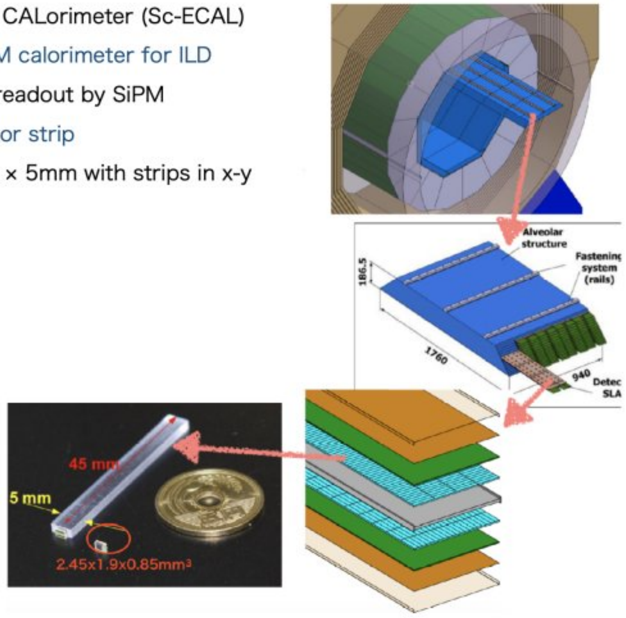
Scint-ECAL tile wrapping

Reflector wrapping (90mm strip)

- Wrapping by hand with a help of jig

Sc-ECAL (reminder)

- Scintillator Electromagnetic CALorimeter (Sc-ECAL)
  - Technology option of EM calorimeter for ILD
- Based on scintillator strips readout by SiPM
  - 5 × 45 × 2 mm scintillator strip
- Virtual segmentation : 5mm × 5mm with strips in x-y configuration
- Timing resolution < 1 ns
- Low cost

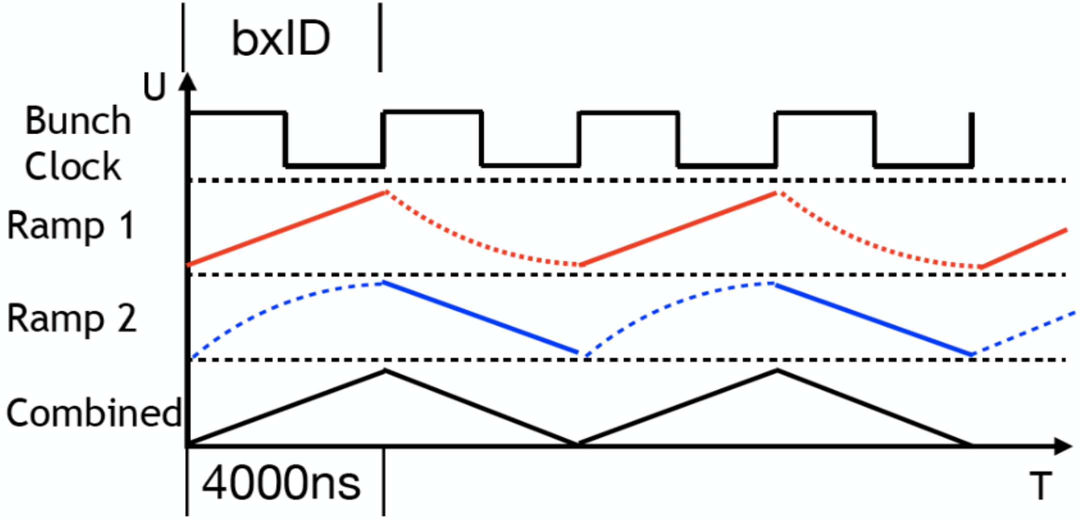


Time calibration (HW)

Time measurement with Spiroc2E: TDC (time to digital converter)

1. Common external clock with ~1ns bins

2. Ramp up voltage during one bunch crossing ID

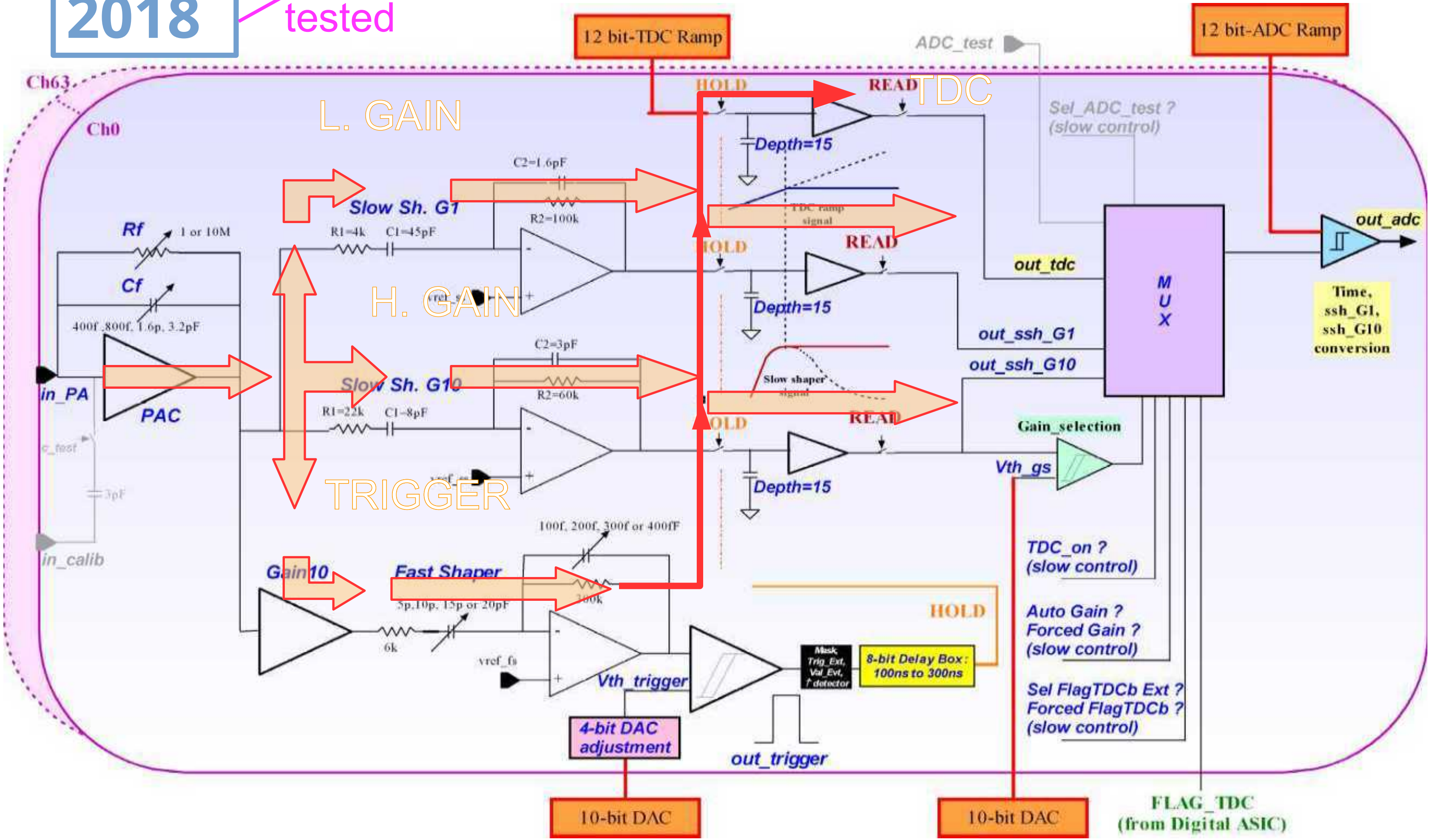


Lorenz Emberger (MPI. Munich)

SKIROC2 / 2A Analogue core

2018

tested



Similar to SiD Kpix

- 64 channels
- Preamp
  + 2 (auto)Gains
  + TDC (~1.4ns)
- Auto-triggered
  - **per cell adj.**
- 15 (×2) analogue memories
- Low consumption
  - 25 μW/ch with 0.5% ILC-like duty cycle
- Power-pulsed

Not final chip
(full 0-suppr.)