# A. R. C. A. D. I. A.

## Advanced Readout CMOS Architecture Depleted Integrated Array

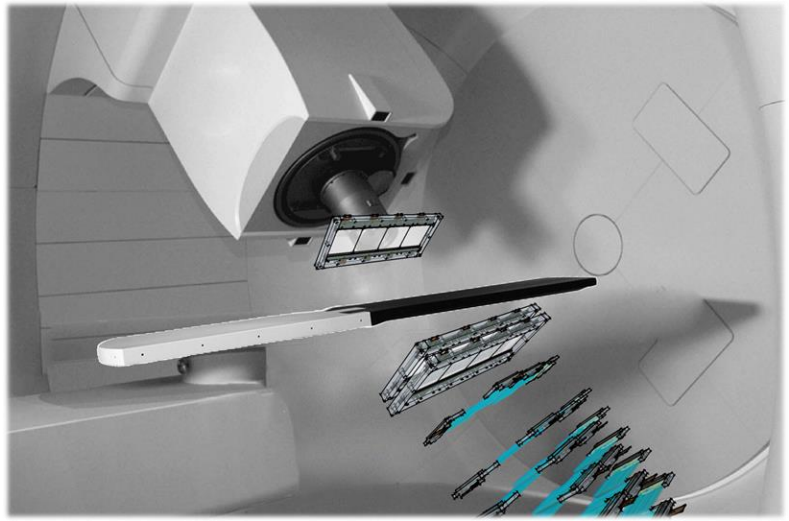
F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, T. Corradino, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, L. De Cilladi, B. Di Ruzza, A. Di Salvo, D. Falchieri, M. Favaro, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi

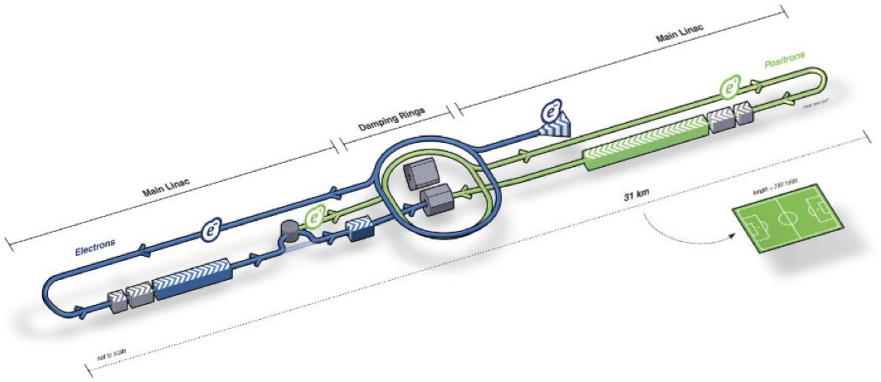
INFN

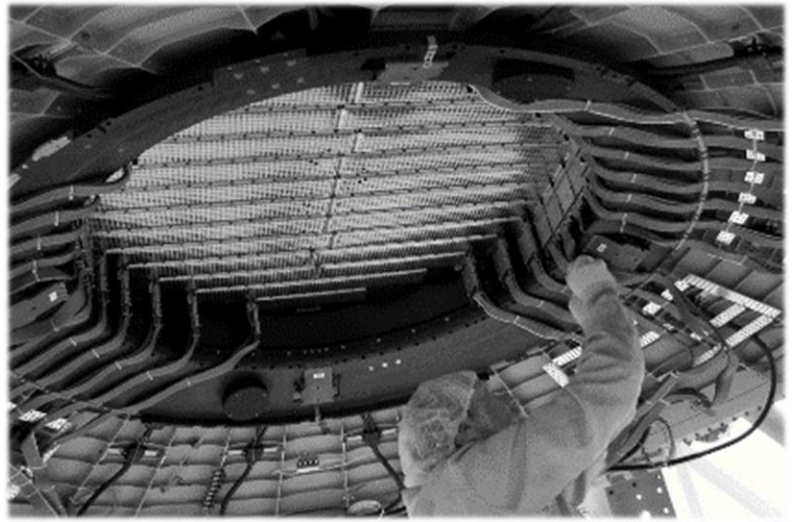
P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, S. Mattiazzo, C. Neubüser, F. Nozzoli, J. Olave, L. Pancheri, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, H. Roghieh, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, M. Zarghami, P. Zuccon

# Overview and goals

- The ARCADIA project aims to develop a **design and fabrication platform** for large-area CMOS sensor
- Target applications: space, medical and detectors at lepton colliders.
- Use a proven sensor (SEED) with good radiation tolerance and full depletion.
- Require a designed characterized by a scalable architecture over large area.





## Medical

- Low power (≤ 40 mW/cm$^2$)
- Medium rate ≈ 10 MHz – 100 MHz/cm$^2$
- Ultra low material budget (low energy)
- Very large area (≥ 16 cm$^2$)
- 3-side buttable
- Low to medium rad-tolerance ≈ 10 kGy

## Lepton collider

- Low power (≤ 40 mW/cm$^2$)
- Medium rate ≈ 10 MHz – 100 MHz / cm$^2$
- Very low material budget
- Large area (≥ 6 cm$^2$)
- 3-side buttable
- Low to medium rad-tolerance ≈ 10 kGy

## Space

- Ultra low power (≤ 10 mW/cm$^2$)
- Very low rate ≈ kHz/cm$^2$
- Low material budget
- Large area (≥ 6 cm$^2$)
- 3-side buttable
- Low rad-tolerance ≈ 1 kGy

# Target specifications

| | Min | Max | Note |
|---|---|---|---|
| Power consumption | 10 mW/cm$^2$ | 20 mW/cm$^2$ | |
| Pixel pitch | - | 25 µm | In demonstrator the largest dictated by CCE |
| Matrix area | 4 cm$^2$ | 24 cm$^2$ | 1 cm$^2$ in the first demonstrator |
| Hit Rate | 10 MHz/cm$^2$ | 100 MHz/cm$^2$ | Assuming 4 px/hit |
| Timing resolution | O (1 µs) | O (10 µs) | For first demonstrator |
| Radiation hardness | - | 5 kGy | Clearance required if > 5 kGy (lepton collider) |

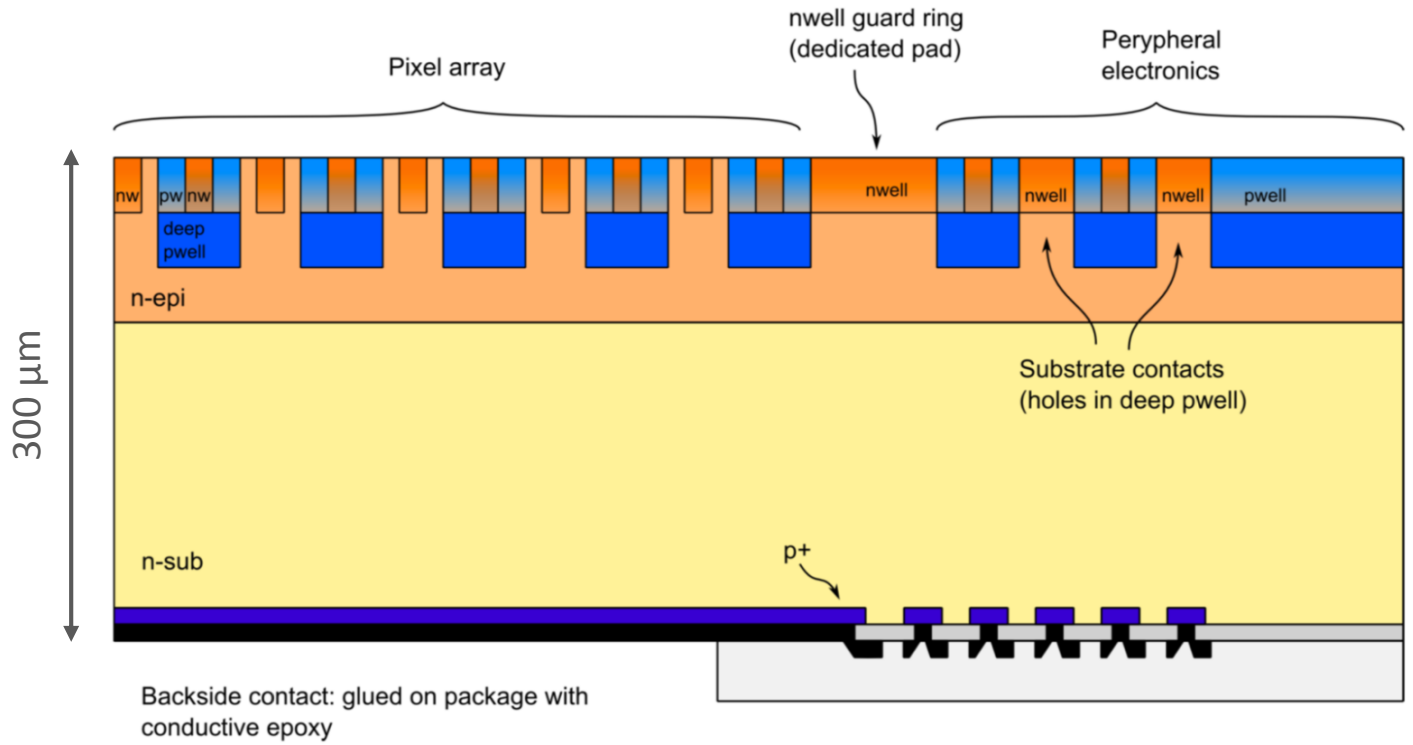
## Main features

- Clockless matrix (to minimize power dissipation)
- Trigger-less readout
- Binary readout (with pixel masking)
- Easy replicable, identical sections (512 × 32 px each in the demonstrator)
  - Scalable architecture able to cope with 2048 pixel high sections
  - One output link per section (with power-off and bypass for space-mode operations)
- Ultra low power "space" mode, using only one high speed output for all the sections.

# Fully depleted sensor

The ARCADIA design uses a sensor solution (SEED) developed in collaboration with LFoundry to achieve uniform, full depletion over thicknesses of few hundreds microns by virtue of a patterned backside (4 mask process).

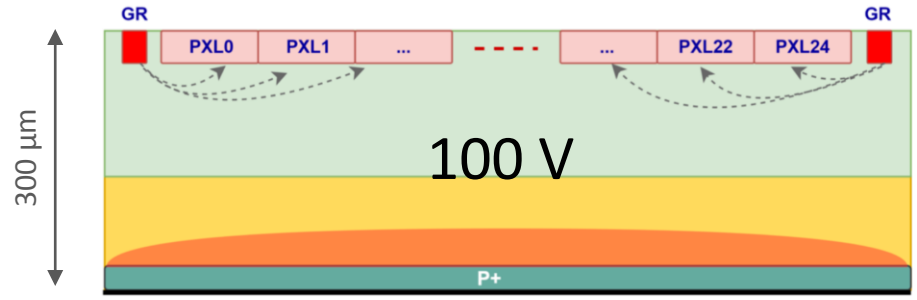
- Technology: 110 nm CMOS CIS technology, high-resistivity bulk
- Full depletion with fast charge collection
- Both NMOS and PMOS transistors, 6 metal layers
- Custom patterned backside (patented) with LFoundry
- 50 µm to 500 µm sensor thickness (more if necessary)

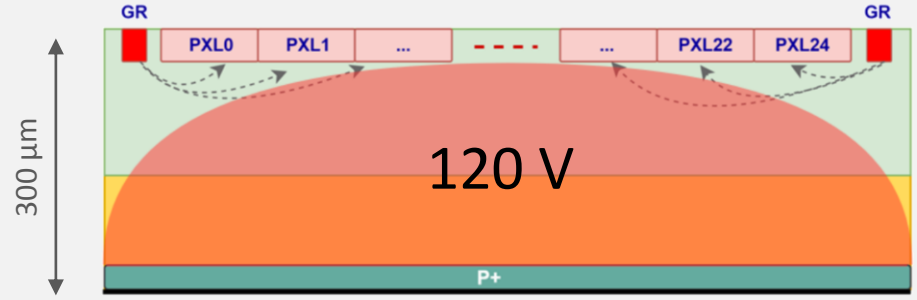


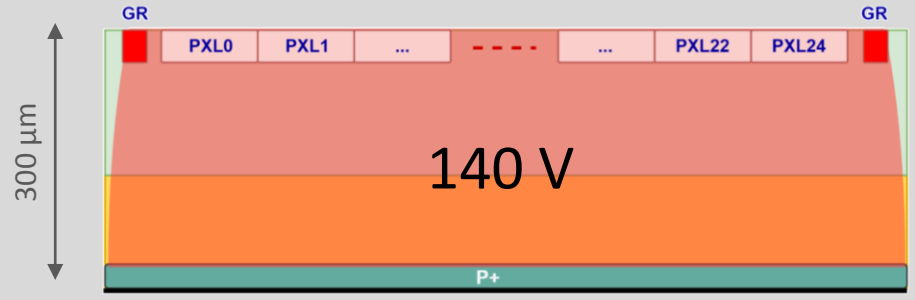

A "thin" 100 µm thickness version has been also successfully produced and tested

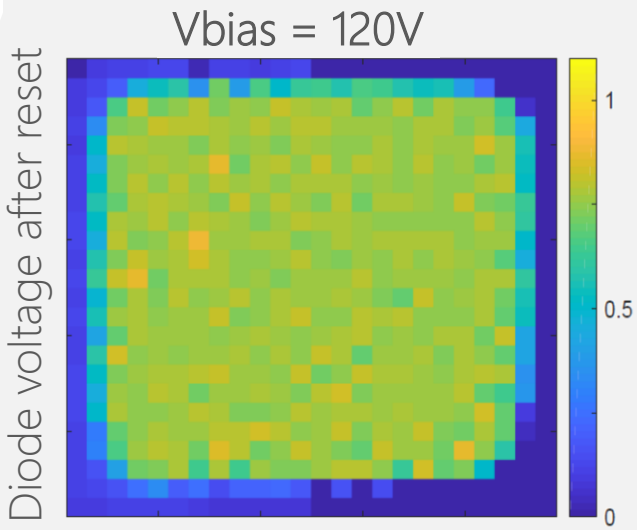
# Full depletion achieved on 300 µm thick sensor

The sensor becomes fully depleted, with uniform field below the pixel wells, for voltages above 140 V for a 300 µm thick detector. The same happens at lower voltages (60 V) for a thinner version of 100 µm thickness.

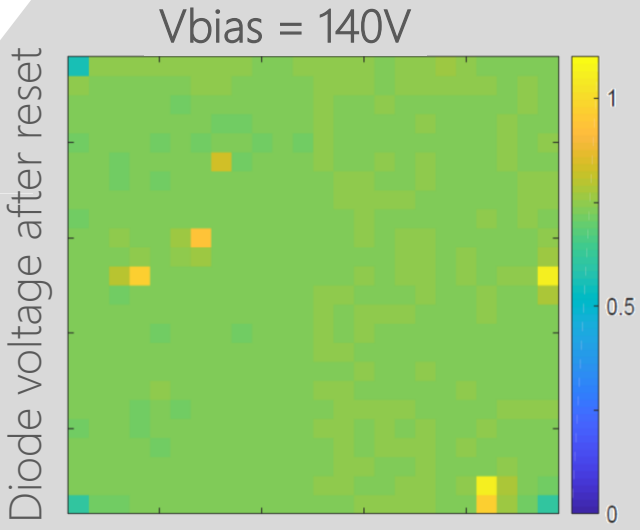



Not yet fully depleted at the sensor periphery, where the diodes remains connected to ground (reset voltage ≈0V at the borders)

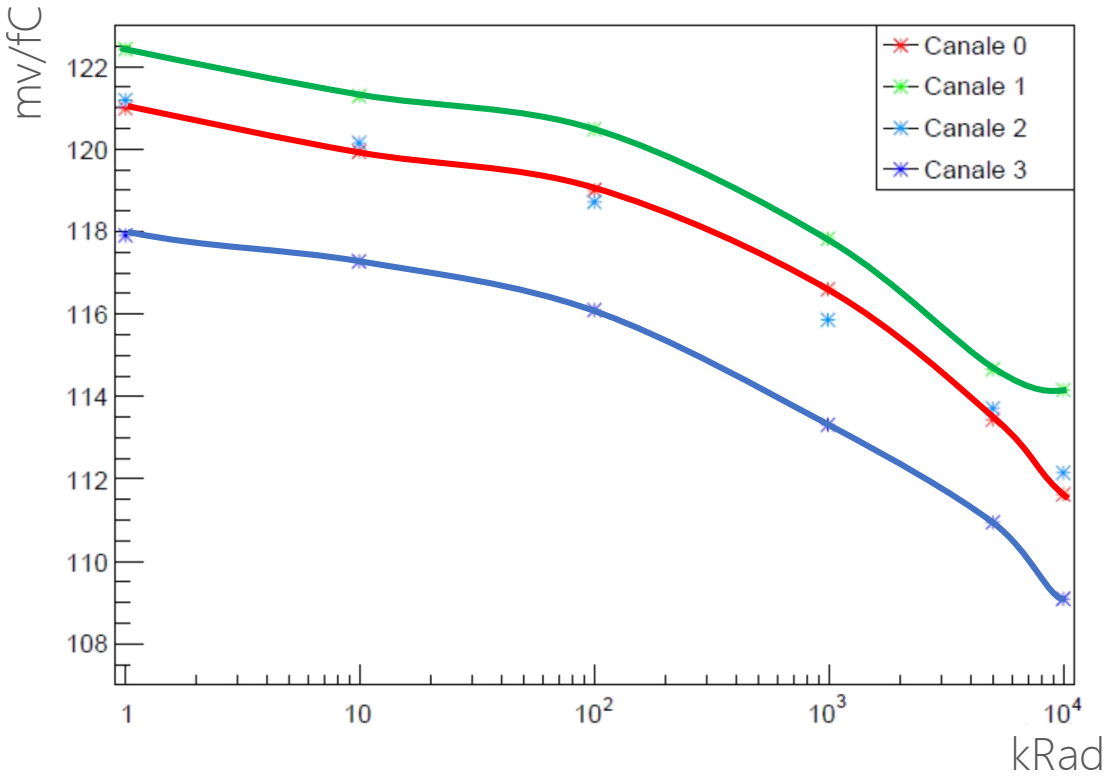



Uniform full depletion achieved across the device, even border diodes are insulated from ground (uniform voltage after reset ≈0.6V)

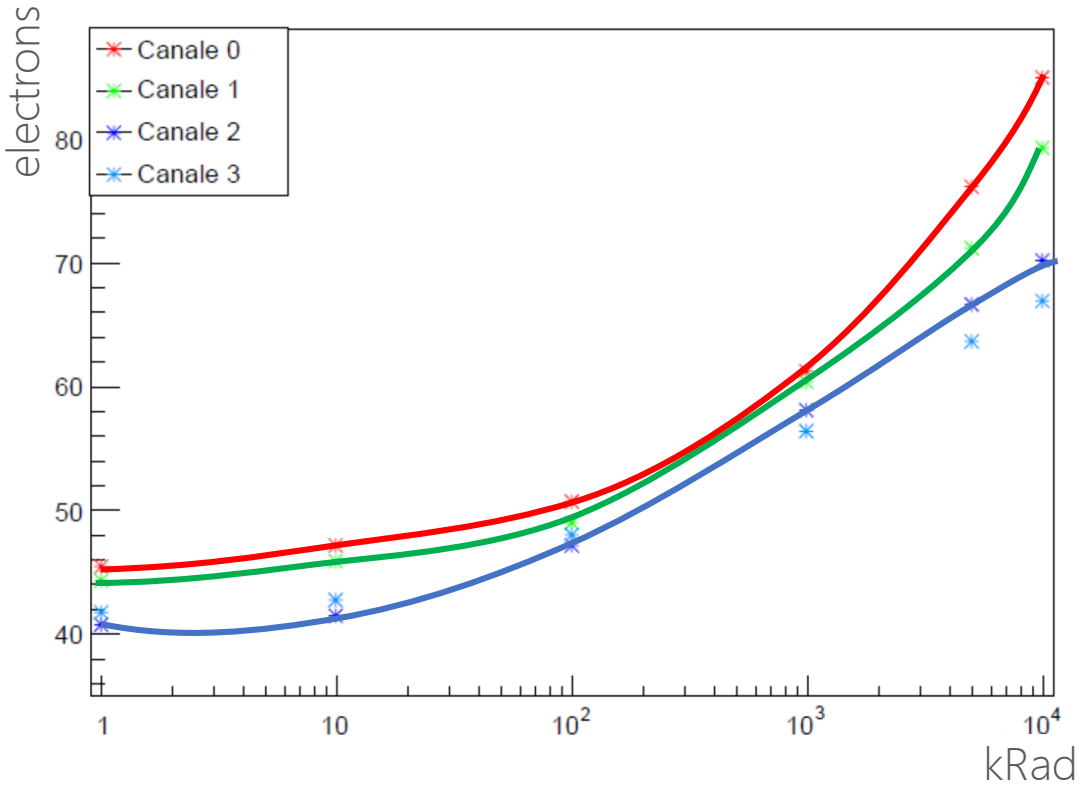
# Sensor radiation hardness

The sensor behaves well respect to ionizing radiation. Initial measurements for TID done using x-rays (Seifert machine) show how the gain (calibrated with $^{55}Fe$ source) is only slightly affected up to about 1 kGray (100 kRad).

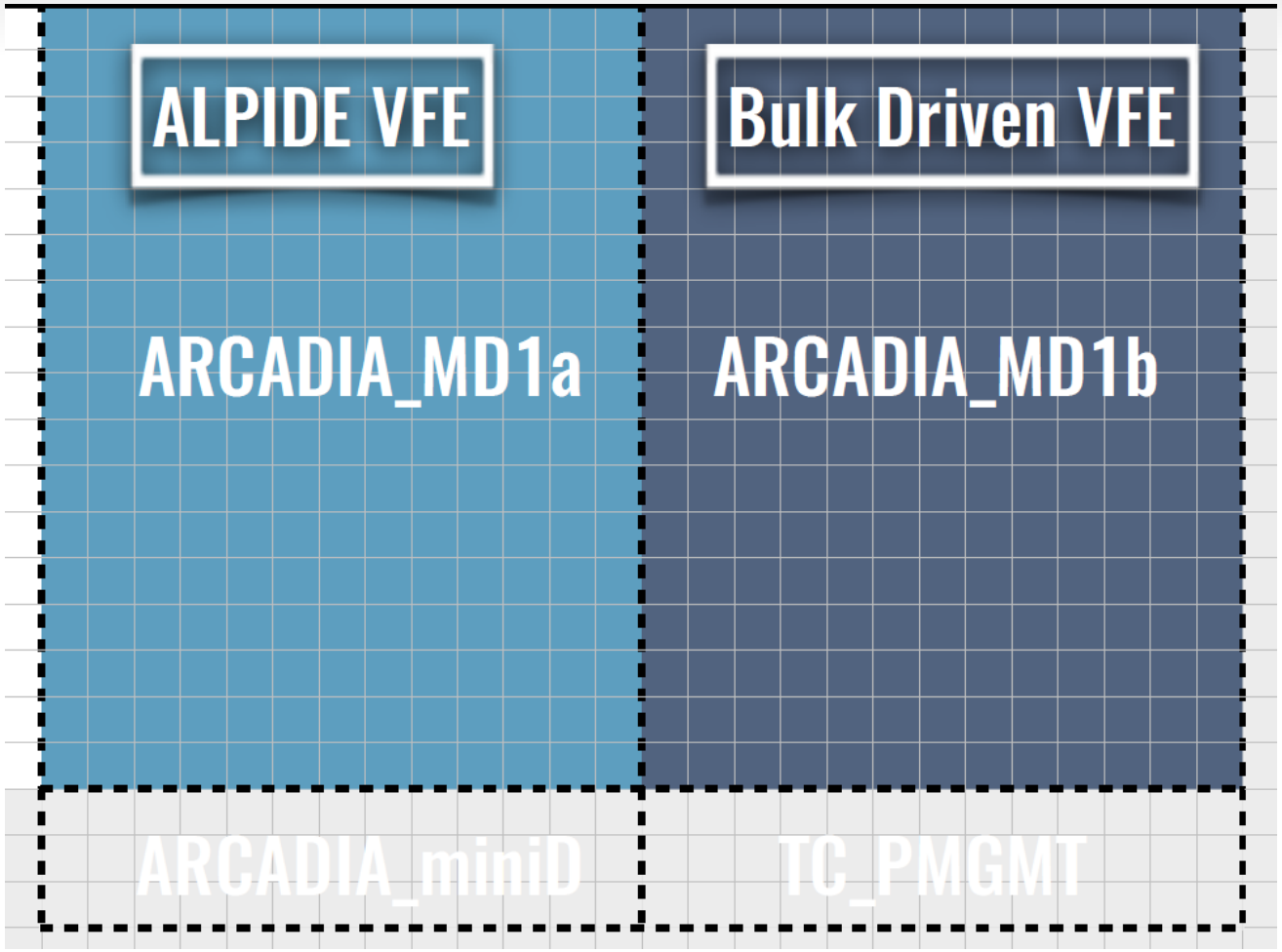
## Gain vs total dose




## Noise vs total dose



# Demonstrator production engineering run (September 2020)



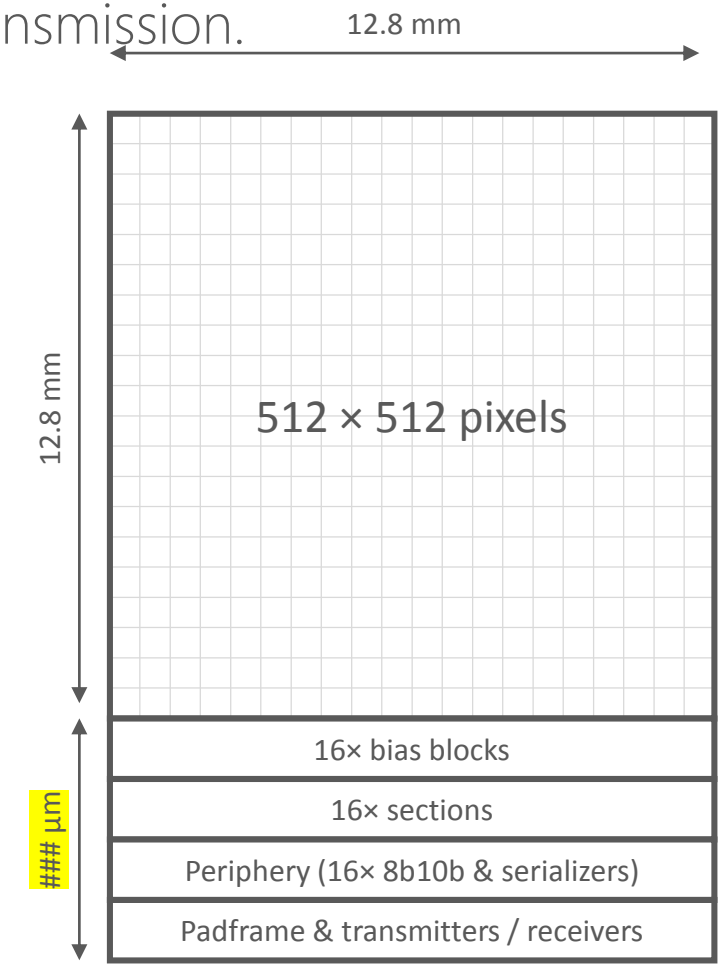

Various test structures:

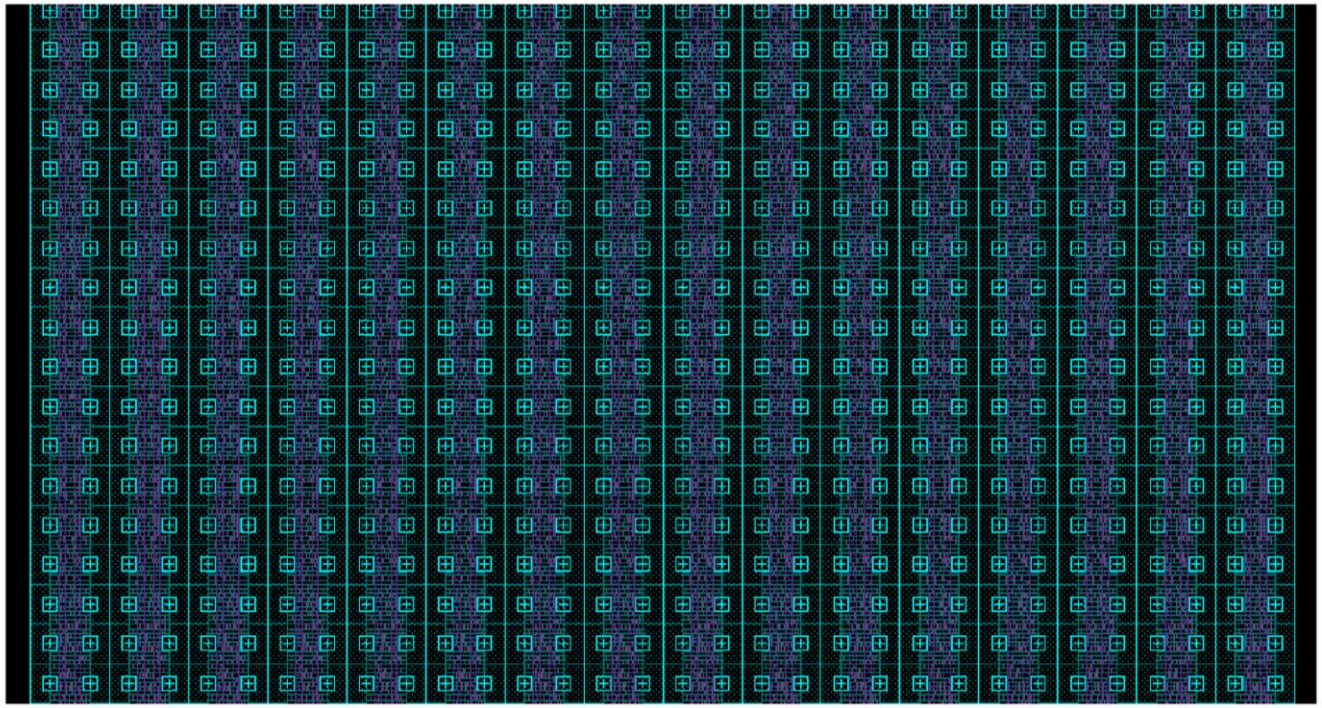
- Smaller matrices
- Sensor design modifications
- Macro-pixels (strips of 25 µm and 50 µm)

Two main matrices of 512 × 512 pixels, implementing two different front-end topologies (see next slides)

# Matrix demonstrator characteristics

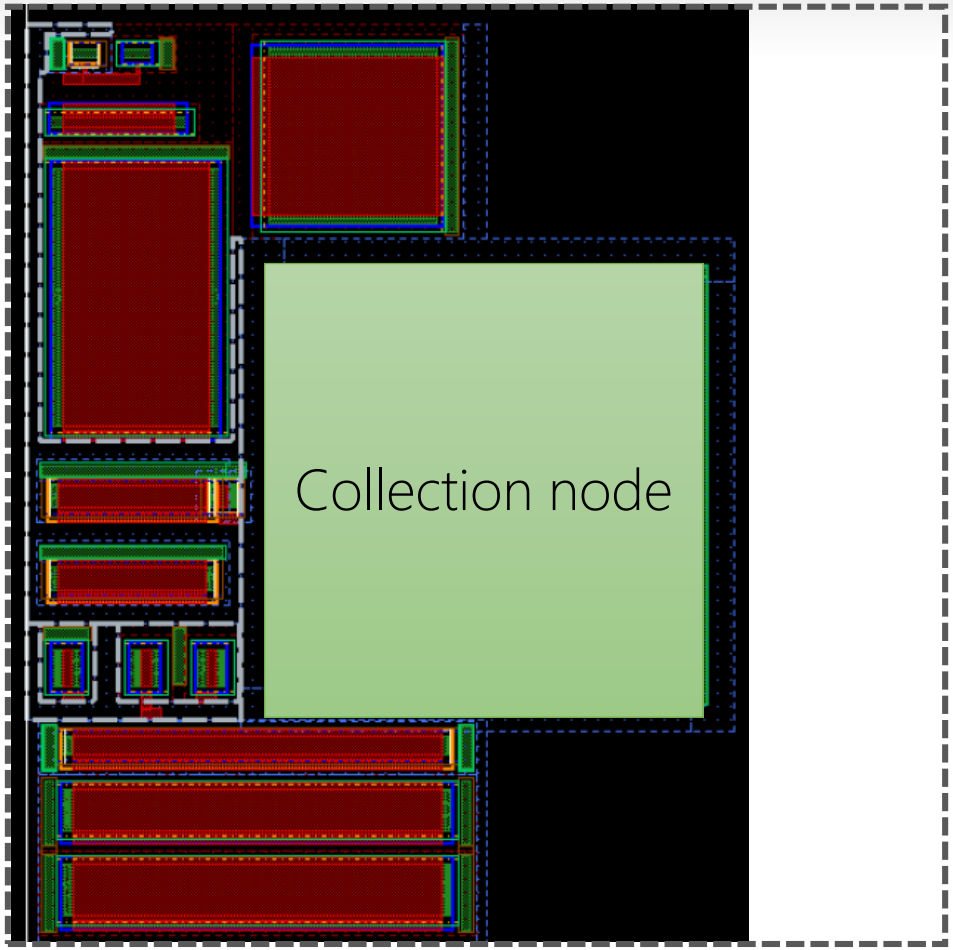
The first prototype embeds two 512 × 512 pixel matrices (different front-ends), divided into 16 identical sections. Each section has a dedicated bias and readout blocks, plus a I/O stage for 320 Mb/s data transmission.



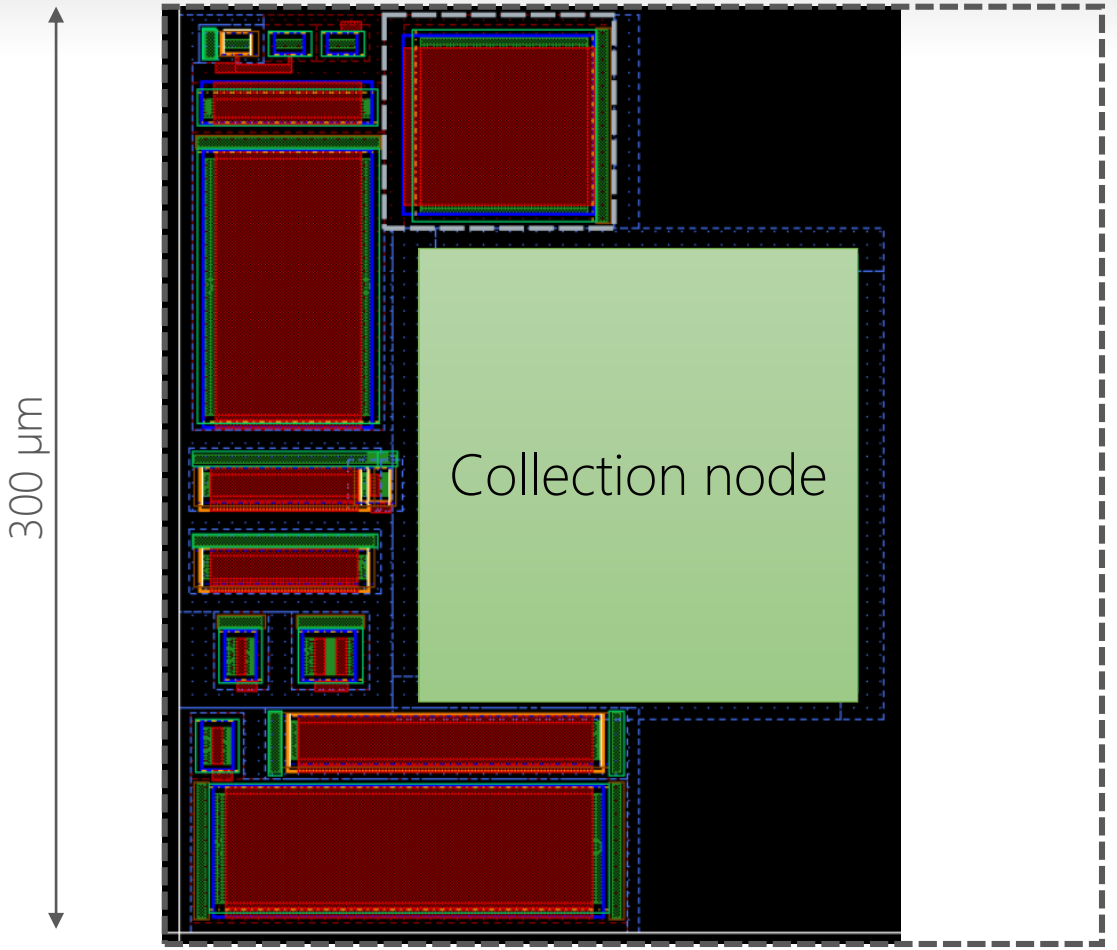



- Pixel size: 25 µm x 25 µm
- Matrix core 512 x 512, side-buttable.
- Matrix, EoC architecture, data links scalable to 2048 x 2048
- Trigger-less binary data readout, up to 10-100 MHz/cm$^2$

# ALPIDE-like and Bulk-Driven front ends




ALPIDE-like front-end

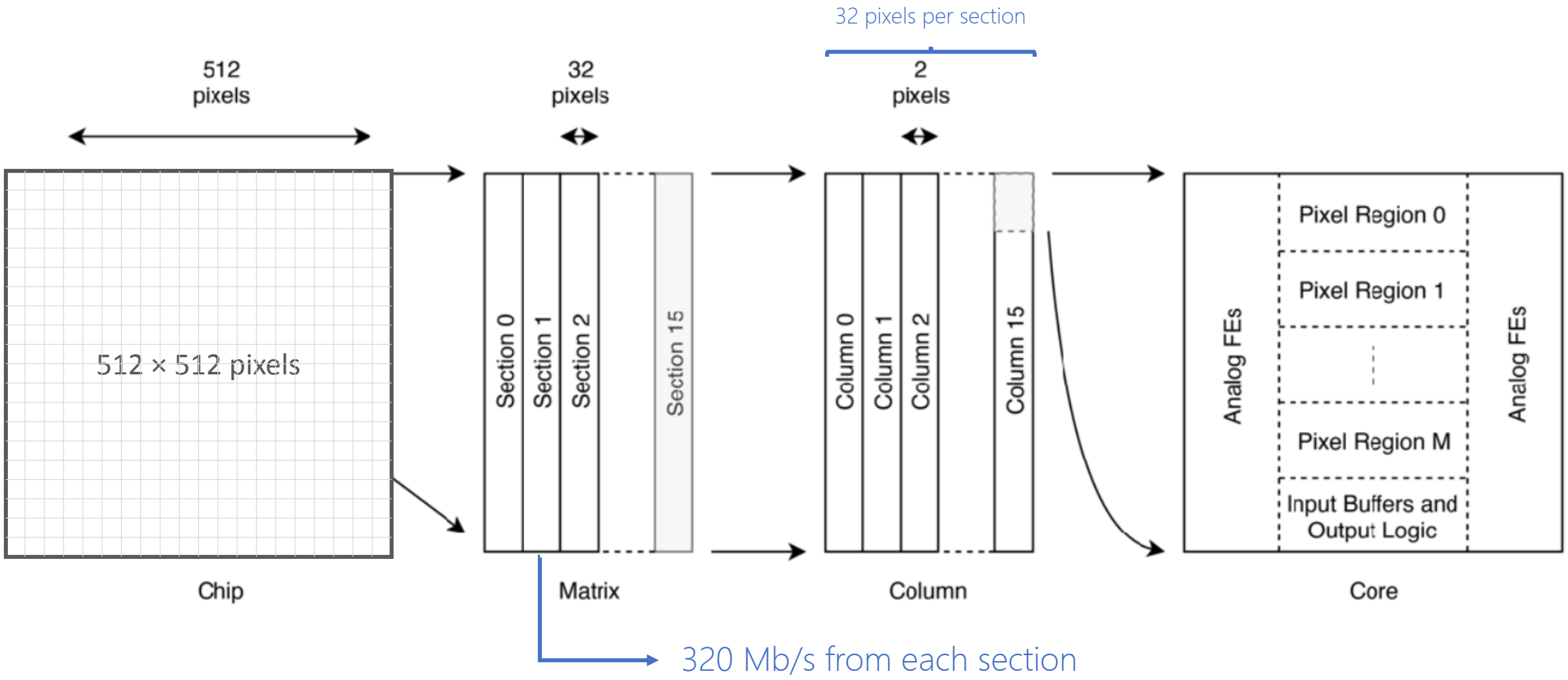



Bulk-driven front-end

- Pixel area: 25 x 25 µm$^2$
- Diode area: 9 x 9 µm$^2$
- Analog circuits area: 223 µm$^2$

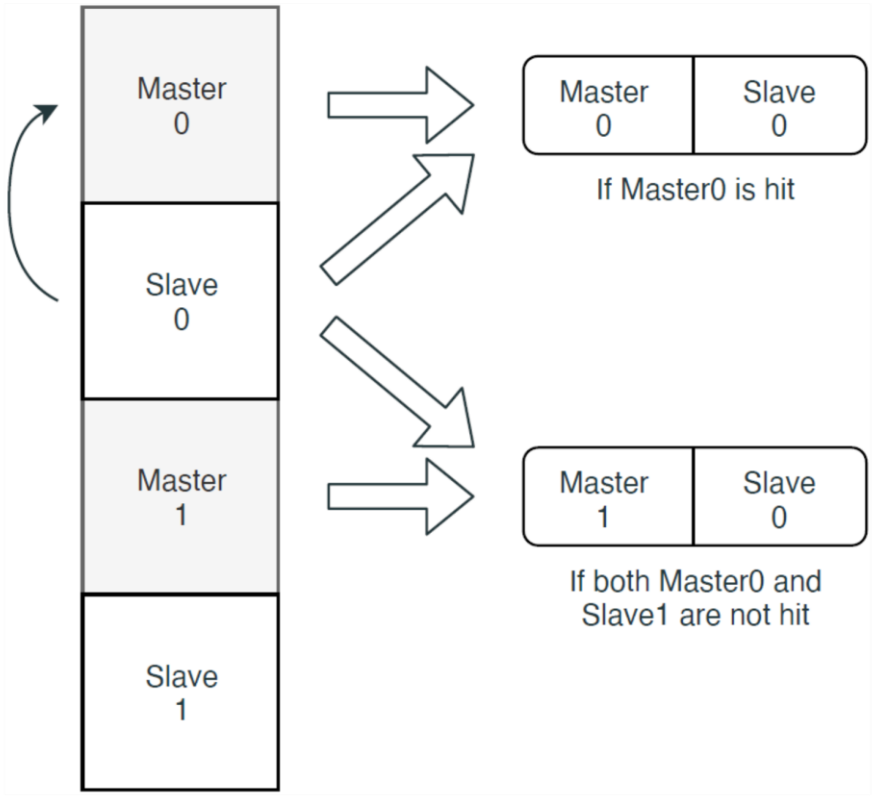
# Architecture: custom modular readout

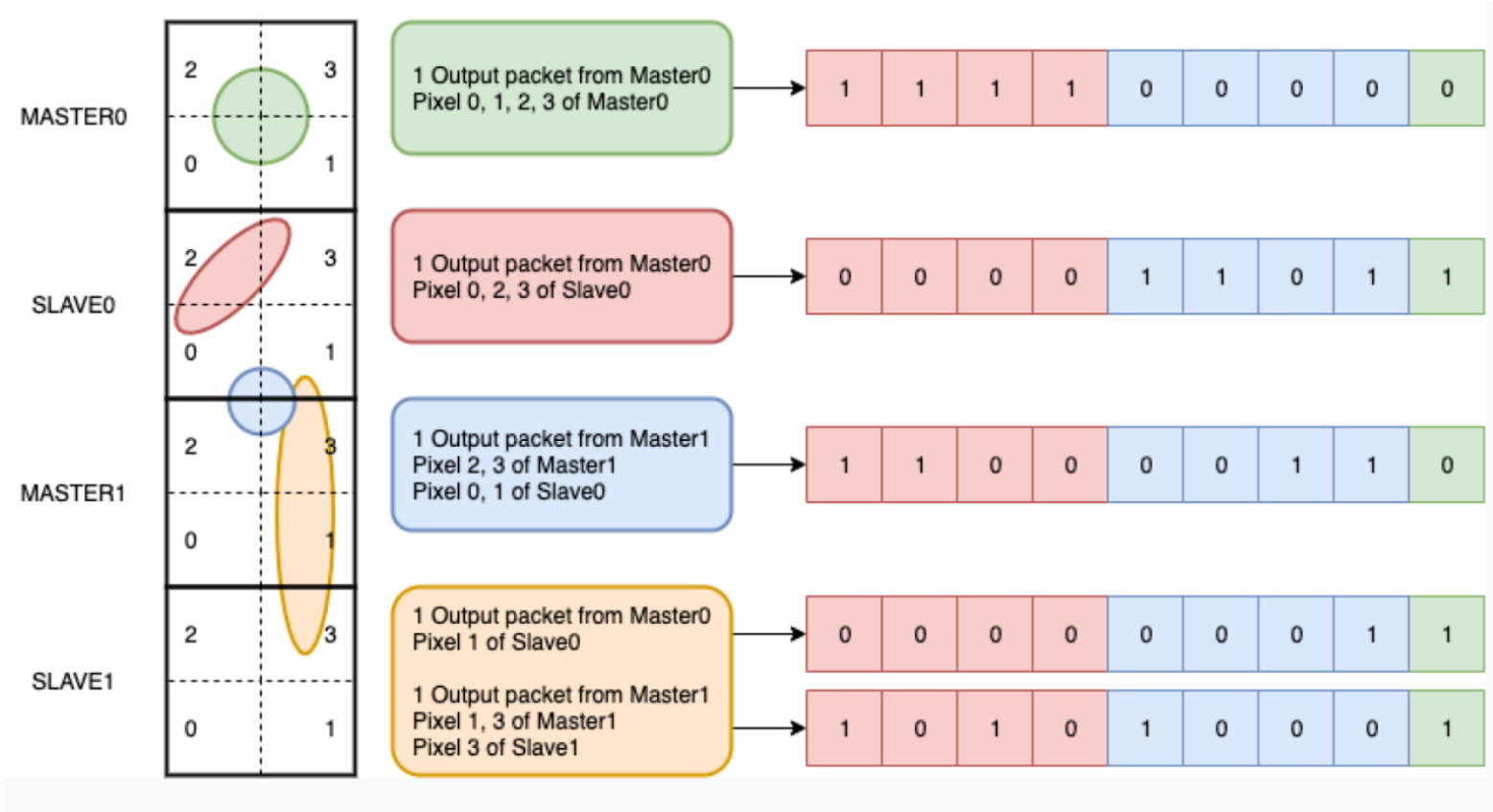
The first prototype embeds a 512 × 512 pixel matrix, divided into 16 identical sections. Each section has a dedicated bias and readout blocks, plus a I/O stage for 320 Mb/s data transmission.



# Architecture: clusterizing within the matrix

Within a double column the pixels are organized into “cores”, to optimize the readout of multiple pixels clusters. The readout is tokenized, with the clock running only on the periphery.



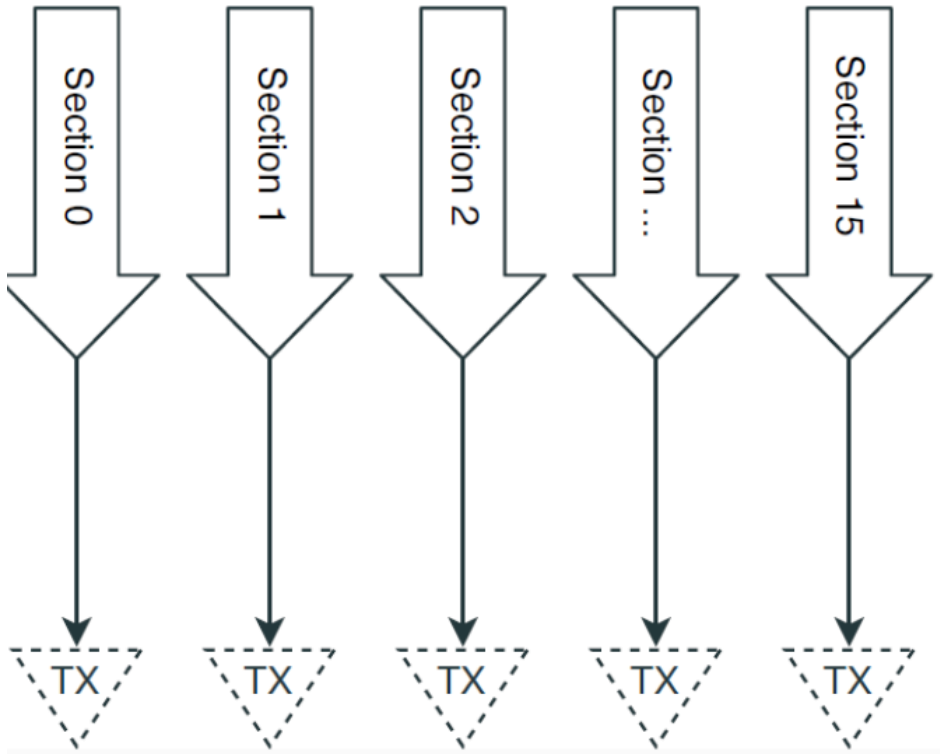




2 × 4 pixel Regions, divided into Master (2 x 2) and Slave (2 x 2)

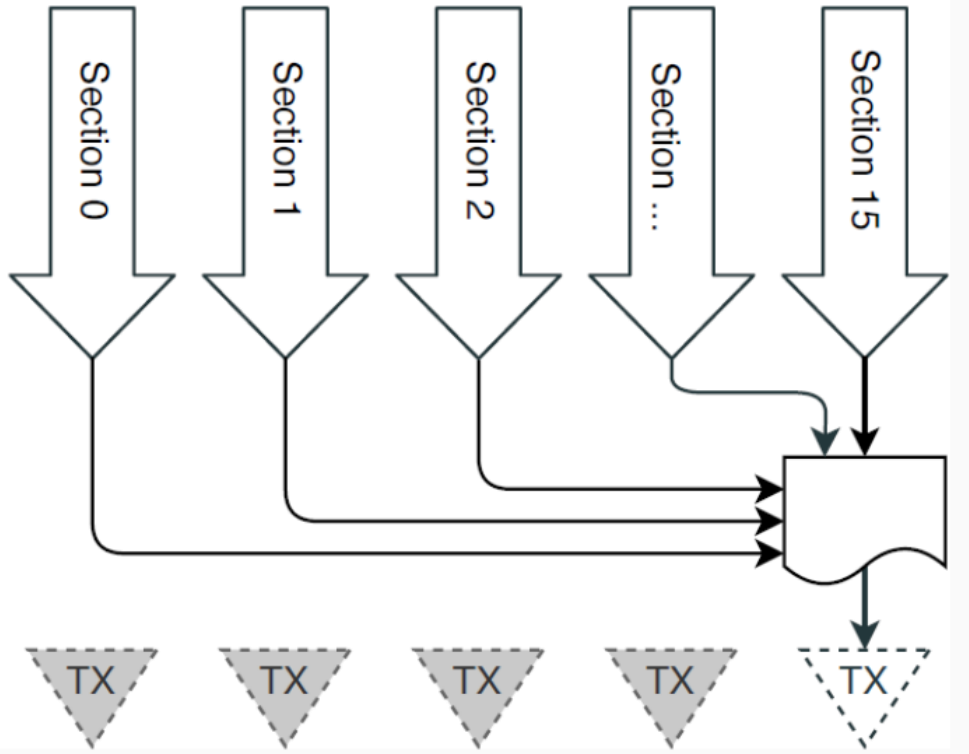
- Slaves (w/o readout) choose a Master: its own (top), or the preceding one (bottom)
- Masters propagate 2×4 pixel data packet to periphery, then await the Acknowledge pulse
- Significant reduction of column occupancy and readout clock

# Architecture: outputs

## High-rate mode




## Slow-rate (space) mode



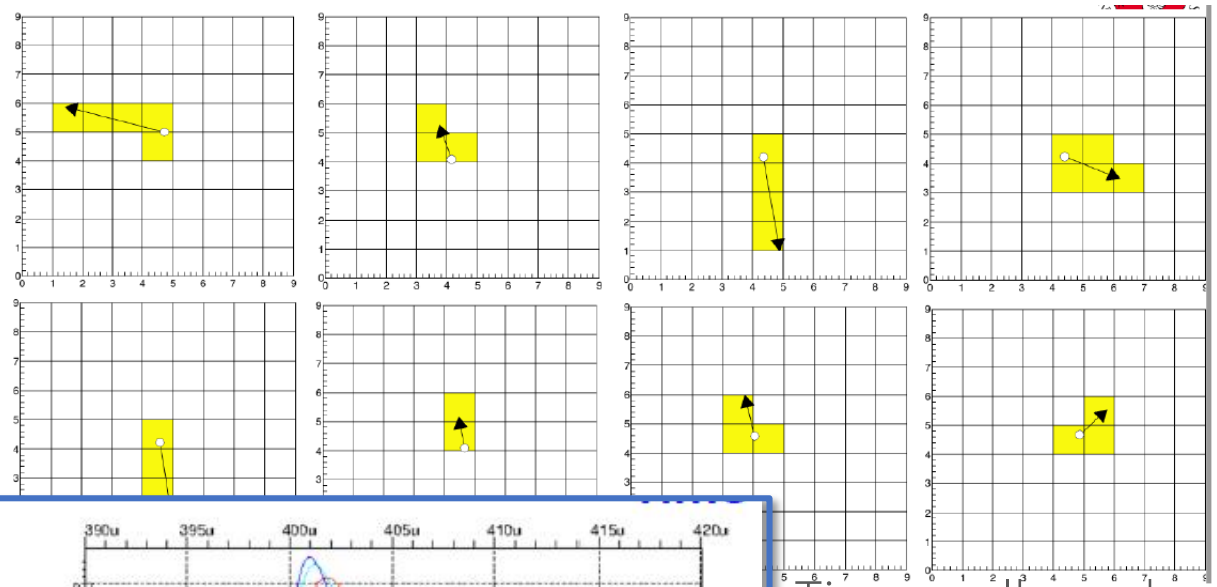

The Section Output Unit comprises:
- a 320MHz DDR Serializer
- an 8b10b encoder
- an SLVS Transmitter

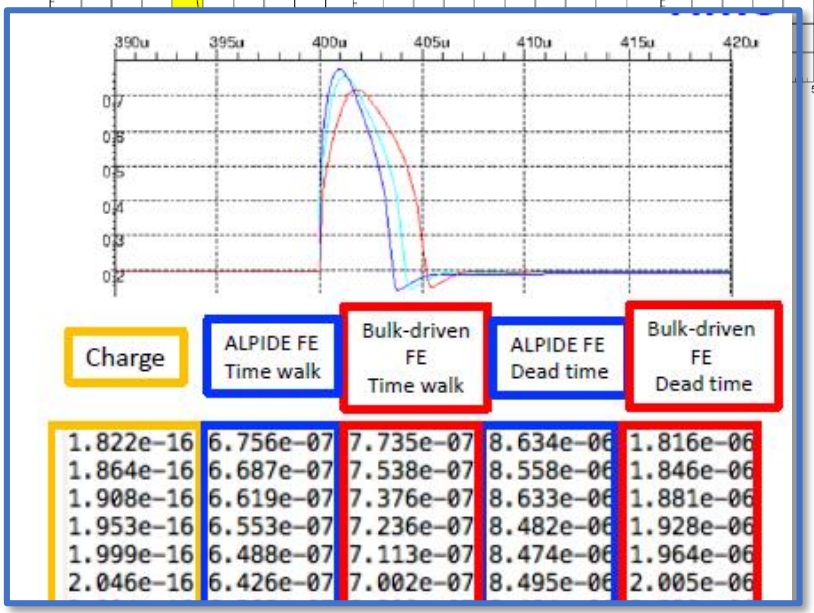
The SOU keeps constant data flow.
Packets are 40-bits long, with 8/10 encoding

- At 320MHz DDR, SOU sends a packet every 62.5ns
- SOU can read data from the SRUs at 16MHz
- If the SRU FIFO is empty, the SOU sends a synchronization packet

# Architecture: verification and performance simulation

Extensive simulation using database-retrieved and/or monte-carlo simulated clusters reflecting different particle types and sensor thicknesses, with spatial and time distribution defined by application-specific file representing the expected particle flux (in space and time) for that scenario.






Time-walk vs charge look up tables from back-annotated simulations to realistically simulate the time evolution of each cluster pixel

## 10 MHz / cm$^2$ uniform (Poissonian in time)

```
Final Summary:
    Matched hits:                    395008/    395199 (99.952% of sent)
    Timing displaced hits:           292594/    395199 (74.037% of sent)
    Deadtime (not injected) hits:       190/    395199 ( 0.048% of sent)
    Ghost hits:                           0/    395009 ( 0.000% of recv)
    Duplicate hits:                       0/    395009 ( 0.000% of recv)

    Missing hits:                         0
```

## 100 MHz / cm$^2$ uniform (Poissonian in time)

```
Final Summary:
    Matched hits:                    393007/    395245 (99.434% of sent)
    Timing displaced hits:           287460/    395245 (72.730% of sent)
    Deadtime (not injected) hits:      2229/    395245 ( 0.564% of sent)
    Ghost hits:                           0/    393008 ( 0.000% of recv)
    Duplicate hits:                       0/    393008 ( 0.000% of recv)

    Missing hits:                         8
```

# Conclusions

## Sensor

- Proven, patented fully-depleted sensor solution (SEED)
- Thickness available in the 100 µm – 500 µm range.
- Radiation tolerant to 5 Gy (500 kRad) TID with minimal degradation, up to 100 Gy with 2× noise.
- Testing with reactor neutrons (MeV range) ongoing.

## Front-end

- Two front-end solutions, ALPIDE-like and Bulk-Driven.
- Similar performances, better timing with Bulk-Driven, but with added jitter and noise
- Decision will come only after prototypes testing.

## Architecture

- Low-power, clock-less matrix targeting ≤ 20 mW/cm$^2$ dissipation and 100 MHz/cm$^2$ hit rate.
- Scalable: up to large area sensor with 2048 pixels/column: 5 cm tall column with 25 µm pitch.
- Partial clustering and compression embedded into the readout itself to further save power.
- Low power mode for space applications, with only one active high-speed output.

## Next

- Improved, more efficient architecture to be tested in the second prototype (spring 2021).
- Protection against SEUs (primary protons and ions, secondary fast neutrons) (spring 2021)
- Testing stitching toward the realization of larger-than-reticle sensors (end 2021).

# Backup