Development and Evaluation of Prototypes for the ATLAS ITk Pixel Detector

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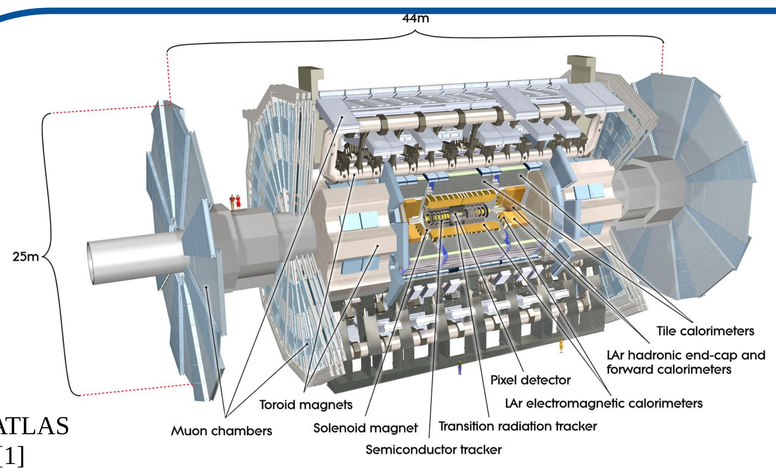
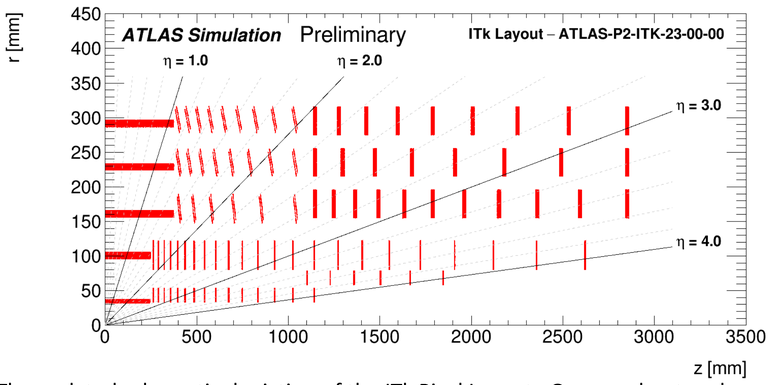
UNIVERSITÄT BONN

BMBF-ErUM-Forschungsschwerpunkt ATLAS-EXPERIMENT
Ausbau von ATLAS am LHC: Physik mit dem ATLAS-Experiment
ErUM-FSP T02

ATLAS Phase-II Upgrade



Current ATLAS detector [1]



The updated schematic depiction of the ITk Pixel Layout. One quadrant and only active detector elements are shown. The horizontal axis is along the beam line with zero being the interaction point. The vertical axis is the radius measured from the interaction region. [2]

High Luminosity Large Hadron Collider (HL-LHC)

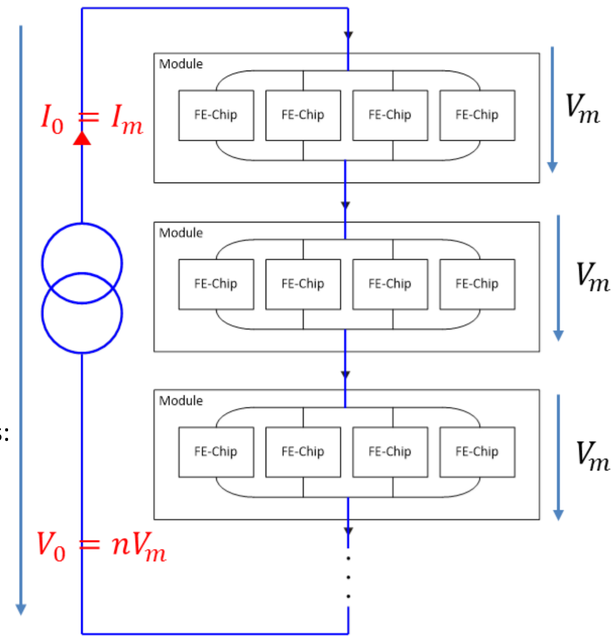
- Instantaneous luminosity increases by factor of 5 – 7.5
- Requires detectors with better radiation tolerance and higher data rate capabilities
- New pixel detector as part of an all silicon tracker (ITk)

New ATLAS pixel detector

- 5 layers of pixellated sensors extending over 6m in z and 70 cm in R
- Increased surface from 2m² to ~15 m²
- Hybrid pixel detectors with 3D and planar sensors and different modules:
  - Quad modules: 4 readout chips bump-bonded to single large sensor
  - Pseudo triplets: 3 single-chip modules connected to same flex PCB
- Pixel size: 50 x 50 µm² & 25 x 100 µm²
- See also Stefano Terzo's talk on Tuesday

Serial Powering Scheme

- Reduce power losses in services and material budget
- Supplied by constant current source to up to 14 modules in series
- On-Chip voltage regulators generate supply voltage
- New powering scheme, requires extensive prototyping

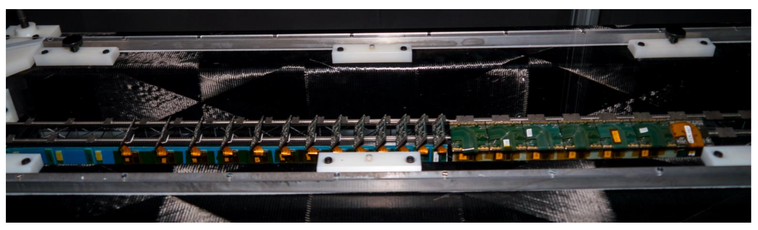


Simplified schematic of the serial powering scheme used to power the ITk pixel detector. Here, each module consists of 4 readout chips connected in parallel, each equipped with Shunt-LDO regulators.

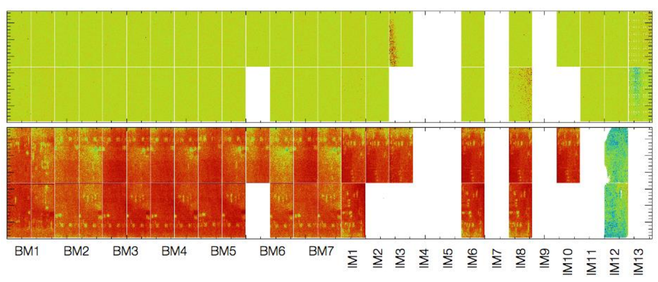
ITk Pixel Prototyping

Prototyping Progress for the Outer Barrel (OB)

- Two fully loaded structures completed: a short electrical prototype with 7 quads and a full cooling line with 28 duals (2 readout chips on common sensor) and 14 quads (FE-I4b based modules)
- Operation of 3 serial powering chains with a common ground revealed no showstoppers: verification of several system aspects like HV distribution and Grounding and Shielding architecture
- Measurements and observations on those prototypes provided input to design of future readout chip and power supplies for overall system compatibility
- Voltage transients by misconfigured modules required design changes for the on-chip voltage regulators



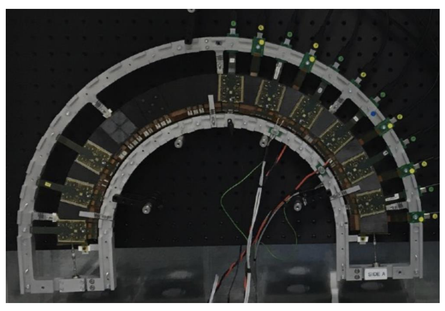
Populated half cooling line during demonstrator integration. This prototype still includes the PSPP chip which will not be present in ITk. [4]



Threshold scans after tuning (top) and scans with a radioactive source (bottom) of all functional chips in this half cooling line. [4]

Endcap (EC) Prototyping

- 2 serial powering chains on half-ring with a total of 12 FE-I4b quad modules
- Verified different assembly methods for quad modules
- Valuable lessons learned for design and integration of endcaps

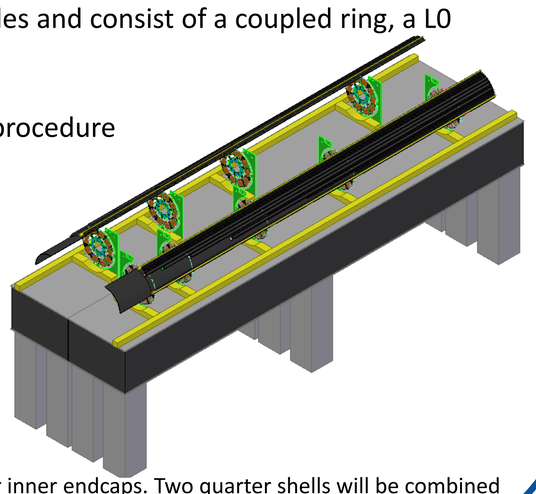


"Ring-0", loaded with 12 FE-I4b quad Modules on an early Type-0 services design. Two serial powering chains with 6 quads each form a fully loaded quadrant. Additional dummy modules have been loaded as well.

Prototyping with RD53A [8] Modules

- Large scale prototypes with RD53A modules being commissioned by ITk pixel subsystems to cover mechanics, electronics and integration
- Example: Inner System (IS)
- Prototype will be loaded with RD53A modules and consist of a coupled ring, a L0 stave and a L1 stave
- Prototype will be used to verify integration procedure

R0/1 Coupled Ring [3]

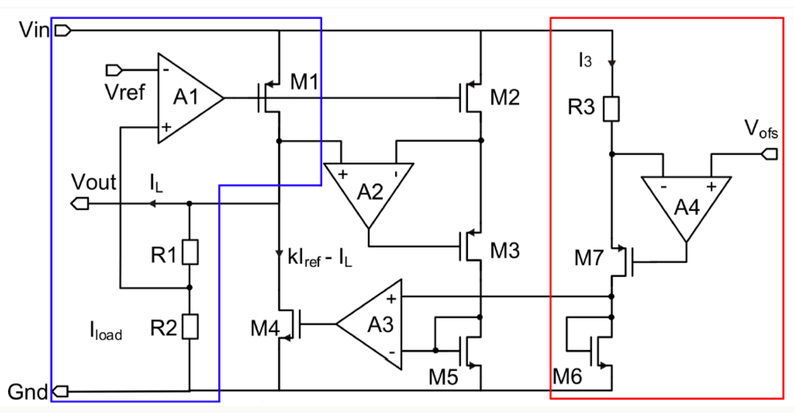


Integration concept for inner endcaps. Two quarter shells will be combined to a half shell and shipped to CERN Number and position of rings not final. [3]

Serial Powering Prototyping

Shunt-LDO Regulators [5]

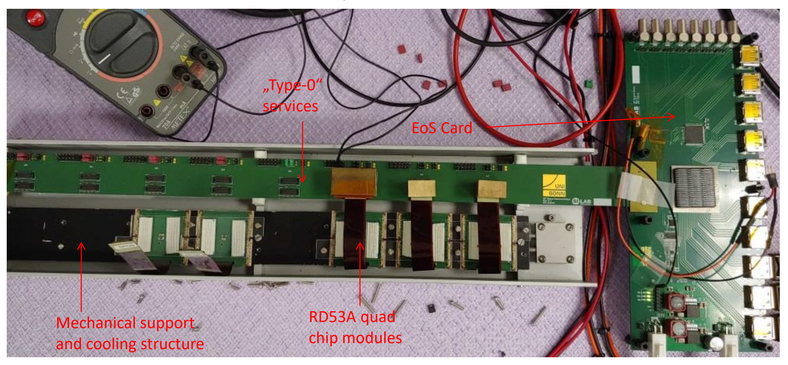
- Regulator to generate readout chip supply voltage from constant current supply, shunting excess current
- Several test chips to prototype design and new features[6] for the future readout chips: Input voltage clamps, overload protection, low-power-mode for testing during integration
- Design and features verified, radiation hardness proven



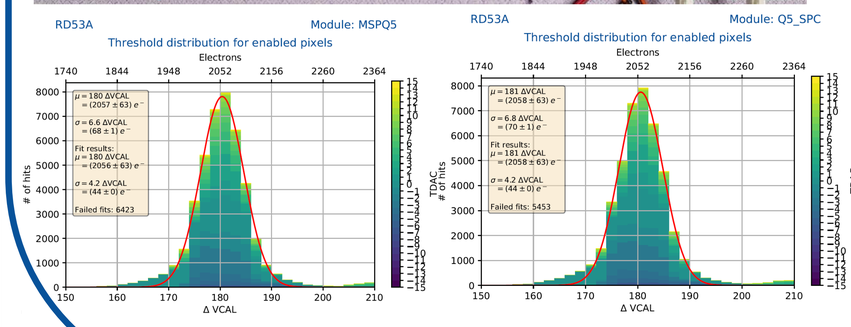
Simplified schematic of the Shunt-LDO regulator. The low dropout voltage regulator is marked in blue. The electrical characteristics are set by the reference Resistor R_3, the current mirror ratio between transistors M_1 and M_2 and the offset voltage V_{ofs}. Excess current is shunted through M_4 . The output voltage is defined by V_{ref} and the resistive divider R_1 and R_2. [7]

RD53A Serial Powering Prototypes

- In Bonn: Prototype to study low-level system aspects on a small, accessible setup
- Up to 16 quads in one chain: commissioning started with digital modules, replaceable with fully functional modules with sensors as soon as available
- First results promising: RD53A modules operational in serial powering chain, performance as expected
- A second iteration of the services is currently being designed to be compatible with ITkPixV1 and fix issues encountered in the first designs
- Several other lab setups available in different institutes



A serial powering chain with RD53A digital quad modules on a simple mechanical support structure. Module flexes, stave flex and End-of-Structure-card are special designs with Extra diagnostics- and debug functionality



Example comparison of the threshold distribution after tuning to a target threshold of 180 Δ Vcal of a single digital RD53A quad module operated stand-alone (left) and in a serial powering chain (right). There is no significant impact observed while operating in a serial powering chain, including possible crosstalk from reading out several modules in parallel.

References

[1] Joao Pequenao, "Computer generated image of the whole ATLAS detector", URL: https://cds.cern.ch/record/1095924

[2] URL: https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/ITK-2020-002/fig_02.png

[3] Caterina Vernieri, private communication

[4] Susanne Kuehn, private communication

[5] Michael Karagounis et al., *An integrated Shunt-LDO regulator for serial powered systems,* ESSCIRC'09 Conference, Athens, Proceedings of ESSCIRC'09, 276

[6] Michael Karagounis et al., *Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades*, TWEPP 2019, Paper under review

[7] Michael Karagounis, private communication

[8] RD53 Collaboration, *Development of pixel readout integrated circuits for extreme rate and radiation,* CERN-LHCC-2013-008 (2013)