ATLAS ITk Pixel Detector Overview

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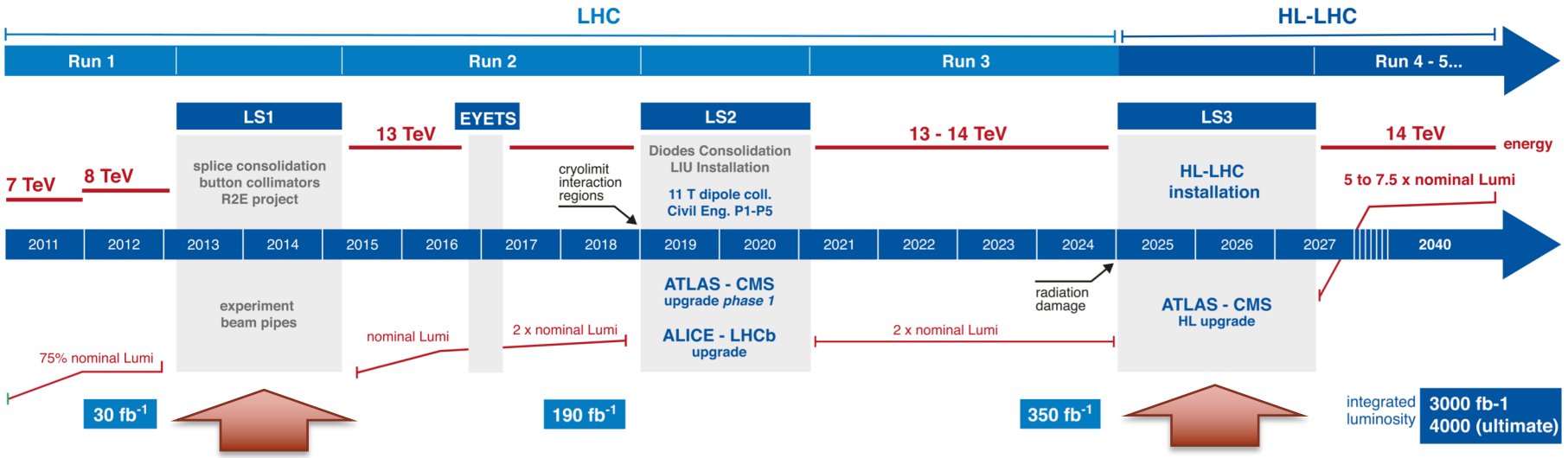
on behalf of the ATLAS collaboration

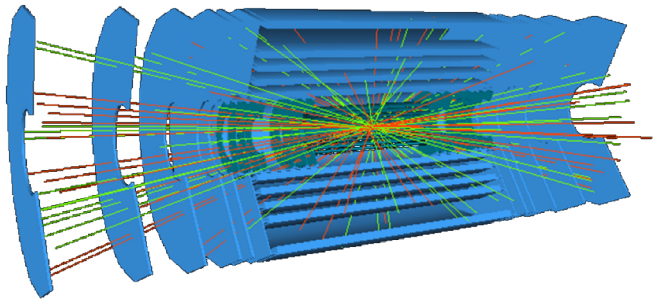
International Conference on High Energy Physics (ICHEP)
Prague, 28th July 2020

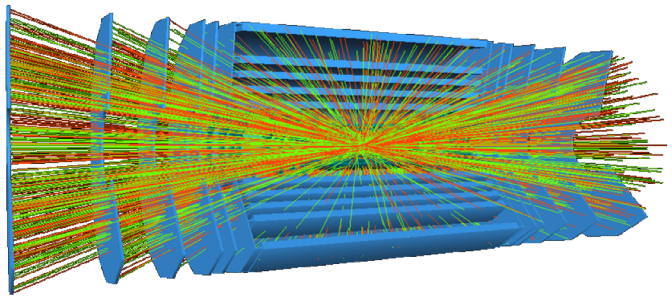
LHC upgrade



Insertable B-Layer (IBL): fourth pixel layer at 3.2 cm from the beam line

"Phase II": full inner detector replacement (5 pixel layers)

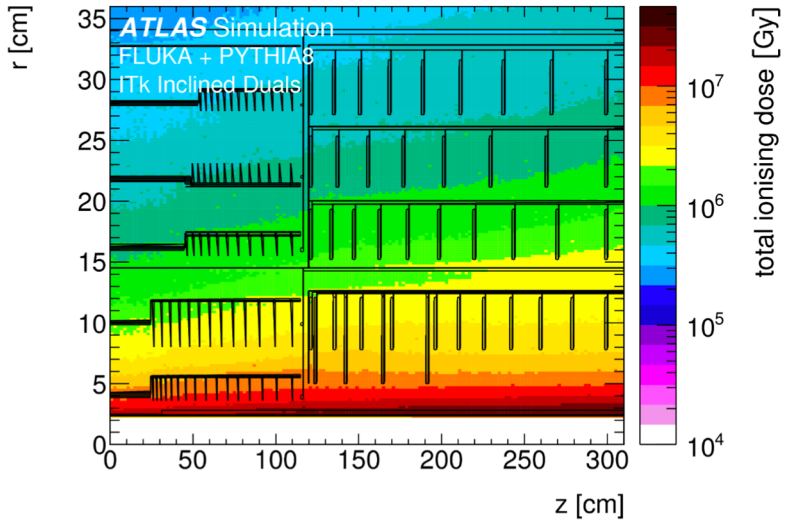


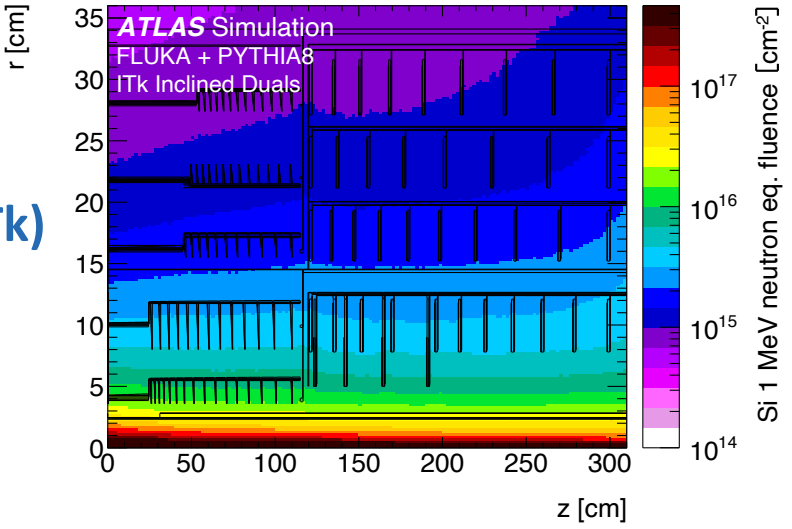


- **LHC**
  - 19 -> 55 Pile-up events
- **High Luminosity LHC (HL-LHC)**
  - 140-200 Pile-up events
    - ➔High particle multiplicity
    - ➔Critical radiation damage

Phase-2 challenges

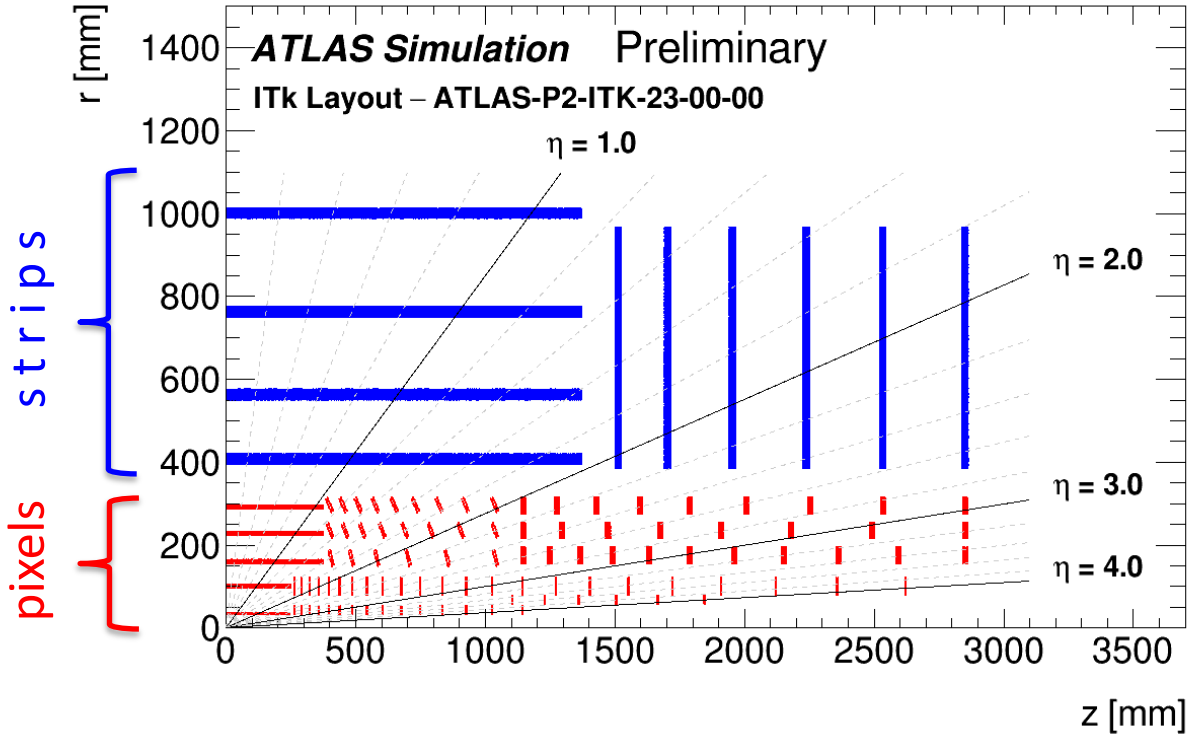
- **Particle multiplicity**
  - About 10 times more track density
    - Needs better tracking granularity
    - Cope with increased readout rates
- **Radiation damage**
  - Radiation dose becomes critical closer to the beam line
    - Total Ionizing Dose (TID) up to 10 MGy
    - Particle fluence up to 2 x 10^{16} $n_{eq}cm^{-2}$ in the pixel region
- **Present Inner Detector system will be replaced with a full silicon Inner Tracker (ITk)**
  - Maintain/improve the present tracking performance in the HL-LHC environment
    - Occupancy < 1%
    - Minimize material
    - Radiation hardness





The new ITk detector

- 4 strip and 5 pixel barrel layers + 2x6 strip disks and pixel ring layers
  - Coverage up to 4 eta with at least 9 space point per track
  - Possibility to replace the two innermost pixel layers (reduce radiation damage)



For the strip detector see next talk by D. Sperlich

Current pixel system

~1.9 m^2 of active area

2000 modules

92 Mega-pixels

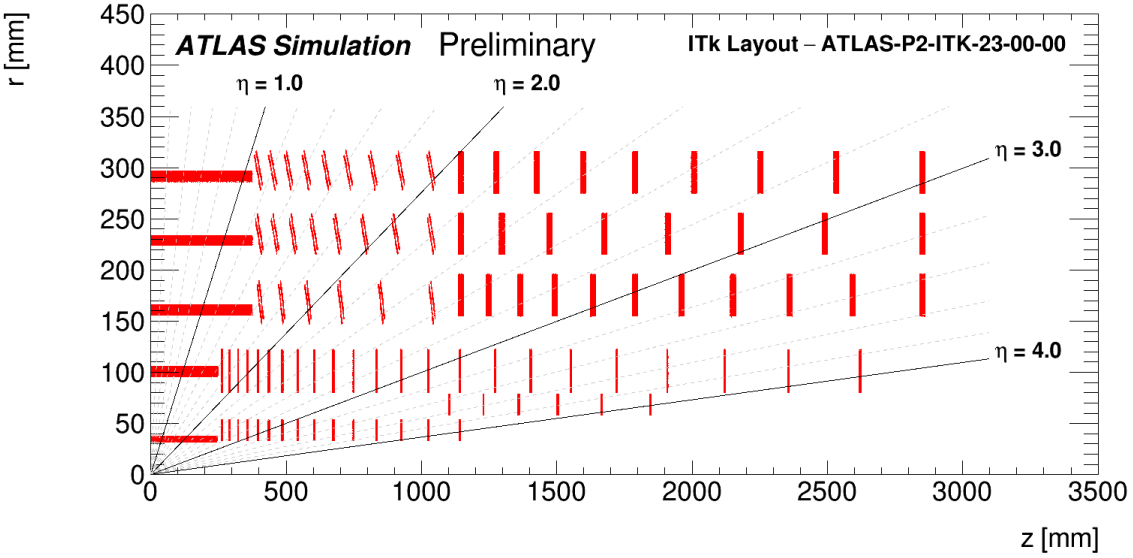
New ITk pixel system

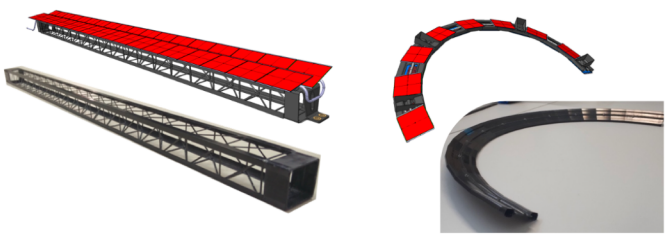
~13 m^2 of active area

9400 modules

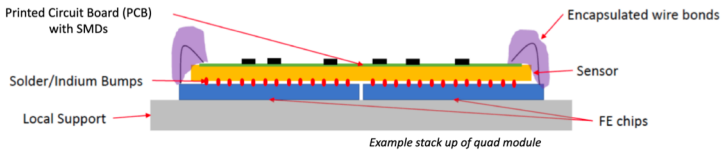
1.4 Giga-pixels

ITk pixel layout

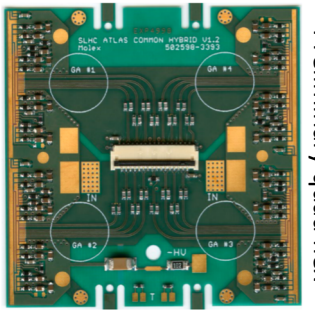




- **Outer Barrel and forward pixels**
  - n-in-p planar silicon sensors (150 µm thick)
  - Quad modules: 4472 (barrel) + 2344 (rings)

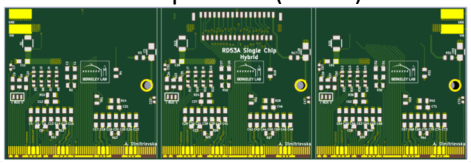


- **Inner pixel layers (replaceable)**
  - Thin n-in-p planar silicon sensors (100 µm thick)
    - Quad modules: 240 (barrel) + 920 (rings)
  - 3D silicon sensors
    - "Pseudo" Triplets modules
      - Single sensors: 288 (barrel) + 900 (rings)
    - 34 mm from the beam line



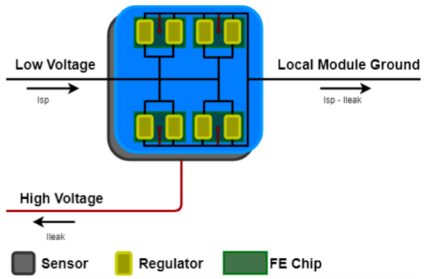
Preliminary quad flex

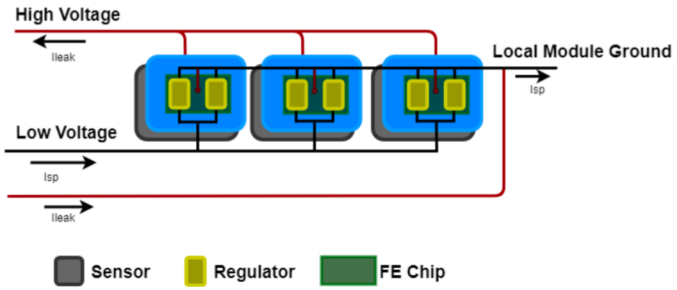
Linear triplet flex (barrel)

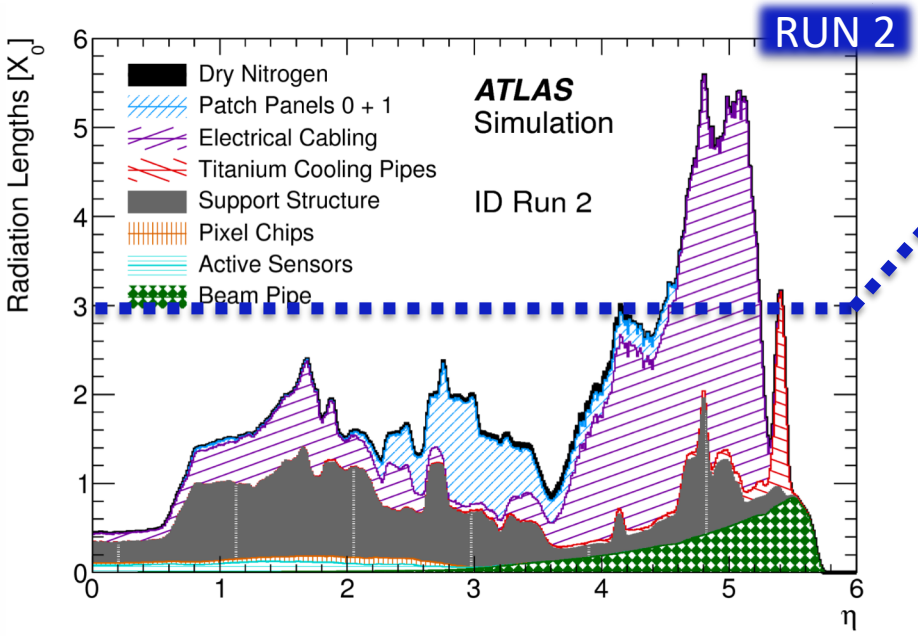


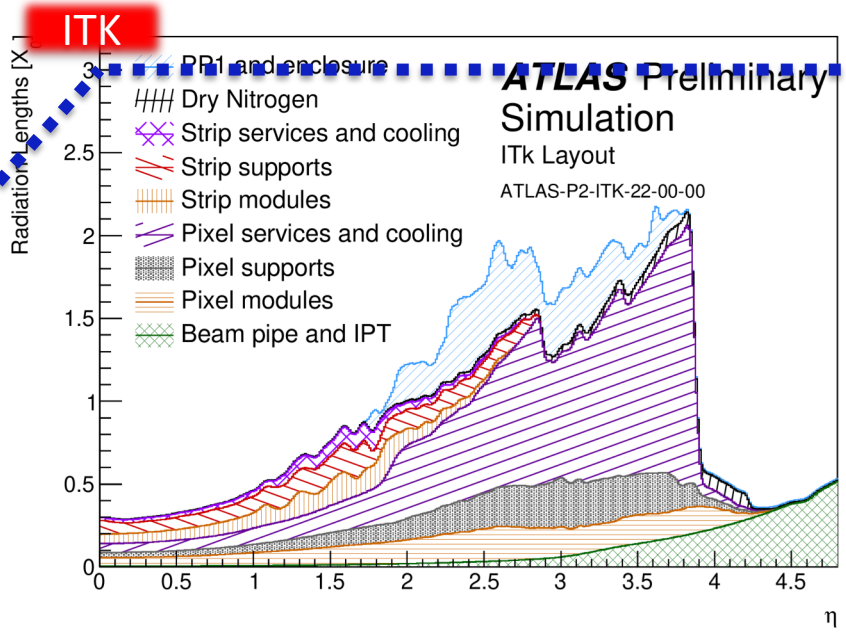
Material budget

- **Reduced material with respect to Run-2**
  - Evaporative CO_2 cooling system with titanium pipes
  - Carbon structures for mechanical stability and mounting
  - Optimised number of readout cables using link sharing
  - Innovative **Serial Powering (SP)** scheme
    - ShuntLDO allow voltage regulation with constant current from the external power source
    - Average chain of about 10 modules
      - LV inside the module distributed in parallel
      - Several HV channel for serial powering chain



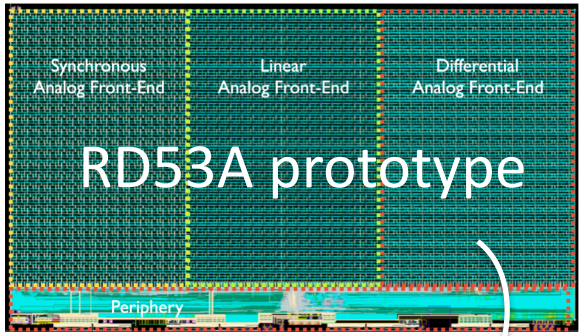




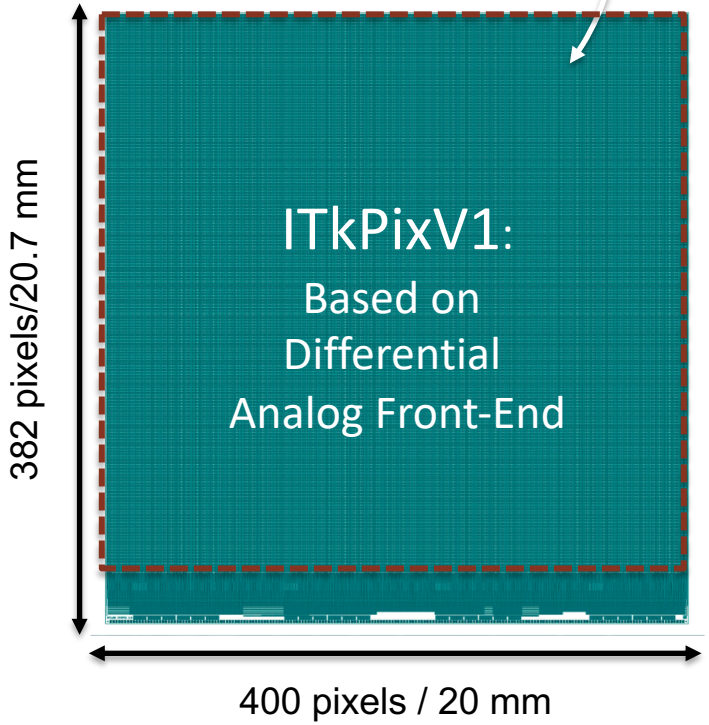


A new Front End chip

- **Present RD53A large prototype in 65 nm**
  - Common ATLAS and CMS R&D
  - Small pixel size: 50 x 50 μm^2
  - Three different Analog Front End (FE)
  - Integrated shuntLDO regulators for serial powering



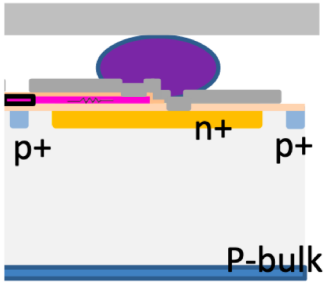
- **Full size chip ITkPixV1**
  - Produced in 65 nm technology
  - Radiation hard > 5 MGy (10^{16} $n_{eq}cm^{-2}$)
    - Single Event Effects (SEE) hardened
  - In time threshold < 1 ke
  - Trigger rate: 1 MHz
  - High hit rate: 3 GHz/cm^2
  - Improved shuntLDO design for serial powering
  - Data format including compression
  - Command forwarding

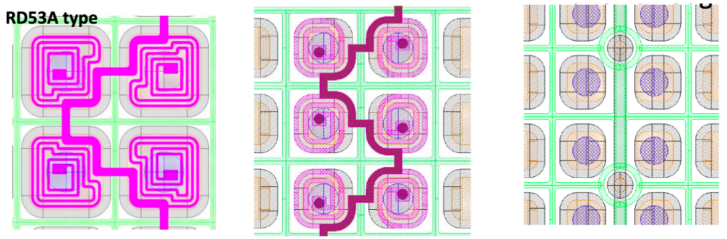


First ITkPixV1 chips ready for module assembly

Planar sensors

- **Thin n-in-p planar sensors**
  - **IBL** is presently using 200 µm n-in-n planar sensors with 50x250 µm^2 pixel cells
  - **ITk** will use n-in-p technology (single side process) with 50x50 µm^2 pixel cells
    - 150 µm for the outer layers
    - 100 µm for the inner Layer-1 (more rad-hard)

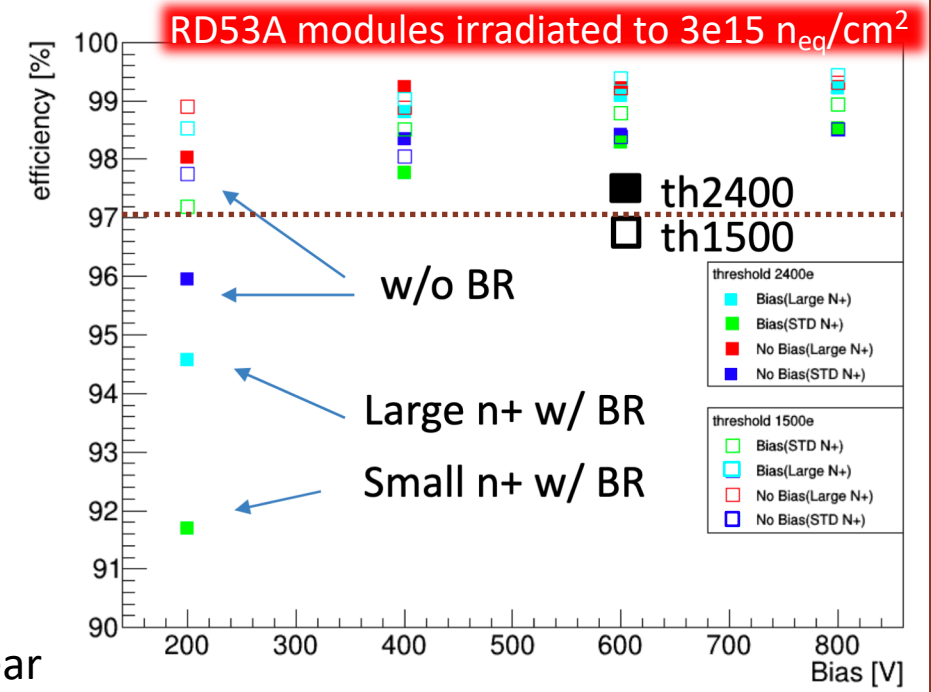




- **Performance required**
  - Hit efficiency >97%
  - Bias voltage at end of life up to:
    - 600 V for 150 µm active thickness
    - 400 V for 100 µm active thickness

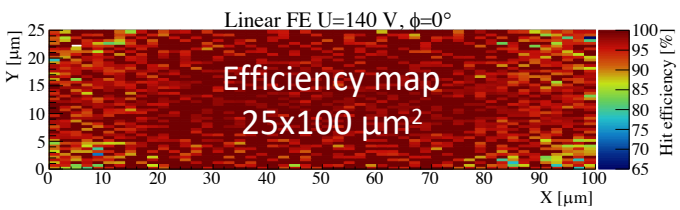
- **Optimisation of the final design**
  - Different biasing solution
    - Punch through (PT)
    - Bias Rail (BR) and bias resistor
    - Temporary Metal (TM)
  - Dimension of the n+ implant

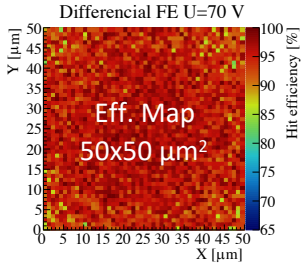
- **Market Survey ongoing…**
  - Results foreseen for the end of the year



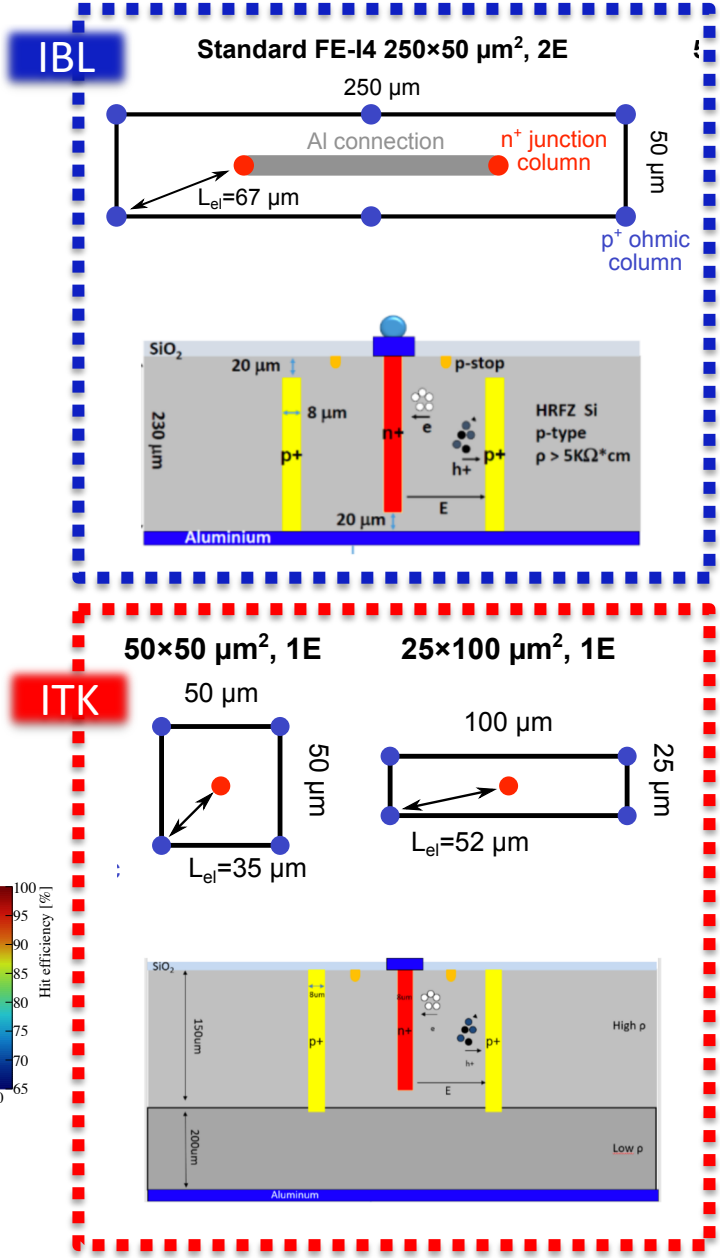
3D sensors

- **New single-side technology**
  - Conductive support wafer (Si-Si)
  - Both electrods etched from the same side
- **Thin active substrates (150 µm)**
  - Reduce cluster size and data rates
- **Small pixels (high occupancy + resolution)**
  - Rings: 50x50 µm^2
  - Flat barrel: 25x100 µm^2
- **Superior radiation hardness (@1e16 n_{eq}/cm^2)**
  - High efficiency: >97%
  - Low operational bias voltage: 80-140 V
  - Low power dissipation < 10 mW/cm^2 (@-25˚C)

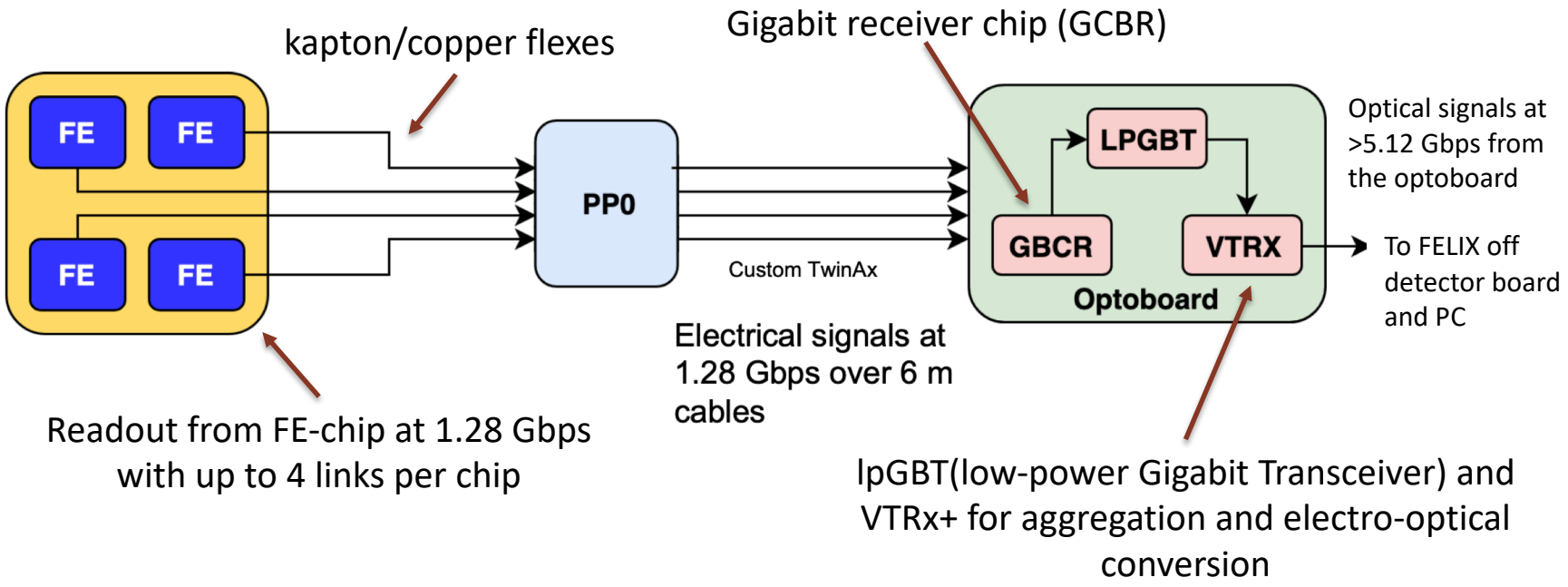




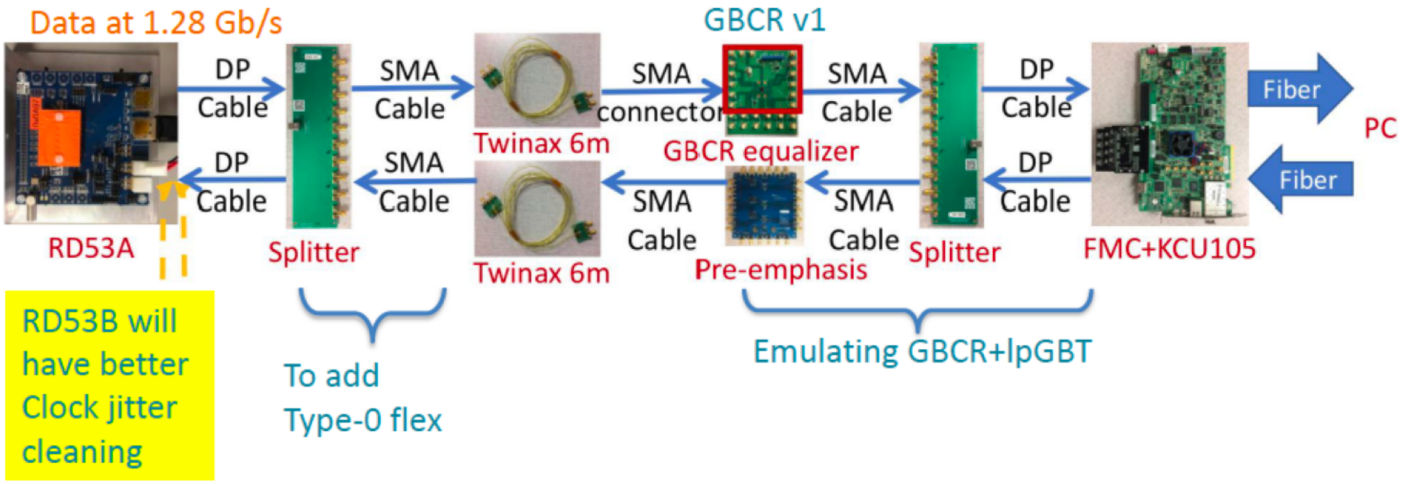
Pre-production already started



Data transmission

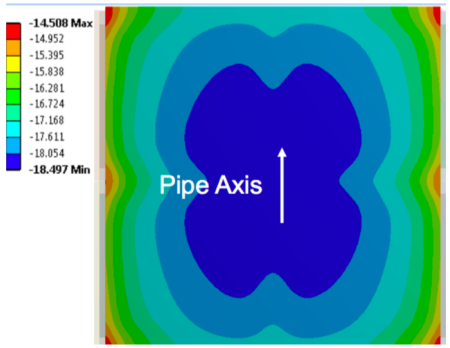


System test development with all elements

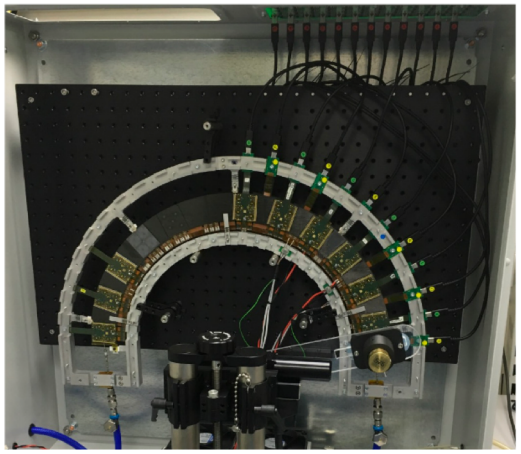


Demonstrator programs

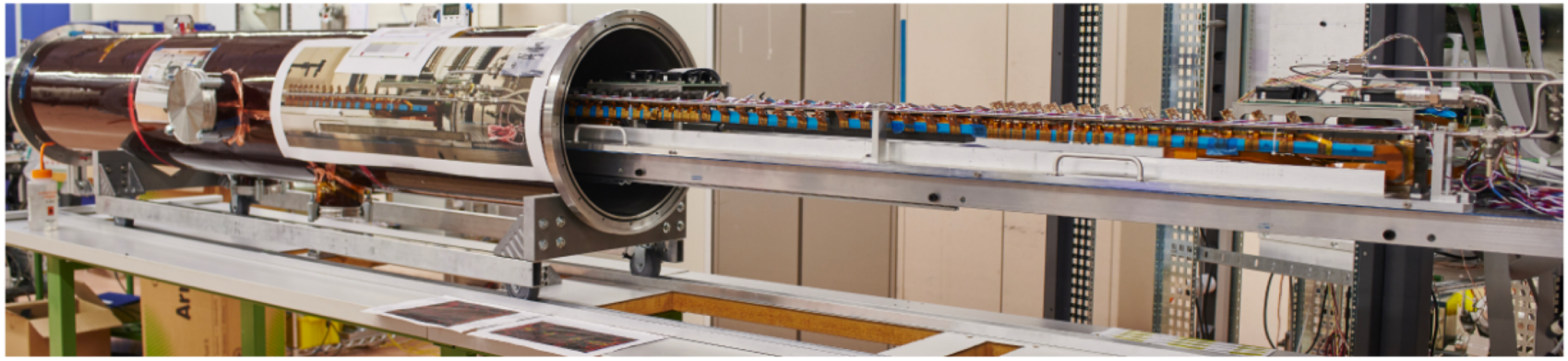
- **Thermo-mechanical studies**
  - Evaluation of thermal performance and manufacturing variability ongoing
  - Simulation results are within thermal specifications



- **Endcap system tests with FE-I4-based prototypes**
  - Double-sided carbon fibre **stave** with 12 quad modules
    - No additional noise observed after mounting
  - **Ring-0**: 12 module ring structure (2 SP chains)



- **Outer barrel demonstrator programme**
  - Thermal and electrical prototypes
  - Full size prototype (1.6 m) with 7 quads and 13 duals
    - 6 serial powering chains with electrical modules



See poster by F. Hinterkeuser

Summary

- **Preparing a new pixel detector to face the HL-LHC challenges:**
  - Radiation hardness
  - Low material
  - Increased granularity

- **The new Inner Tracker: 5 pixel barrel layers and rings**
  - A new radiation hard readout chip **ready**
  - Planar sensors with 50x50 μm^2 pixels (outer layers)
  - 3D sensors with 50x50 and 25x100 μm^2 (innermost layer)
  - Serial powering
  - CO_2 cooling

- **Several Market Surveys, final tests and developments ongoing**
  - Moving from design to **prototyping**
  - Getting **ready** for the pre-productions

Other ITk presentations

TALKS

- Dennis Sperlich (on Tuesday 28)
  The ATLAS ITk Strip Detector System for the Phase-II LHC Upgrade

POSTERS

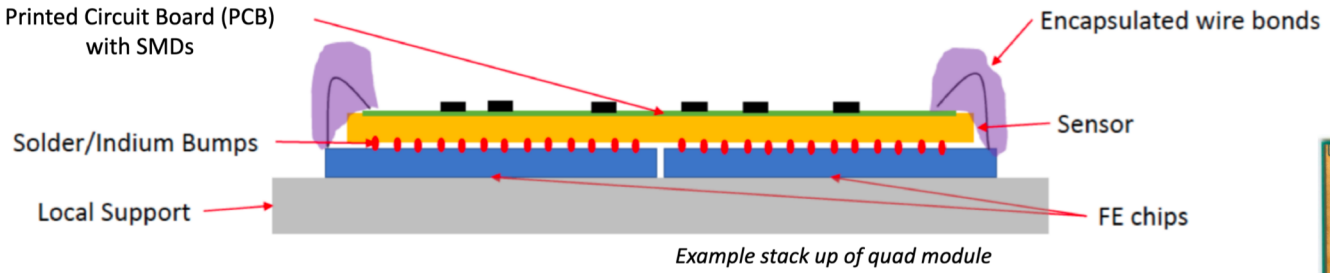
- Florian Hinterkeuser (on Thursday 30th)
  Development and evaluation of prototypes for the ATLAS ITk pixel detector

- **Test Beam Studies of Barrel and End-Cap Modules for the ATLAS ITk Strip Detector before and after Irradiation**

- **Radiation-Hard Silicon Strip Sensors for the ATLAS Phase-2 Upgrade**

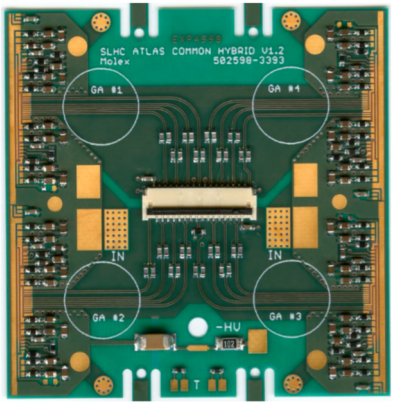
BACKUP

Module concept



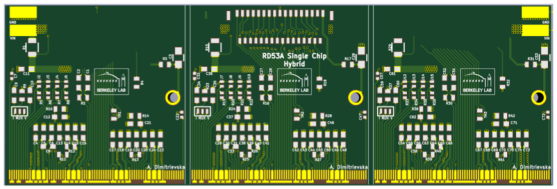
Example stack up of quad module

Preliminary quad flex



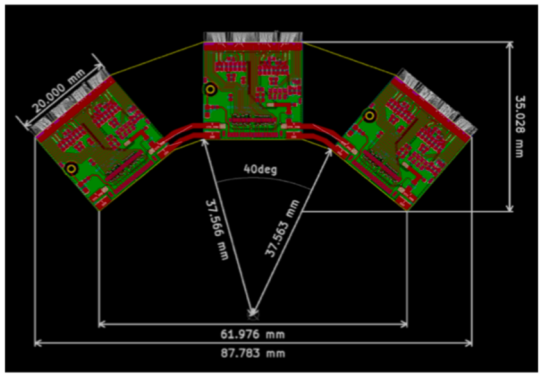
- **Quad module (outer layers and rings)**
  - 1 large single sensor bump bonded to 4 readout chips
  - Common design for all outer layers
  - Longest Serial Powering (SP) chain of 14 modules

Linear triplet flex (barrel)



- **Pseudo Triplets (innermost layer and rings)**
  - 3 single-chip bare modules connected to the same flex
  - Power and ground in parallel + 1 data connector
  - Limited space for services -> SP is essential
    - Longest SP chain in L0: 5 SP units in endcap rings

Ring triplet flex (rings)



- **Wire-bond encapsulation**
  - Damage protection and to avoid corrosion
  - Evaluating Parylene, mechanical protection and alternative materials