

SiPM characterisation and updates on the scintillator and FEE designs

POLAR-2 biweekly meeting

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- 1** **The Hamamatsu S14616 SiPM**

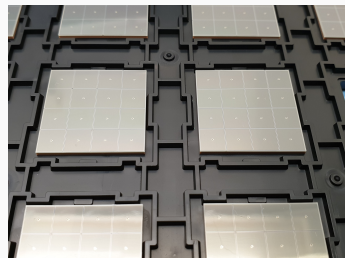
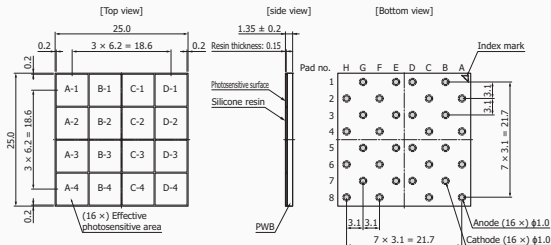
- 2** **I-V measurements and break-down voltage**

 - Measurement setup (probe station)
 - Results
- 3** **I-V measurements vs. temperature and dark noise**

 - Measurement setup (industrial probe station)
 - I-V curves evolution with temperature
- 4** **POLAR-2 module prototypes**

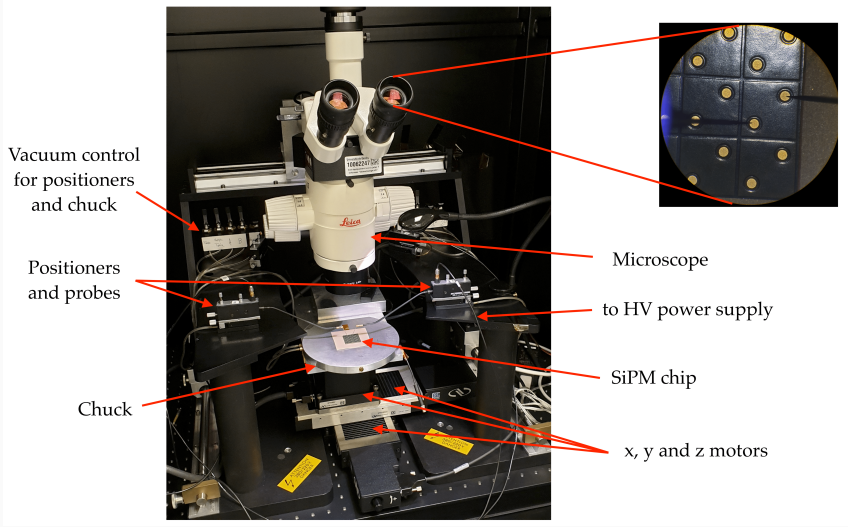
 - Baby mind board and first module prototype
 - New scintillator and grid designs
- 5** **Summary and work to come**

The Hamamatsu S14616 SiPM

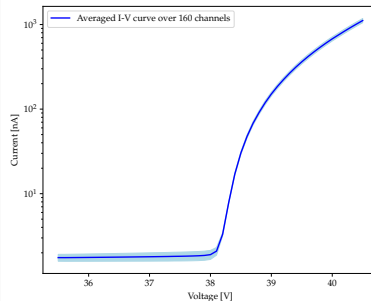
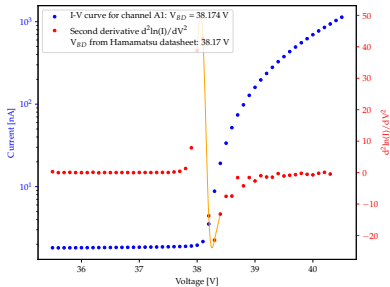
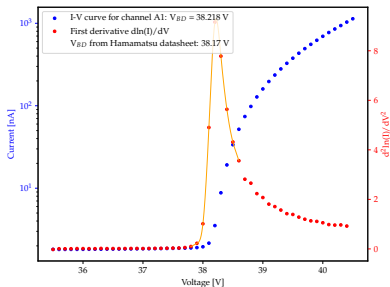


Type	S14161-6050HS-04
Geometrical fill factor	74%
Operating temperature	-40 to +85°C
Spectral response range	270-900 nm
PDE @450 nm (max)	50%
Breakdown voltage	38 V
Recommended V_{OP}	$V_{BD} + 2.7$
V_{OP} variation across array	typ. ± 0.05 , max. ± 0.1 V
Cross talk probability	7%
Dark current	typ. 2.5, max. 7.5 μ A
Terminal capacitance	2000 pF
Gain	$2.5 \cdot 10^6$
Temperature coefficient	34 mV/°C

→ Hamamatsu datasheet

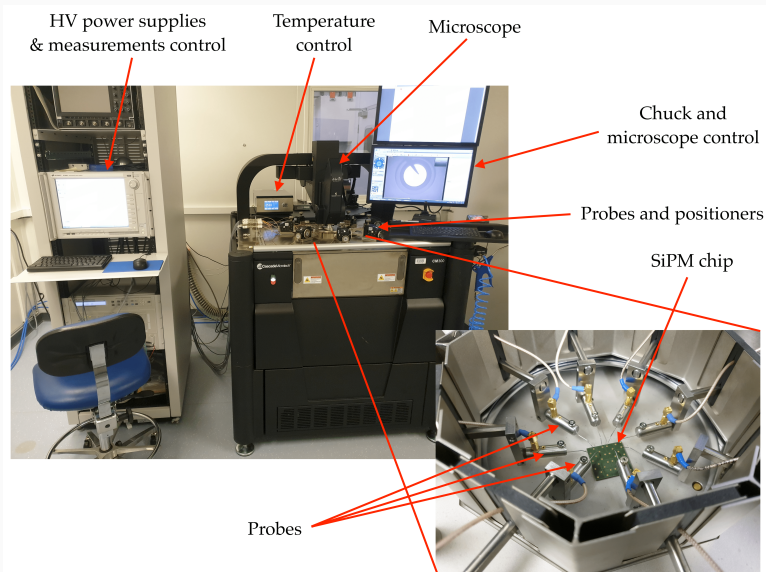


I-V curves and break-down voltages

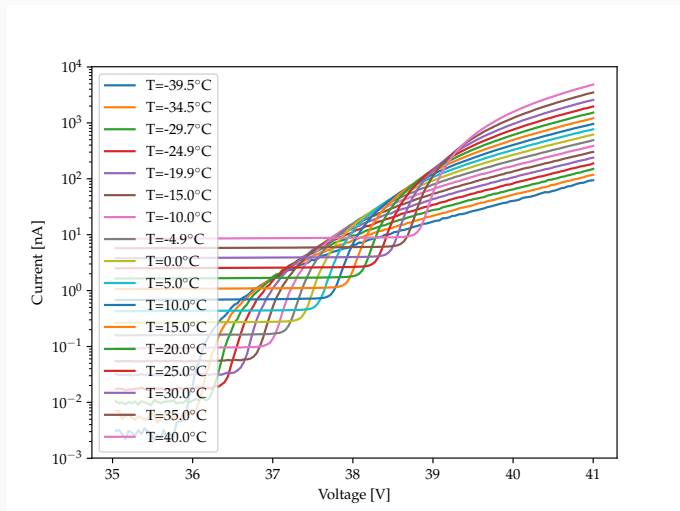


→ I-V curves very stable between the different channels and arrays of SiPMs
 → Break-down values to be compared with datasheet provided by Hamamatsu

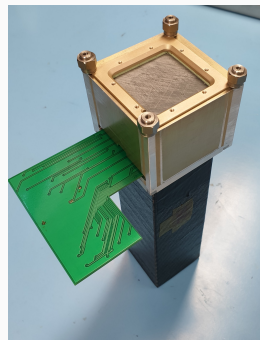
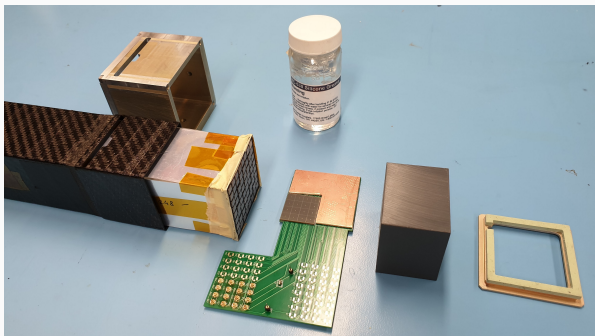
Setup for measurements vs. temperature

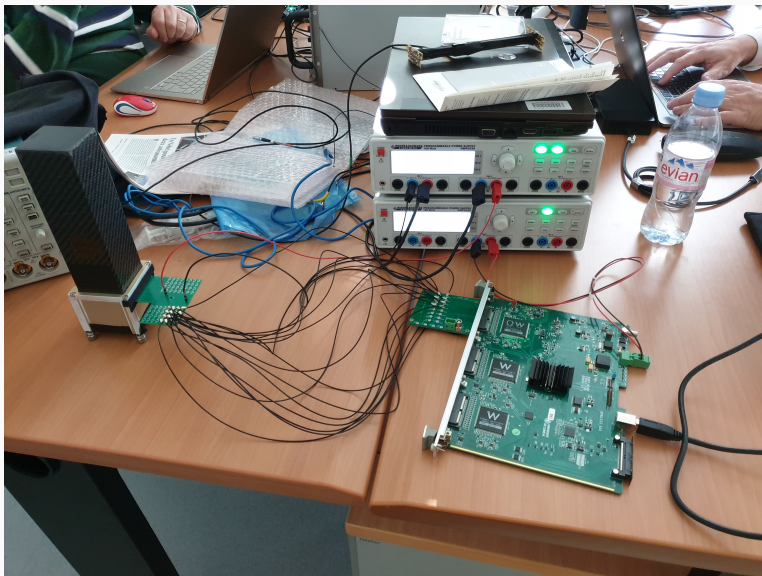


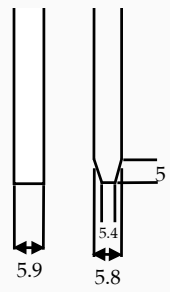
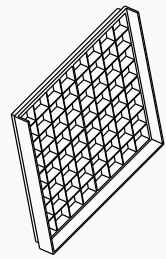
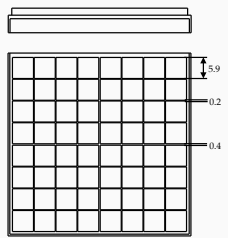
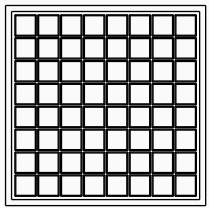
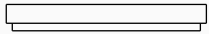
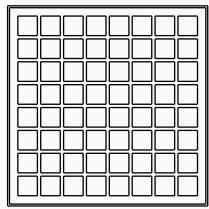
I-V curves evolution with temperature



→ Break-down and dark noise vs. temperature have still to be extracted







Summary and work to come

- I-V characteristics seems very stable among the different SiPM chips, temperature coefficient and dark noise vs temperature have still to be extracted from data
- incoming tests for SiPMs: I-V curves down to -60°C for one chip, measurement of the quenching resistor, measurement of the DCR vs. temperature
- A first 1/4 of module has been built and some preliminary tests with the BabyMind board (based on CITIROC ASIC) have been performed
- The BabyMind board has been upgraded and its FW updated, a proper front-end PCB is under production \rightarrow incoming tests on module prototypes, 2 modules with the SiPMs that we have
- Scintillator bars and grids designs have been modified \rightarrow no more truncation (bars ~ 3 times cheaper), bigger bars (5.9mm^2 instead of 5.8mm^2)
- Fake scintillator bars have to be printed to do some mechanical tests with the new grids designs (grid prototypes are being printed at CERN)

