Readout system for the phase I of the LHCb VELO upgrade

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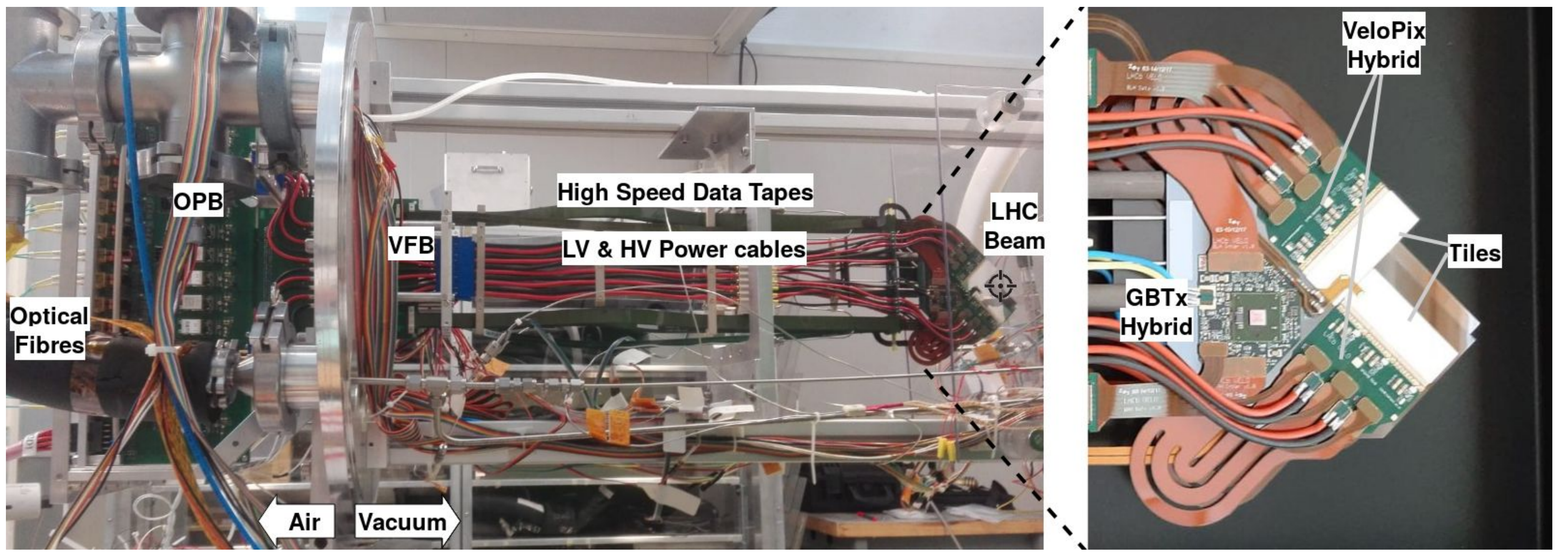
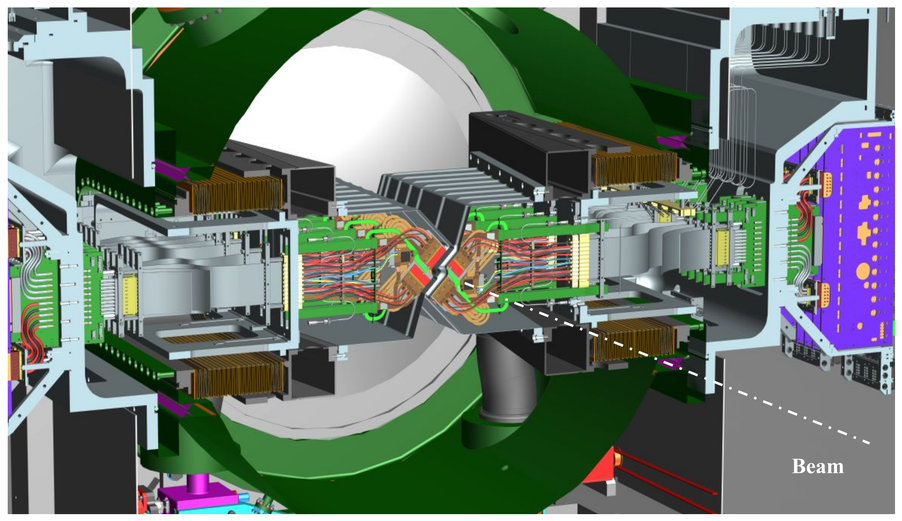
LHCb and VELO Upgrade

The LHCb collaboration plans to change key features of the present detectors for Run III, moving to a full detector readout at 40MHz and operating at a luminosity of $2x10^{33}cm^{-2}s^{-1}$. The new readout scheme and operation conditions will require the replacement of many sub-detectors among which is the VErtex LOcator (**VELO**).
VELO is the primary tracking and vertex detector that surrounds the interaction point. It will use hybrid pixel detectors (55µm x 55µm) composed of silicon sensors bump-bonded to the new **VeloPix** [1] CMOS readout chips designed to be readout at the LHC clock rate. The whole VELO will be composed by 52 modules with 4 sensors each. A sensor will be readout by 3 VeloPix ASICs, mounted in a mechanical frame capable of moving the sensors away from the beams when LHC is not in stable colliding beam mode.



Slice view of a VELO upgrade prototipe (left), close view of a module (right)



The VELO Upgrade CAD view

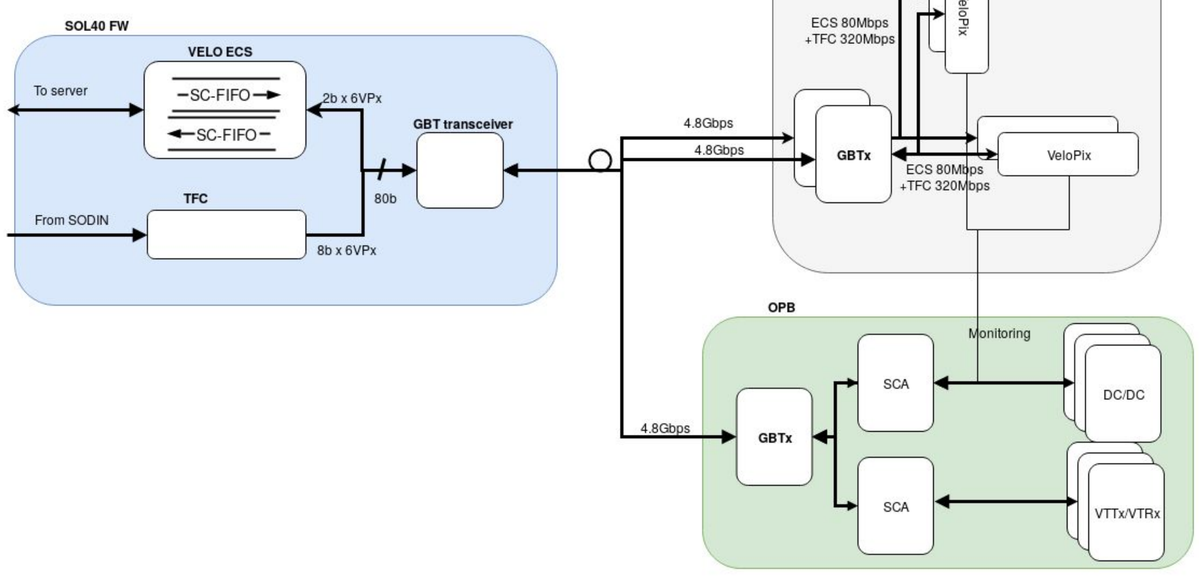
LHCb Off-detector electronics

Off-detector electronics, placed at the ground level, are responsible for the underground detector operation by controlling and taking data synchronously at the LHC clock rate.
A LHCb common back-end board [5] is design to act as supervisor (S-ODIN), control (SOL40) and readout board (TELL40), called PCIe40, based on the Intel Arria 10 FPGA and which function is defined by the firmware flavour. PCIe40 board will be controlled and read out from a PCI express slot. The LHCb detector comprises one readout supervisor board. This board receives the 40 MHz clock of the LHC and distributes it along the detector but also generates the signals that keep all sub-detectors synchronous.

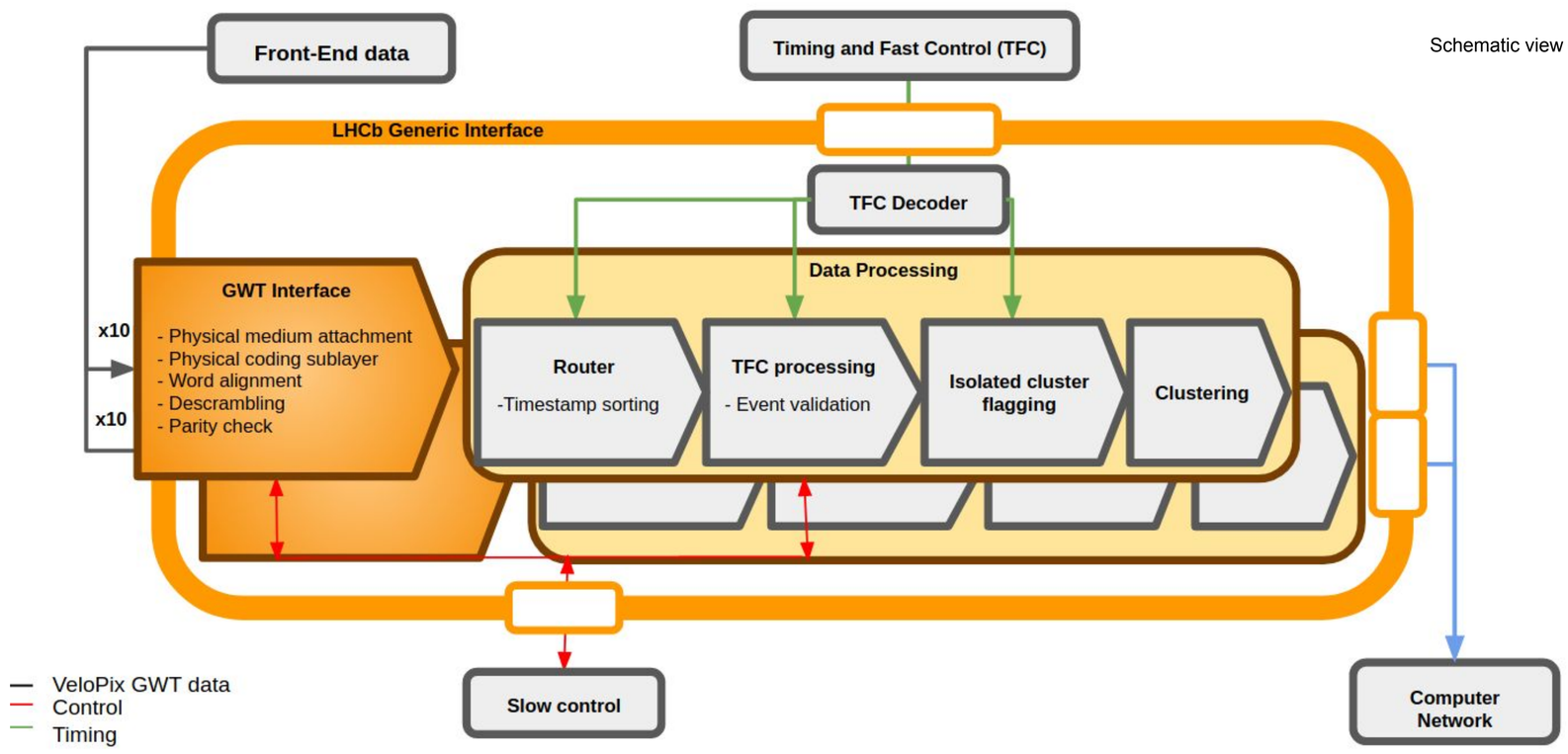
Besides that, the supervisor card contains information about the LHC filling scheme that is used to accept events only with collisions in the interaction point. Readout and control interface board firmwares are developed in a LHCb wide common framework with provision made for sub-detector specialization. In order to reduce firmware complexity in the readout board, two independent datastreams are instantiated.

VELO control and timing firmware

LHCb sub detector front-ends are controlled in a centralized way. A series of read/write registers in the PCIe40 boards that controls the hardware are accessed from a server that interfaces with the different SCADAs. In the case of VELO front-end ASICs the communication with the server is done by a FIFO memory. The interface between the previously mentioned FIFO and the front-end is done by serializing the word at 80Mb/s and encapsulating it in a GBT frame that goes directly to the GBTx ASIC in the module.
VELO's firmware receives timing commands from the centralized S-ODIN and encapsulate it in the same GBT word shared with the control signals and send it to the front-end GBTx ASIC and therefore to the consequent VeloPix ASIC.



Schematic view of the control firmware for the VELO SOL40 that distributes the control and timing signals to the front-end



VELO TELL40 firmware scheme

VELO Upgrade on-detector electronics

A VELO slice is composed by a module with 12 VeloPix ASICs controlled over two multipurpose radiation tolerant bidirectional link ASIC (**GBTx**) [2]. Readout data are driven at ~5 Gb/s from the VeloPix ASIC over almost a meter of copper, converted into optical and send out to the back-end readout boards.
The transmission lines that control and read out the module are divided in 3 sections: The first starting from the module are four ~50cm **flexible tapes** that absorb the telescopic displacement of the module, the second is the Vacuum Feedthrough Board (**VFB**) that deals with the differential of pressure between the VELO secondary vacuum and the air, and finally the third section is the Optical and Power Board (**OPB**) that performs the optical conversion of the transmission lines. The OPB also monitors the voltages and temperatures as well as feeds the low voltage to all on-detector electronics through 14 DC/DC converters (FEASTMP) [3]. One GBTx and two GBT-SCA ASICs [4] are used for the control and monitoring.

VELO Readout firmware

The specific characteristics of the Velopix (GWT serializer, and unordered data by bunch count) require an ad-hoc firmware design. The only LHCb common developments included are the event generation and PCIe interface. The whole VELO must handle around 3 Tb/s of data distributed in 52 TELL40 boards (1 per VELO slice) with these main firmware blocks:

- **GWT interface** is the first layer of the firmware and is responsible for recover the data from the optical fibers, which is a customised and more extended version of the physical layer (PHY) of the OSI model. As the VeloPix uses its own serializer and protocol, GWT, a VELO LLI needs to be developed by customizing the Intel standard physical medium attachment and creating a new GWT physical coding sublayer.
- **Data Processing**
  - **Router**, The main processing function of the back-end readout boards for VELO is performed in the router and consists in sorting the VeloPix unordered data (by bunch count) by its timestamp in real time. The Router sorts the 10 input links at the same time with an average of 22 packets per bunch cross. The router uses a two stages Multiple Input Multiple Output (MIMO) algorithm that stores the output in 512 RAM segments.
  - **TFC processing** block converge the data scattered in multiple RAM segments and propagate only the valid data synchronously within Intel standard format "Avalon-ST" and the LHCb Run 3 data format.
  - **Isolated Cluster Flagging** search to determine if a SuperPixel has a neighbour or is completely isolated. A bit is asserted on the output of each SuperPixel to indicate if It is isolated.
  - A real time **Cluster** algorithm for FPGA is being implemented, releasing the computing resources and time from the CPU farm. The design of the clustering is being made keeping a relatively small amount of FPGA resources to make it fit in the PCIe40 board.
  - The TELL40 receives the timing information per buch cross from the S-ODIN and stores it in a RAM memory. VELO's timing mechanism triggers the data acquisition when the **Pre-Router** receives a certain number of synch commands from the VeloPix, this information is propagated to the **Post-Router** where the core of the sync mechanism is implemented. The Post-router sync mechanism reads the information per event from the previously mentioned RAM starting from the synch event and propagates the data according to the content of the RAM.

VELO Bypass firmware

A parallel design to the data acquisition firmware was developed with the aim of having a reliable way of adquire raw front-end data synchronously with a reference telescope in a testbeam, besides that this firmware will be used in the module production sites.
The **data processing**'s code is a completely new design that stores the data on individual FIFO per link. These memories are readed whenever one of the links is receiving data, and the output multiplex the link with higher priority to the link with greater occupancy sending the output data directly to the PCIe interface.
In order to work in the test beam a synchronization mechanism is included. It takes the command that triggers the data acquisition and sent it out from an LVDS output to the Telescope.

References

[1] T. Poikela et al.,"The VeloPix ASIC", JINST 12 (2017) C01070
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[3] FEAST Radiation tolerant 10 W Synchronous Step-Down Buck DC/DC converter, CERN, 2014
[4] A. Caratelli et al., "The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments", JINST, March, 2015, Art. no C03034
[5] M Bellato et al., "A PCIe Gen3 based readout for the LHCb upgrade", Journal of Physics, Conference Series, 513, 2014, no. 1, 012023

2020 LHCC

Poster session

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Research project:
-FPA2017-89204-C2-1-P. Búsquedas de nueva Física con el experimento mejorado LHCb del CERN.
-FPA2014-57896-C4-1-R. Desafíos presentes y futuros del experimento LHCb del CERN.