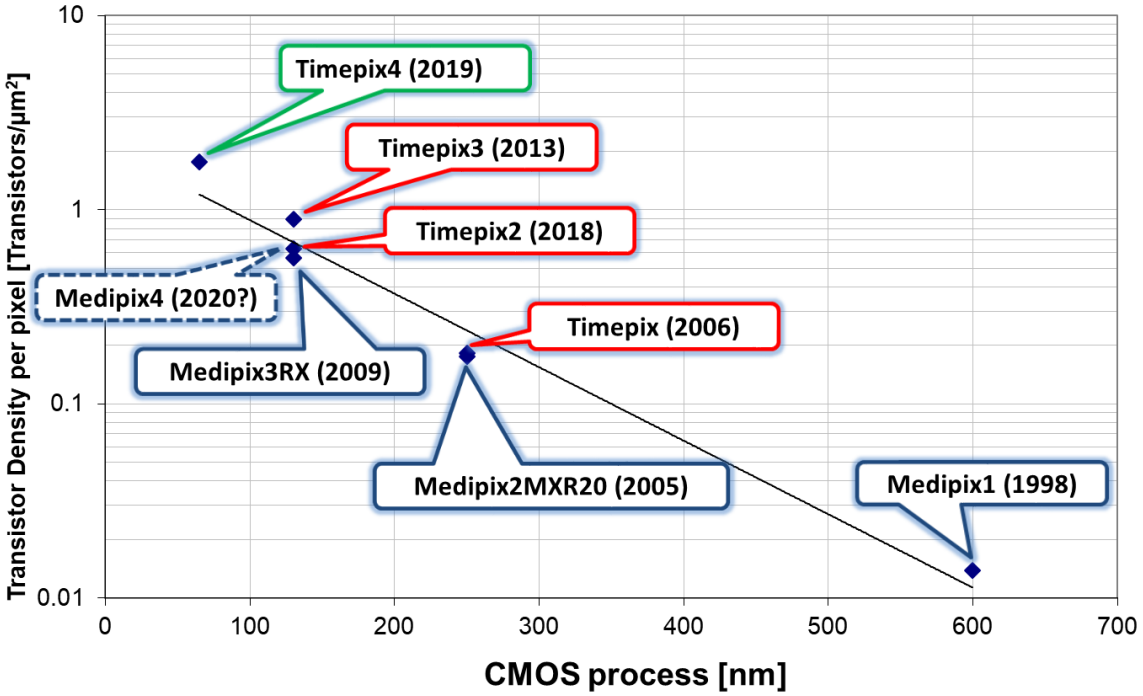
The Timepix4 design parameters

X. Llopart,
On behalf of the Medipix4 Collaboration

11th February 2020

Medipix4 Collaboration (from 2016)



Timepix4: A 4-side tillable large single threshold particle tracking detector chip with improved energy and time resolution and with high-rate imaging capabilities

CEA, Paris, France

CERN, Geneva, Switzerland,

DESY-Hamburg, Germany

Diamond Light Source, Oxfordshire, England, UK

IEAP, Czech Technical University, Prague, Czech Republic

JINR, Dubna, Russian Federation

NIKHEF, Amsterdam, The Netherlands

University of California, Berkeley, USA

University of Houston, USA

University of Maastricht, The Netherlands

University of Canterbury, New Zealand

- University of Oxford, England, UK
- University of Geneva, Switzerland
- IFAE, Barcelona, Spain
- University of Glasgow, UK

15 members

Timepix4 applications

- Data-Driven applications:
  - HEP:
    - Very high rate pixel telescope
    - Sensor studies (high speed)
    - Beam gas interaction (PS SPS/LHC?)
    - AeGIS/ASACUSA
    - ATLAS background rad monitor and TRD detector
    - MOEDAL
    - GEMPIX / large area TPC
    - Test vehicle for next gen LHCb-VELO with tens of ps time resolution
  - Time-of-flight mass spectrometry
  - Neutron time-of-flight imaging
  - Radiation monitors
  - Electron microscopy
  - X-ray and powder diffraction
  - Compton camera for medical diagnostics
  - Sub-pixel resolution imaging
  - Gamma and neutron imaging for nuclear industry and Homeland Security

- Frame-based imaging applications:
  - X-ray imaging in synchrotrons with extreme high rates > 10^9 particles/mm^2/s

- 20th Anniversary Symposium on Medipix and Timepix
  - https://indico.cern.ch/event/782801/

Timepix4 main requirements

- Use of a commercial 65nm CMOS process
- Build a 4-side buttable “as large as possible” pixel array
- Particle identification and tracking (Data-driven and zero suppressed)
  - Sub-ns time binning
  - Improve the energy resolution
- Imaging (frame based with CRW sequential readout)
  - Increase particle count rate
- Designers:
  - CERN: R. Ballabriga, T. Poikela, E. Santin, V. Sriskaran, N. Egidos and X. Llopart
  - Nikhef: V. Gromov and A. Vitkovskiy
  - IFAE: R. Casanova

Timepix3 → Timepix4

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	**6.94 cm^2**	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**5x**
TOT energy resolution			< 2KeV	< **1Kev**	**2x**
TOA binning resolution			1.56ns	**195ps**	**8x**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)	**4x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	**32x**
Target global minimum threshold			<500 e^-	<500 e^-	

Timepix4 floorplan arrangement

- 512 x 448 of 55 x 55 µm pixels

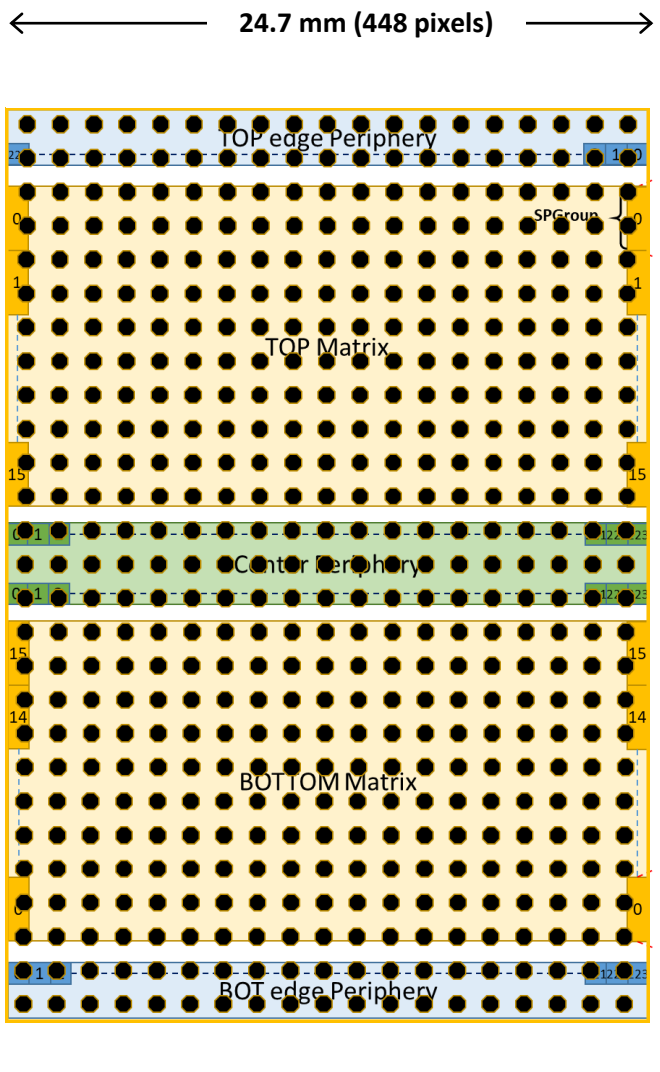
- 3 “hidden” peripheries with TSV (Through-Silicon-Vias):
  - TOP Edge: Data Readout & Slow Control
    - 147 TSVs/WBs: 106 POWER/GND and 41 IO
  - BOTTOM Edge: Data Readout & Slow Control:
    - 147 TSVs/WBs: 106 POWER/GND and 41 IO
  - CENTER: Slow Control and Analog Blocks (DACs, ADC, Band-Gaps…)
    - 147 TSVs: 124 POWER/GND and 23 IO

- On-chip bump to pixel redistribution layer (RDL)

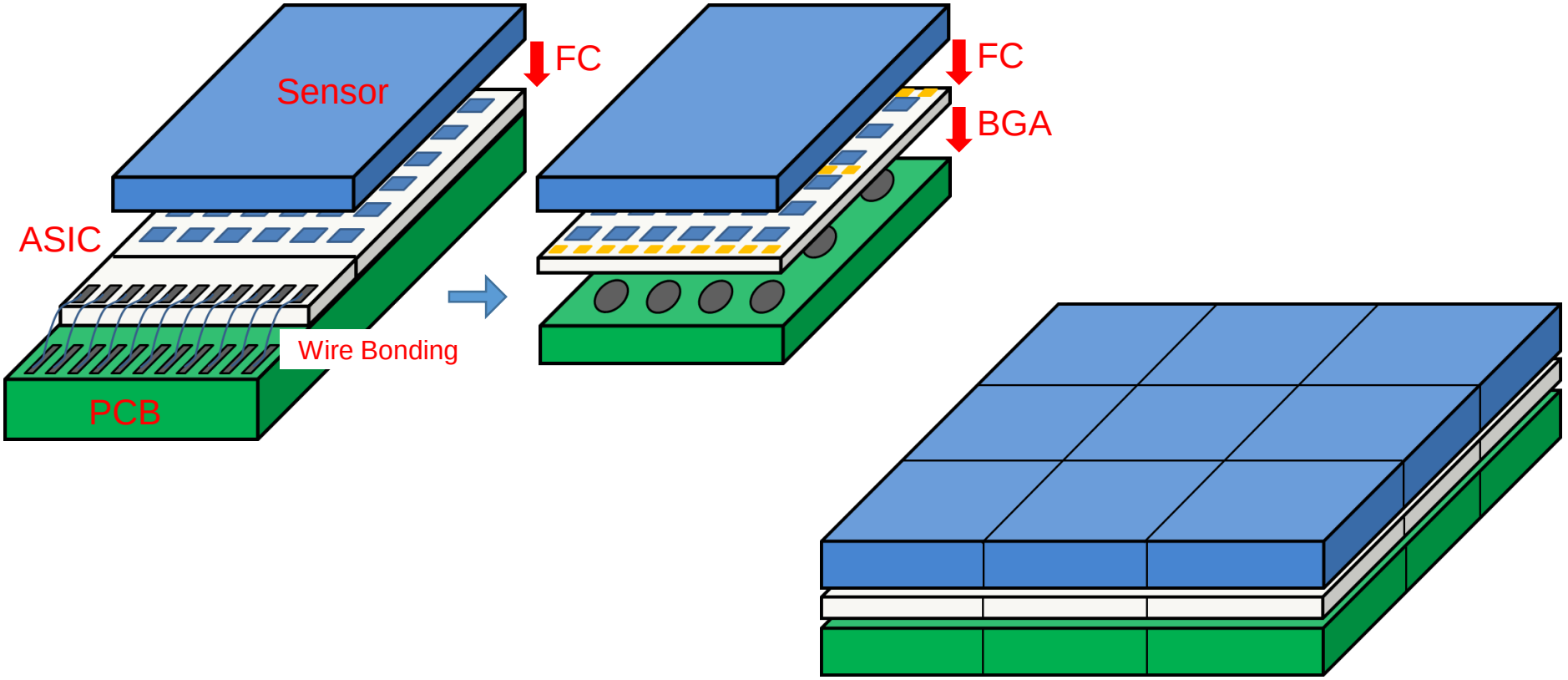
- Chip size:
  - With WB (wirebonds extenders): 29.96 mm x 24.7 mm
    - **>93.7%** active area (28.16mm x 24.64mm)
  - Without WB (TSV Only) : 28.22 mm x 24.7 mm
    - **>99.5%** active area (28.16mm x 24.64mm)

- Control architecture allows to operated Timepix4 from any of the 3 peripheries:
  - i2C protocol
  - Custom Slow Control protocol
  - Interface to DAQ:
    - Through 3xTSVs
    - Through 2xWB

- Fast readout requires at least 1 serial link enabled in each edge periphery:
  - Serial links are highly configurable 40MBps → 10GBps

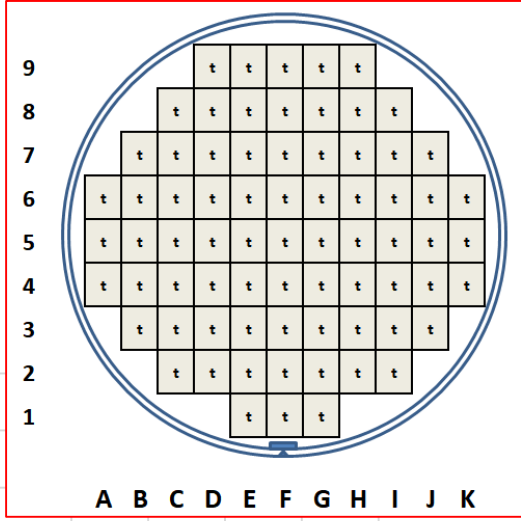


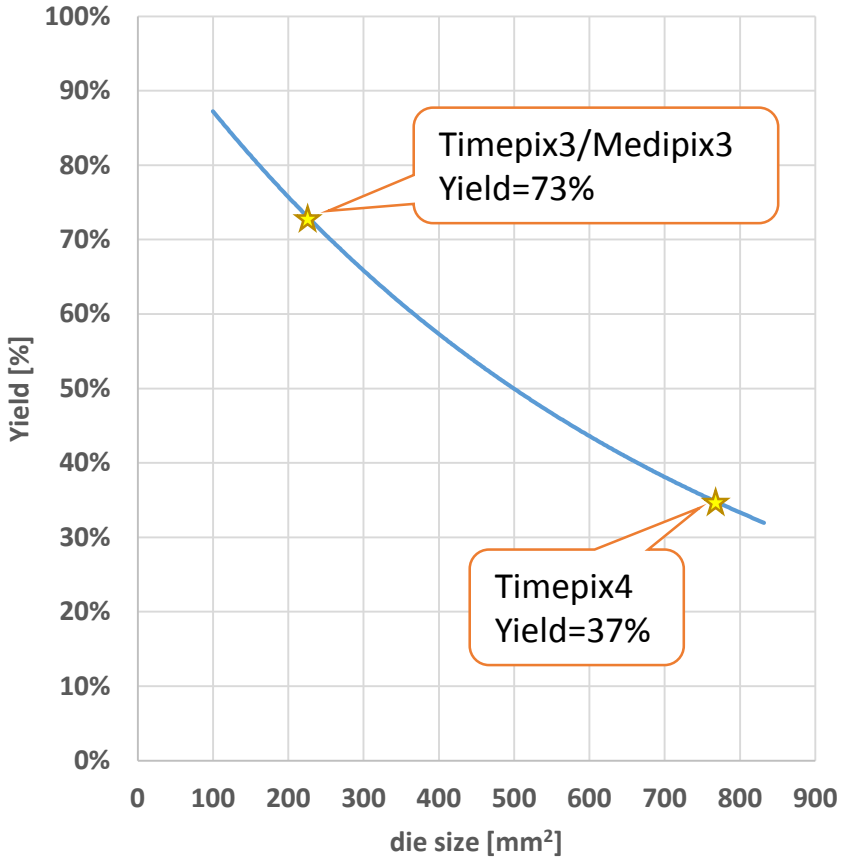
4-side buttable pixel arrangement

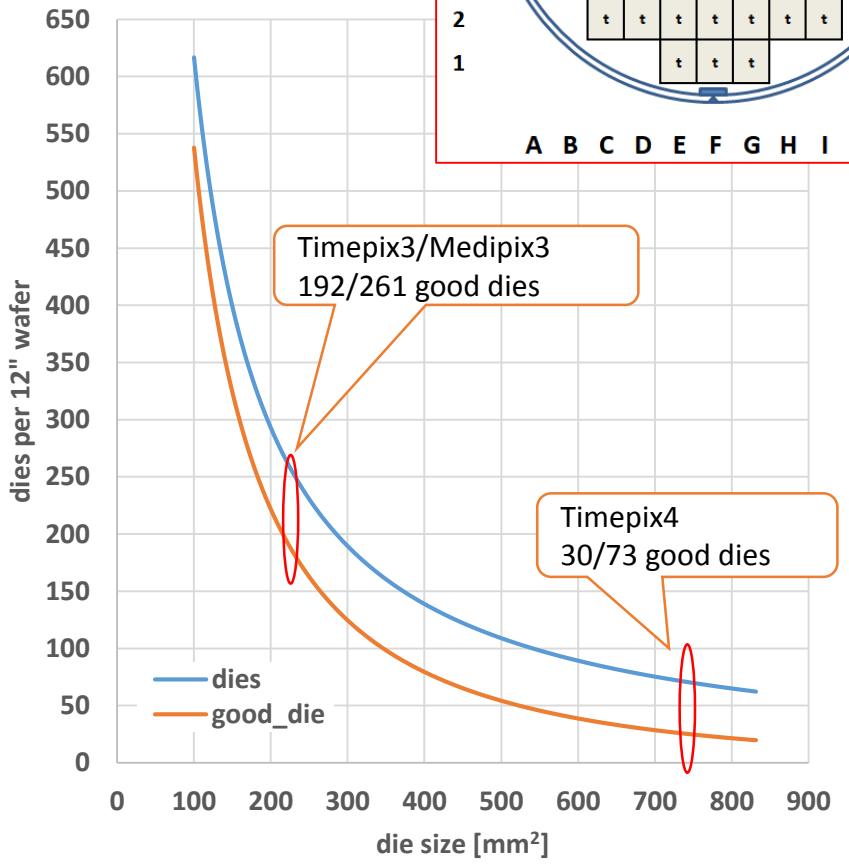


- Target to build **large area detectors** by combining smaller modules
- The through-silicon vias (TSVs) is the key technology for this paradigm shift

Expected Timepix4 Yield

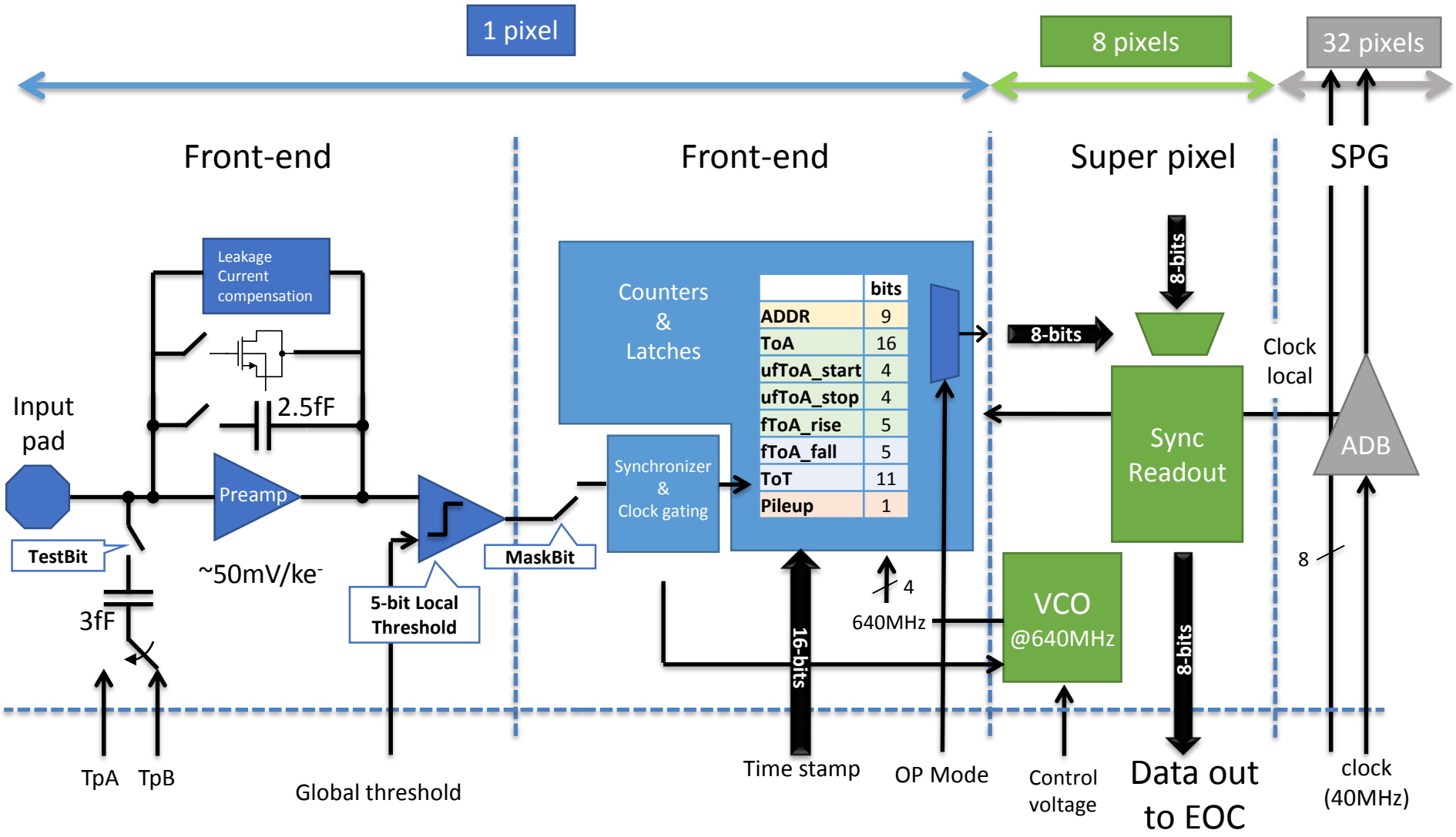




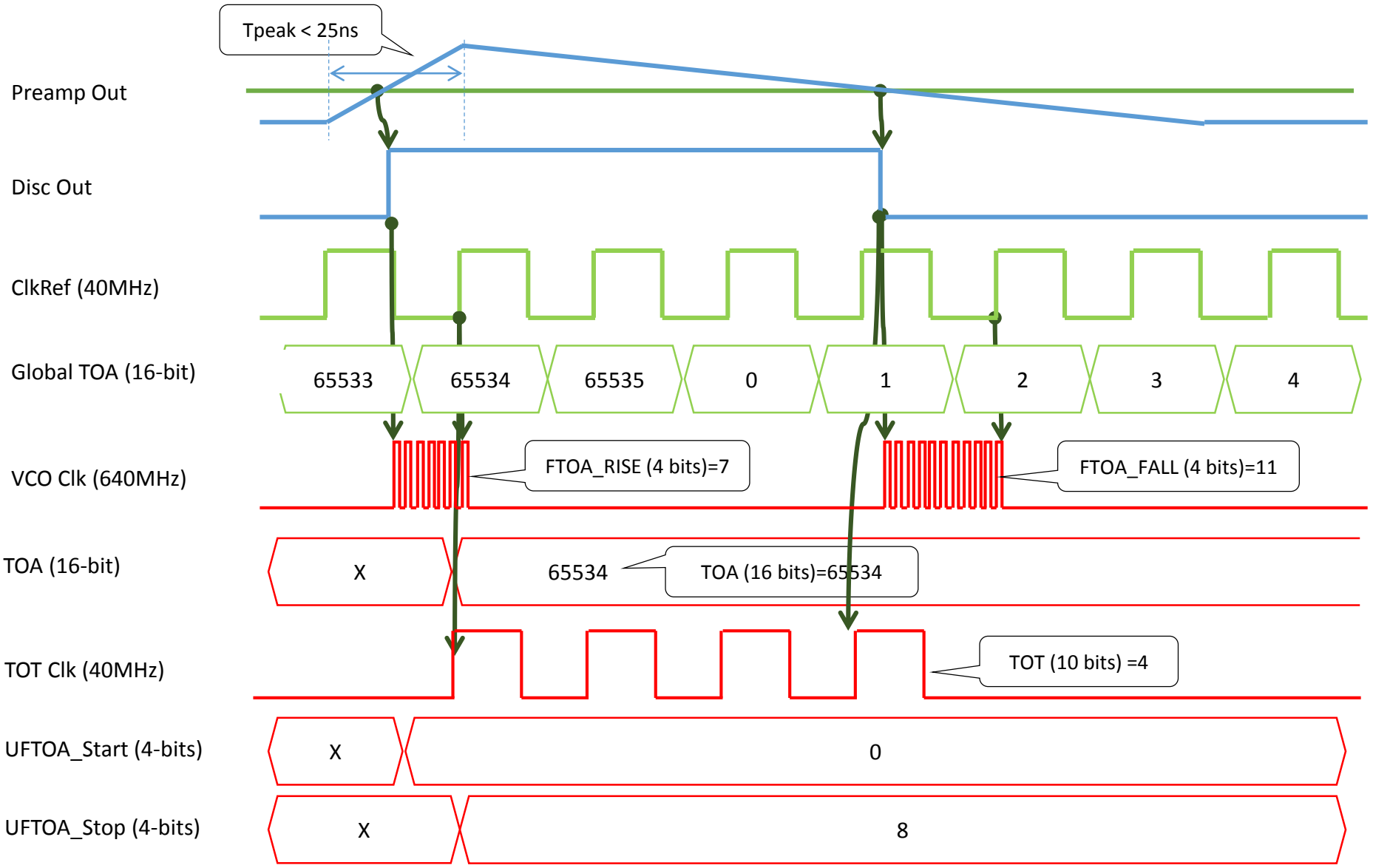


*Based in the foundry yield model for perfect dies

Timepix4 Pixel Schematic



Pixel Operation in TOA & TOT [DD]

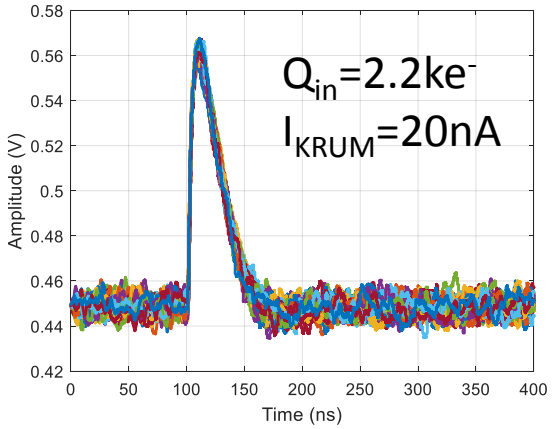


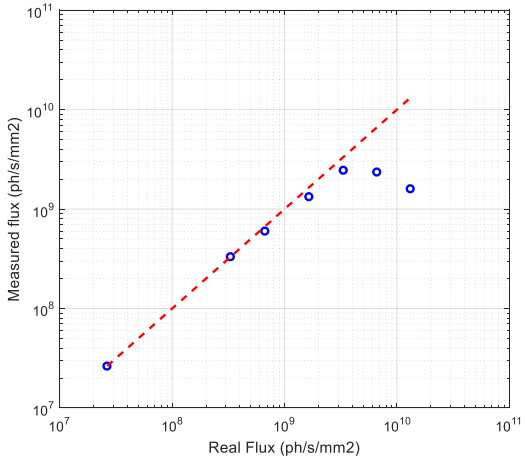
Timepix4 FE

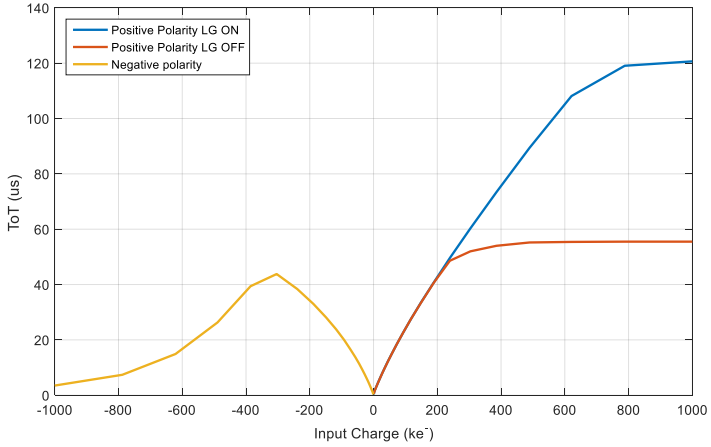
R. Ballabriga

- The Timepix4 chip front-end has to be versatile in order to be used:
  - With different types of sensors:
    - Bipolar detection and <10nA leakage currents (high-Z materials)
  - In tracking and as well in imaging:
    - **Imaging at high rates** (e.g. synchrotrons) imposes a minimum pulse width. In order to be at the state of the art in terms of rate capability, the dead time of the front-end should be smaller than ~200ns.
    - **Tracking applications** impose an input jitter in the front-end below 50 ps_{rms} (time bin 195 ps)

- FE architecture follows the "classic" Medipix approach (Krummenacher FE)
  - Gain adjustment (log gain in hole collection)
  - Improved for low jitter and fast count-rate when required → power







Timepix4 Slow control and Readout

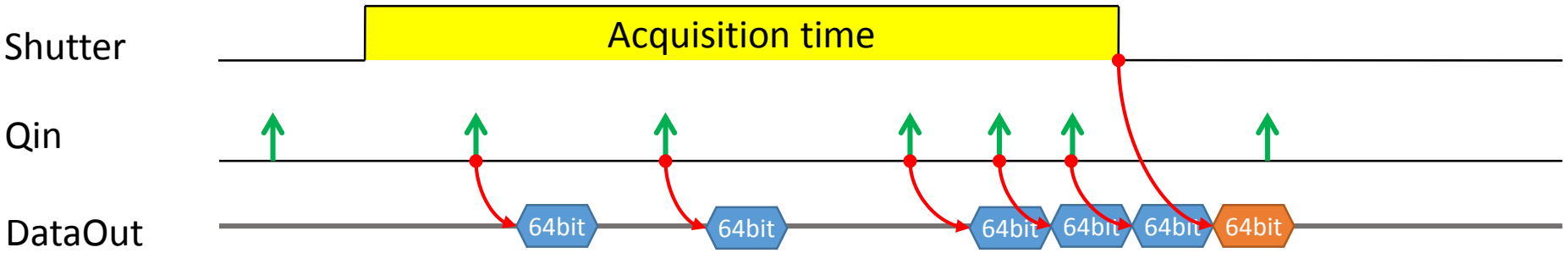
- Timepix4 has separated readout and control data paths

- **Slow control (SC)**:
  - Protocols:
    - I2C protocol
    - Custom serial slow control protocol (< 40 MHz)
  - Slow control operation can be done from any of the 3 available peripheries
  - Registers:
    - Pixel matrix configuration > 2 Mb (8-bit/pixel + 24-bit/spgroup)
    - Peripheral registers (DAC settings, operation modes, e-fuses, ….)

- **Data readout (DAQ)**:
  - Each half matrix readout through its correspondent edge periphery
    - 8 serializers in each periphery with < 81.92 Gbps
  - Uses a 64/66b standard protocol
  - Zero-suppressed and data driven readout → 64-bit data packet/hit
    - TOA/TOT mode
    - 24b data-driven Photon Counting (PC) mode
  - Full frame with Continuous-Read-Write (CRW):
    - 8-bit or 16-bit Photon Counting (PC) mode

Timepix4 Readout Modes : Data-Driven

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
  - Uses 64b/66b standard encoding communication protocol



SPEC: Packet specifications ToA/ToT				
Name	**Width**	**MSB**	**LSB**	**Bits**
Top	1	63	63	[63:63]
EoC	8	62	55	[62:55]
SP	6	54	49	[54:49]
Pixel	3	48	46	[48:46]
ToA	16	45	30	[45:30]
ufToA_start	4	29	26	[29:26]
ufToA_stop	4	25	22	[25:22]
fToA_rise	5	21	17	[21:17]
fToA_fall	5	16	12	[16:12]
ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

Address: 18 bits

Time: 29 bits

Energy: 21 bits

Timepix4 Readout Modes : Frame-based

- Full frame readout with continuous read-write (CRW):
  - No zero-suppressed → no pixel address sent
  - 8-bits or 16-bit counter depth
  - Uses 64b/66b standard encoding communication protocol
  - Frame rate limited by bandwidth:
    - **16-bit @ 8Ghits/mm²/s > 1.28 Gbps → ~370 fps up to 44.6 Kfps @ 163.84 Gbps**
    - **8-bit @ 1Ghits/mm²/s > 20.48 Gbps → ~11.8 Kfps up to 89.2 Kfps @ 163.84 Gbps**

16-bit frame

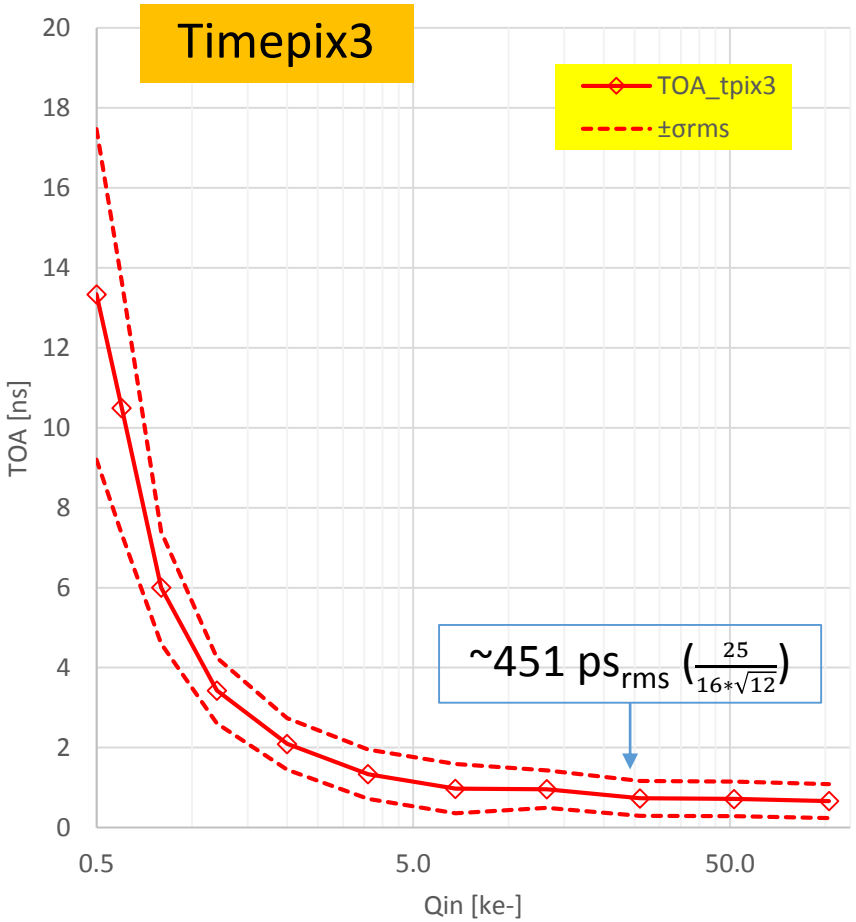
Name	Width	MSB	LSB	Bits
Pixel 3/7	16	63	48	[63:48]
Pixel 2/6	16	47	32	[47:32]
Pixel 1/5	16	31	16	[31:16]
Pixel 0/4	16	15	0	[15:0]

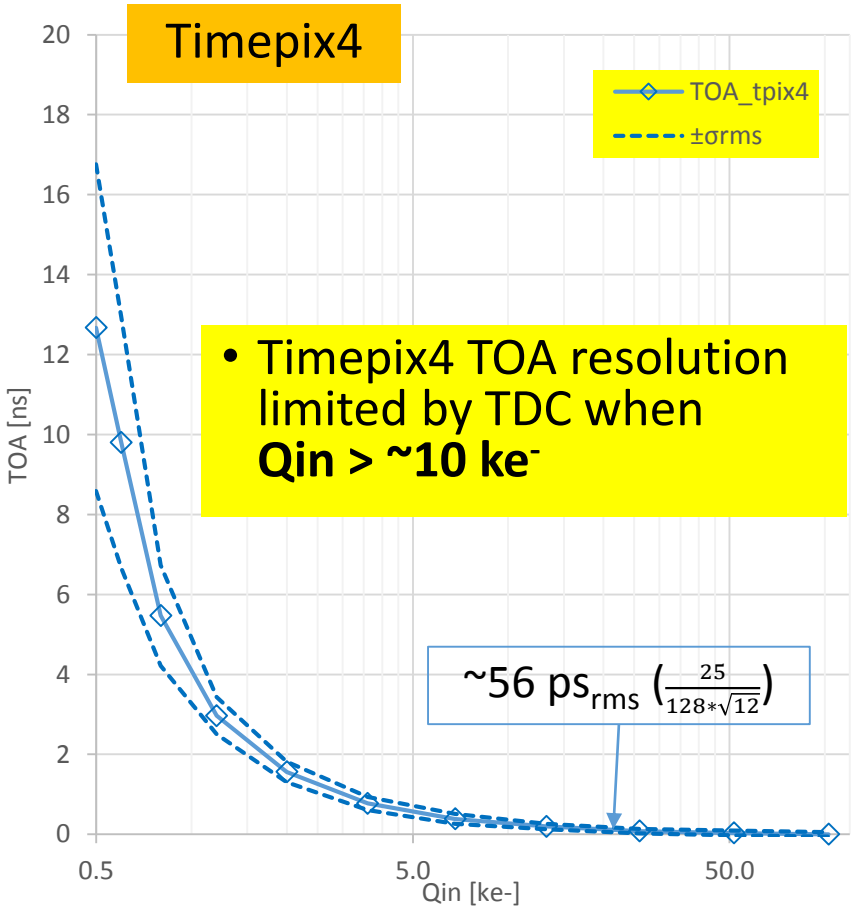
8-bit frame

Name	Width	MSB	LSB	Bits
Pixel 7	8	63	56	[63:56]
Pixel 6	8	55	48	[55:48]
Pixel 5	8	47	40	[47:40]
Pixel 4	8	39	32	[39:32]
Pixel 3	8	31	24	[31:24]
Pixel 2	8	23	16	[23:16]
Pixel 1	8	15	8	[15:8]
Pixel 0	8	7	0	[7:0]

On-pixel TDC simulations → TOA resolution

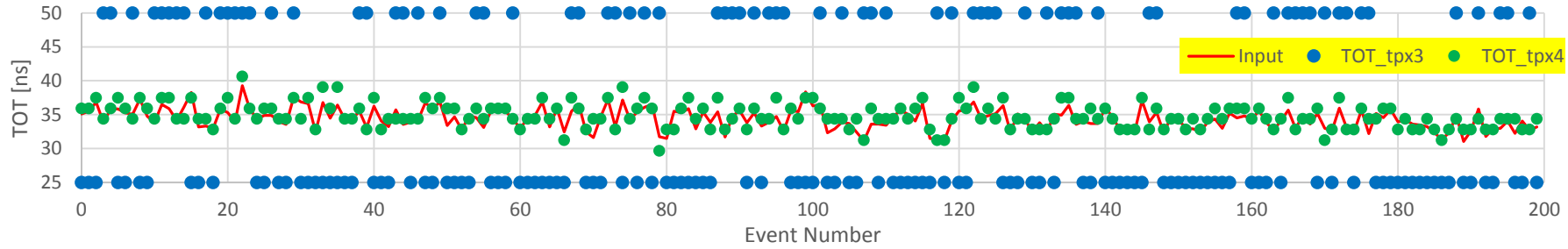
- Threshold set at 500 e^- and FE with ENC 60 e^-_{rms}

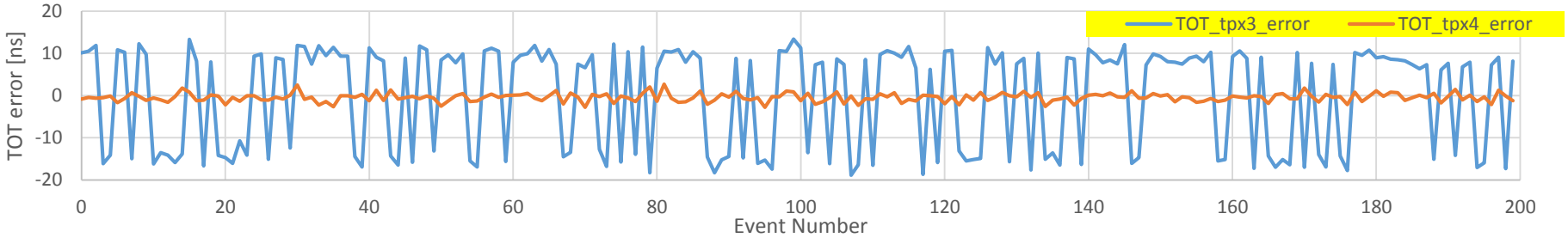




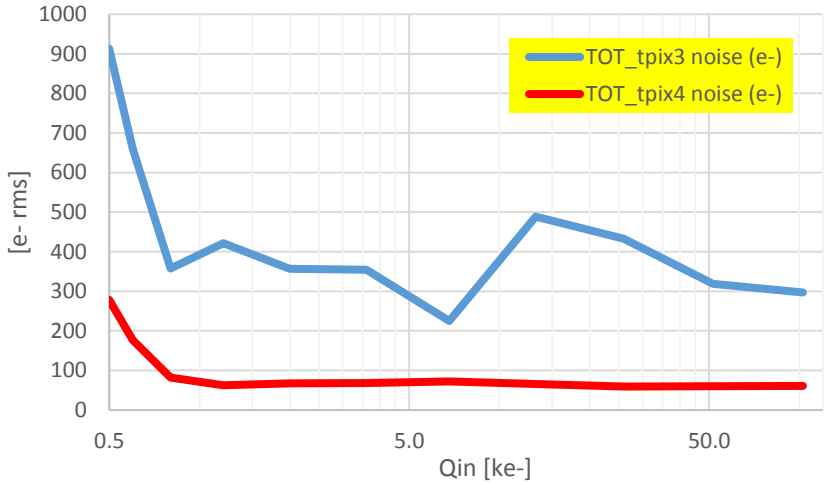
On-pixel TDC simulations → TOT resolution

- Qin =1 .2 Ke$^-$, RZ=25ns/ Ke$^-$ and FE with ENC 60 e$^-_{rms}$



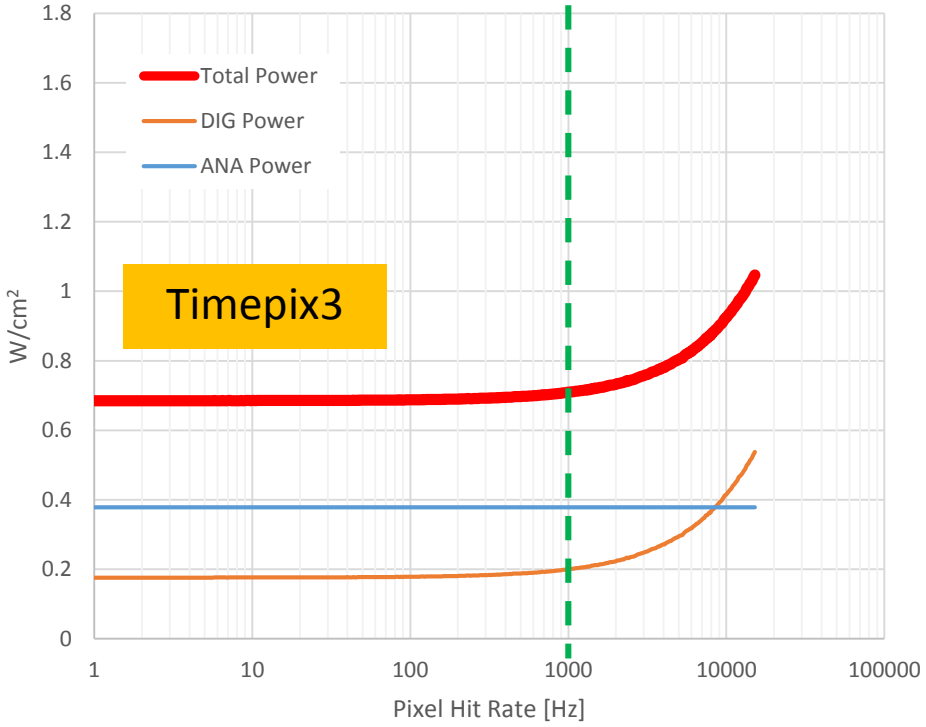


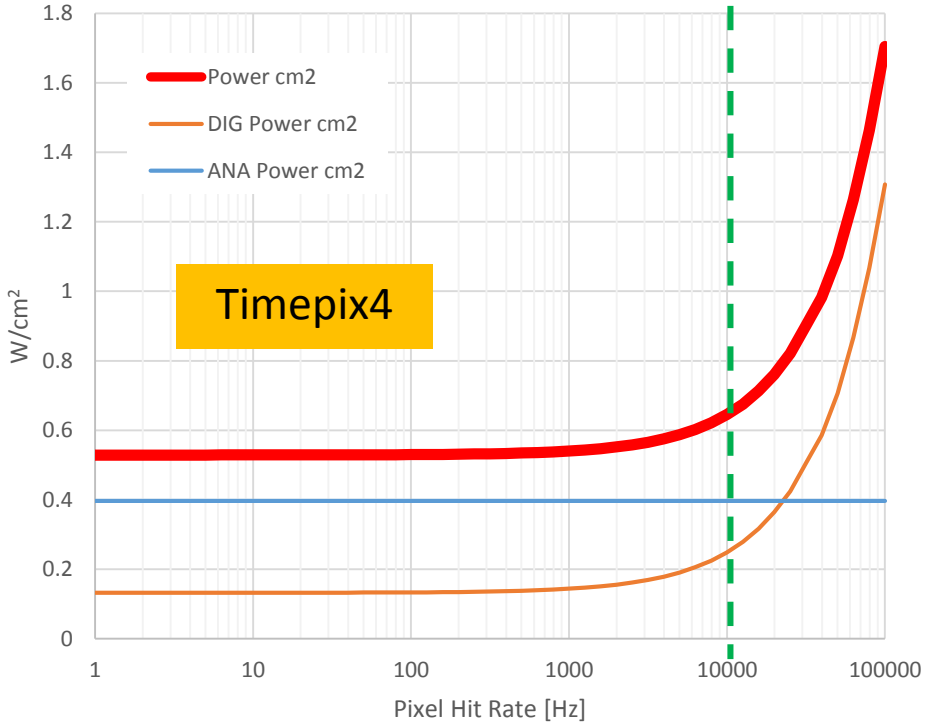
- Timepix4 TOT measurement dominated by ENC and not by sampling error:
- **~700 e$^-$ FWHM** in Si Sensor @ENC 60 e$^-_{rms}$



Digital (dynamic) Power Consumption [data-driven]

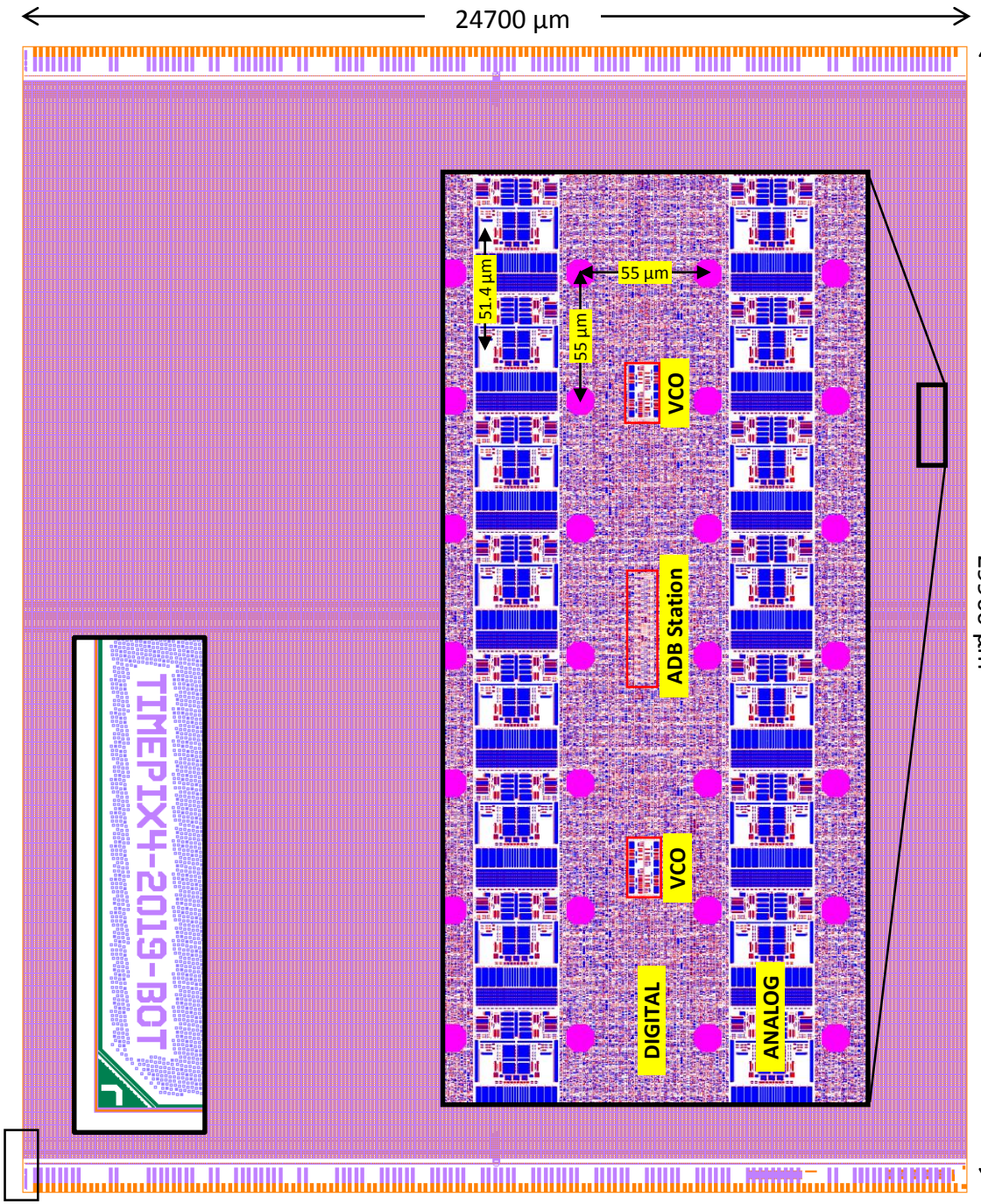
- Simulated power consumption density to be ~20 % less of Timepix3:
  - Digital power consumption 25% less
    - Improved pixel matrix clock distribution (DDLL)
    - 130nm → 65nm
  - Analog consumption is ~5% more
    - Minimize jitter → < $50ps_{rms}$
    - Compensate increase in input capacitance

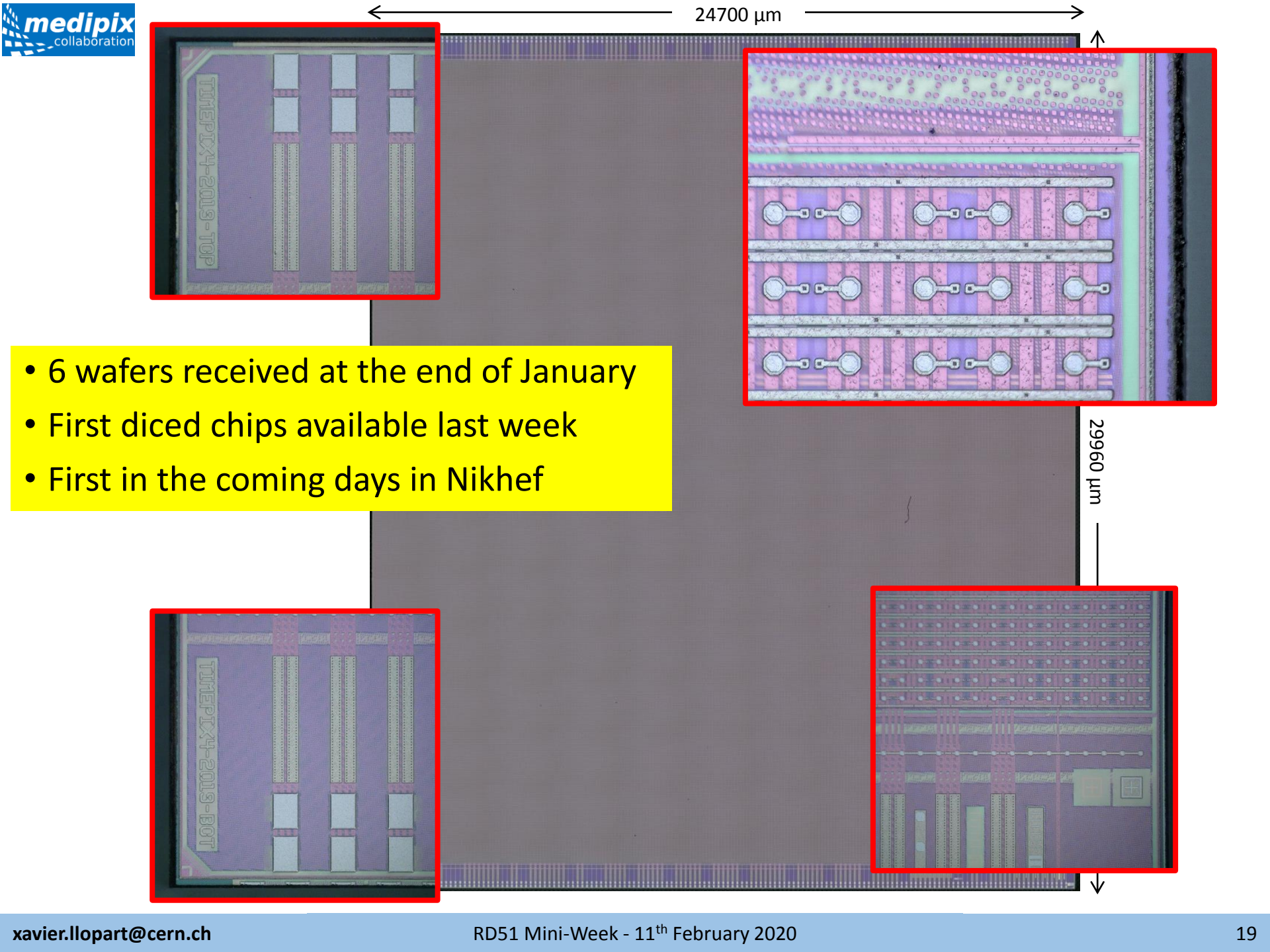




Timepix4 (2019)

Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
APLL	19
ADLL	16
10 Gbps serializers	16
On-pixel VCO	28672
dDLL Columns	448
Biasing DACs	13
ADC	1
Transistors in pixel	~6000
Transistors in chip	~1.5 bn





- 6 wafers received at the end of January
- First diced chips available last week
- First in the coming days in Nikhef

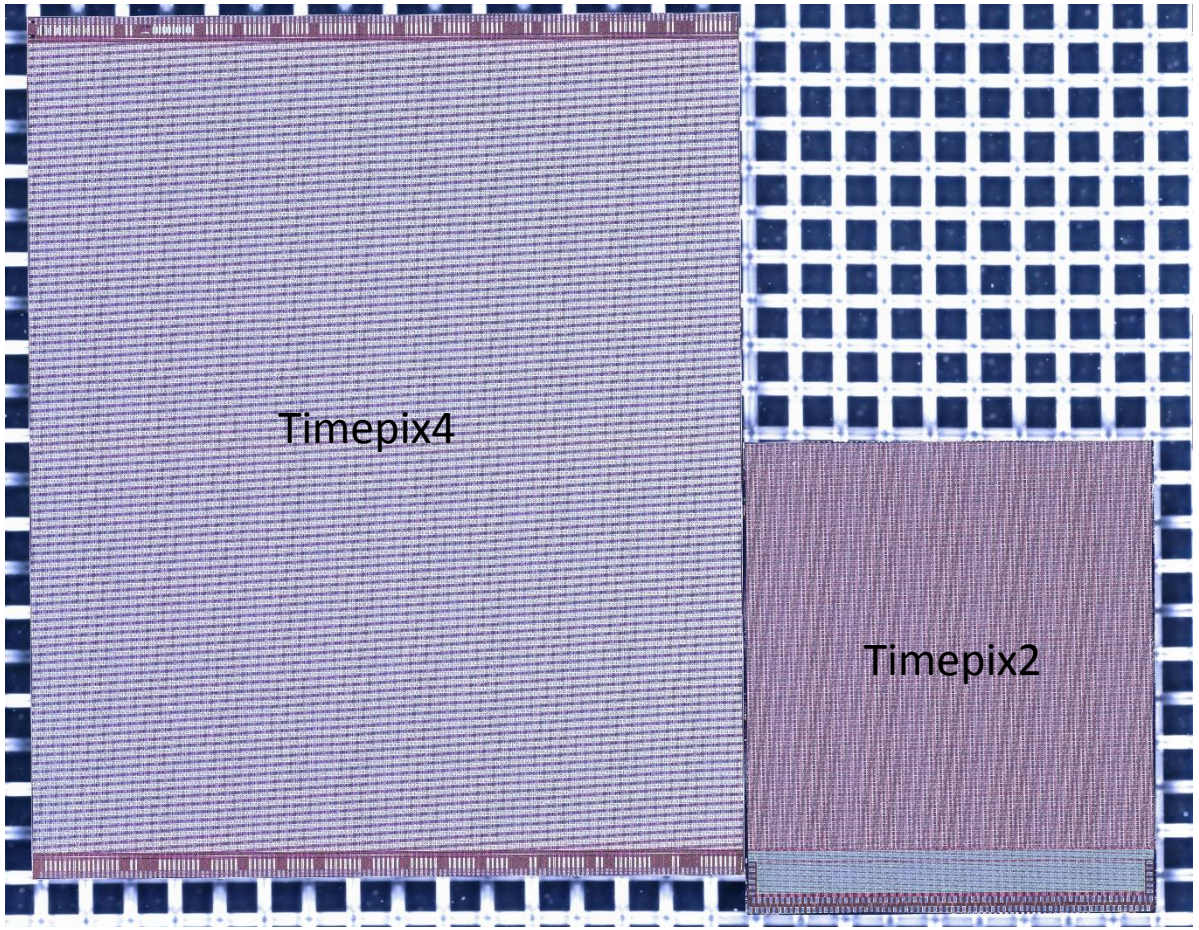
Conclusions

- Timepix4 is the new particle-tracker and photon counting hybrid pixel detector designed with the support of the Medipix4 collaboration:
  - Large area hybrid pixel detector with **6.93 cm^2** sensitive area
  - 4-side buttable with **<0.5% dead area** (not sensitive)
  - TOA: **23-bit dynamic range (1.6ms) with 195 ps LSB**
  - TOT: **15-bit dynamic range with 60-100 e- LSB**
  - PC: **8-bit or 16-bit CRW up to 8*10^9 hits/mm^2/s**
  - **Very configurable architecture** to accommodate a large number of different applications

- Total design time of ~3 years with 9 engineers → ~13 year FTE

- Timepix4 was submitted to fabrication on the 7th of November
- First tests in the coming days @ Nikhef

Thank you !

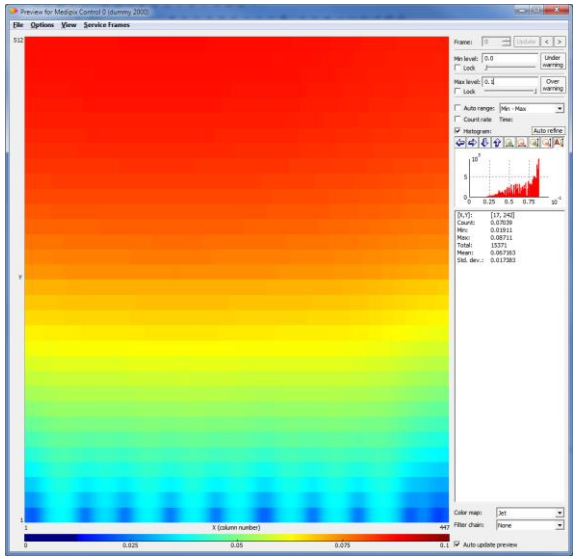


- More detailed information in: https://indico.cern.ch/event/788037/
- http://medipix.web.cern.ch/

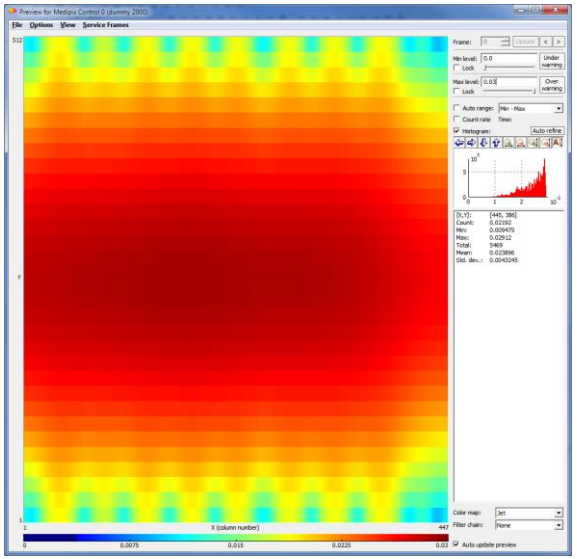
SPARE

Analog (static) power supply distribution

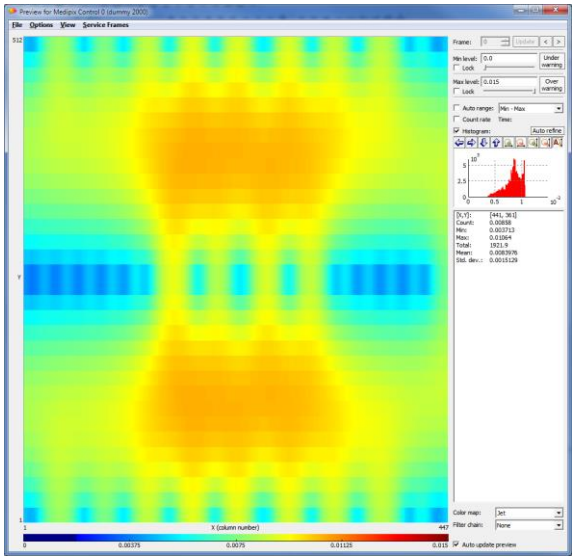
	Total I (chip)		1 WB	2 WB	3 TSV
Nominal Analog Power [10 µA/pixel]	**~2300 mA**	V_{drop} [max-min]	**68 mV**	**19.6 mV**	**6.9 mV**
		Imax pad	**118 mA**	**60 mA**	**57 mA**
Low Analog Power [1 µA/pixel]	**~230 mA**	V_{drop} [max-min]	**6.8 mV**	**1.96mV**	**0.69mV**
		Imax pad	**11.8 mA**	**6 mA**	**5.7 mA**



1 WB



2 WB



3 TSV