Studies on the Rate-Capability of the VMM3a within the SRS

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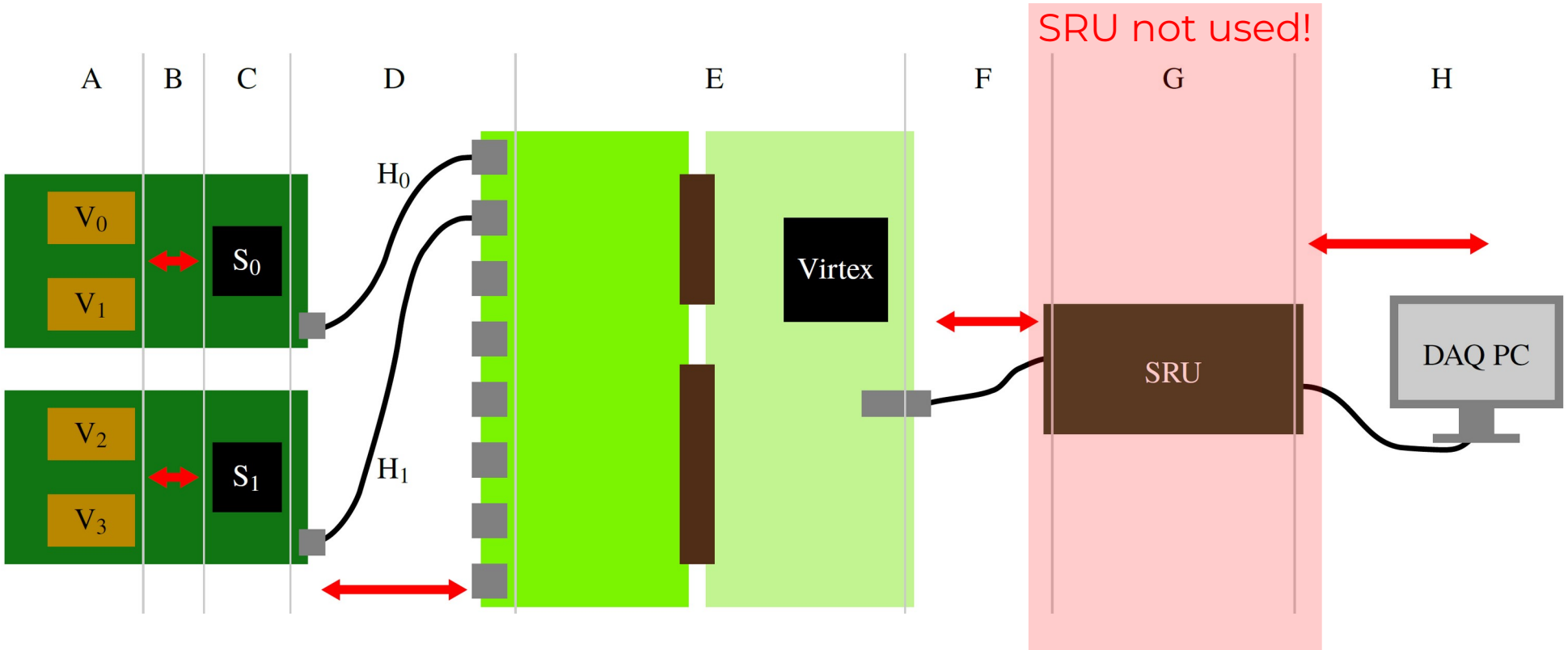
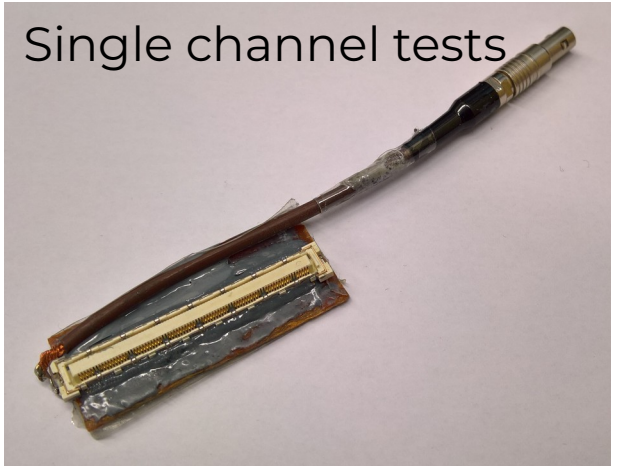
VMM3a within the SRS

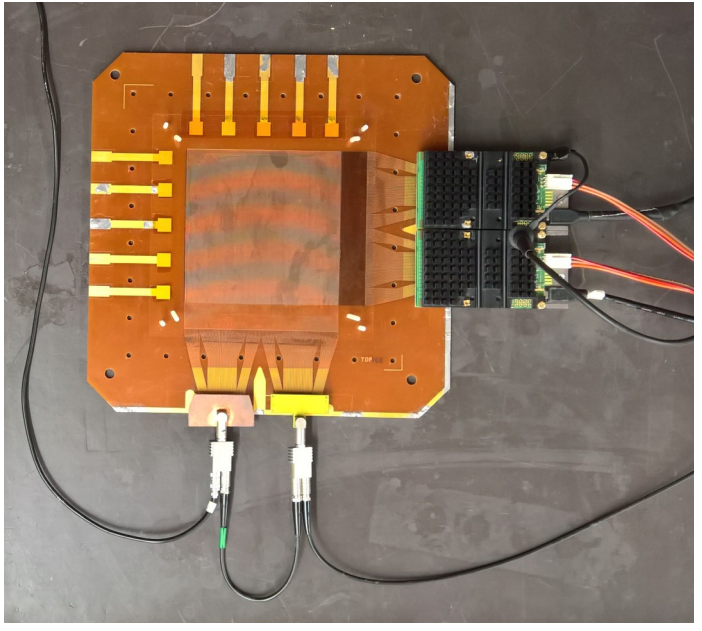


Test Set-Up

- External pulse/waveform generator → periodic, but controlled situation
- 25 ns peak time
- 40 MHz BC clock
- 80 MHz dual edge readout clock → more possible, but not yet stable
- Analysis of data rate at network and digital data



Pulses send to HRS connector directly pluged to hybrid

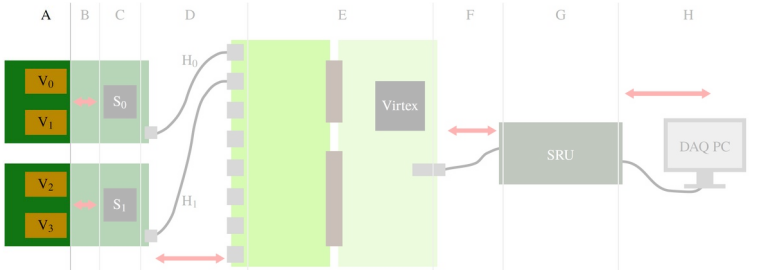


Multi channel + hybrid tests:

Pulses on x strips of readout board → capacitive coupling between x and y strips, read out y strips

A: VMM-Level, Single Channel

Pulse single channel of VMM → where is the limit

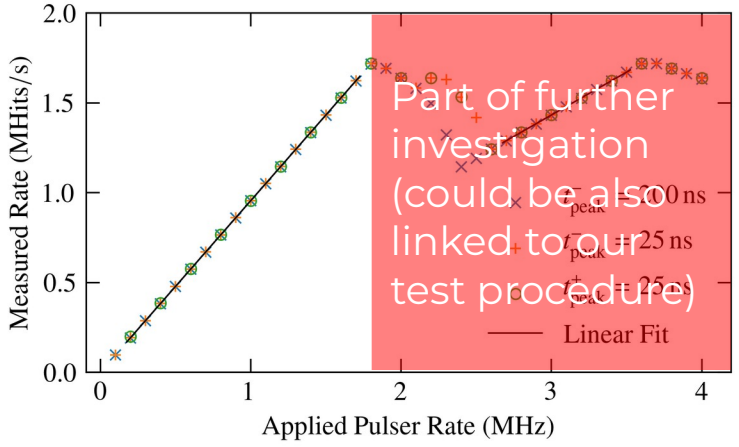


Expected:

- In continuous read/write mode: **4 MHits/s per channel**
- 6-bit ADC: even faster
- 40-bit per hit → **160 Mbps per channel**

Measured:

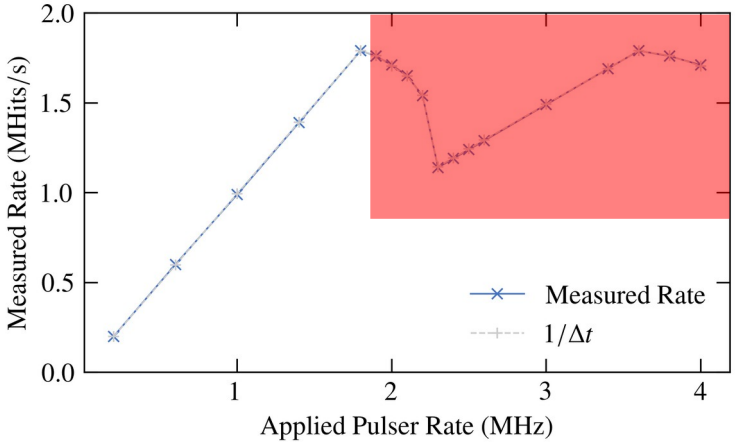
- Linear 1:1 relation up to **1.8 MHits/s per channel** → **72 Mbps per channel**
- Higher rates are part of further investigation



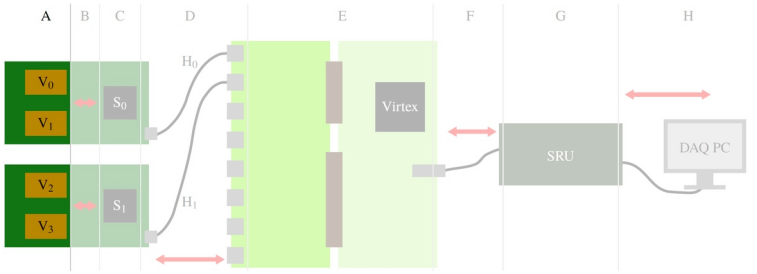
Network rate

and digital data

are compatible



A: VMM-Level, Multi Channel



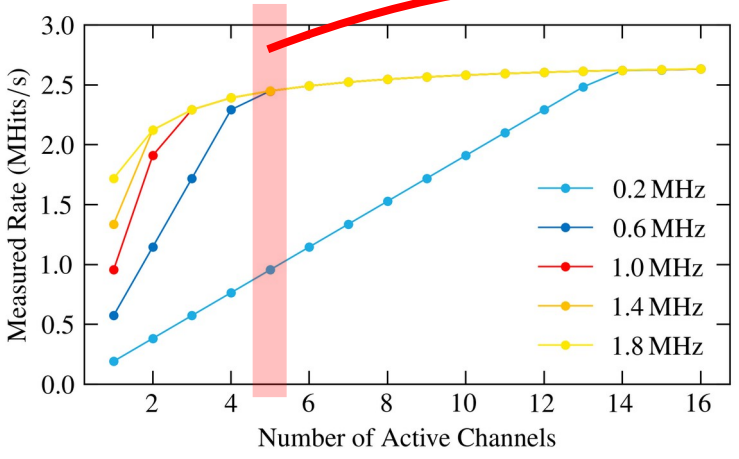
Increase number of pulsed channels @ different frequencies

Expected:

- Max. 160 MHz readout clock
- 2 Data lines per channel
- Dual edge readout
- **Max. 640 Mbps = 16 MHits/s output**

Measured:

- Saturation observed at **108 Mbps = 2.7 Mhits/s** (although 320 Mbps = 8 Mhits/s expected with our settings)



What does this mean detector-wise?

ASSUMPTION:

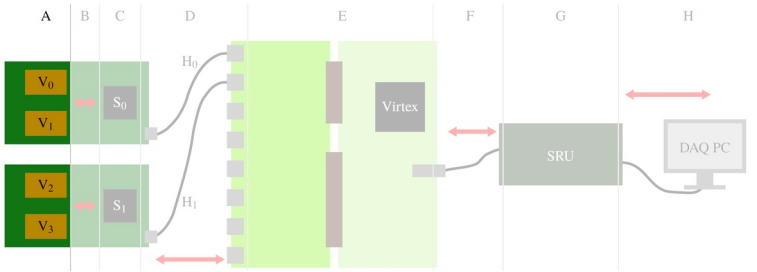
- 10 x 10 cm² COMPASS-like triple-GEM detector
- x-ray interactions
- mean cluster size: 5 strips (with neighbouring logic enabled)

1 VMM covers 2.5 cm

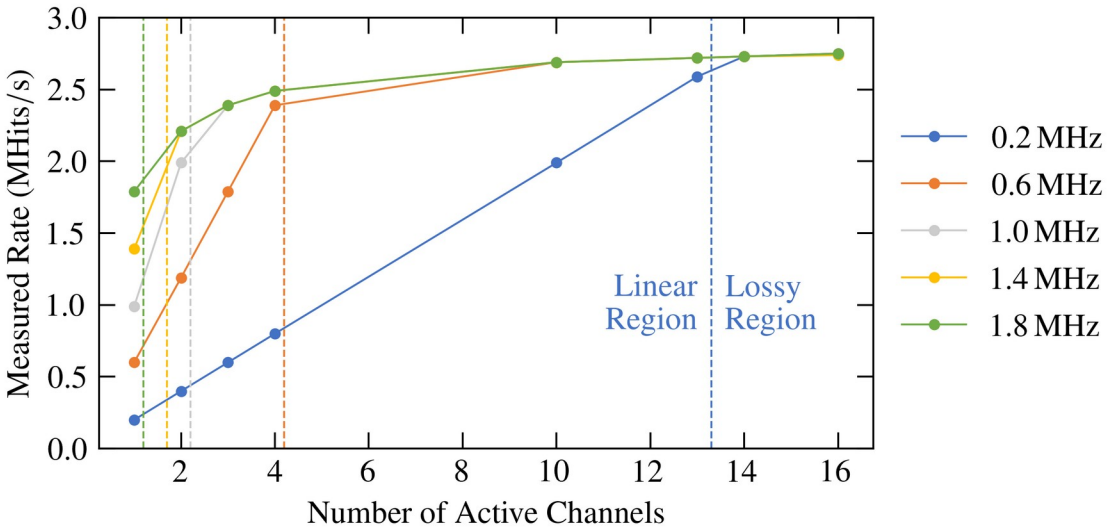
Rate @5 channels should be < 500 kHz

→ **200 kHz/cm**

A: Multi Channel Stability

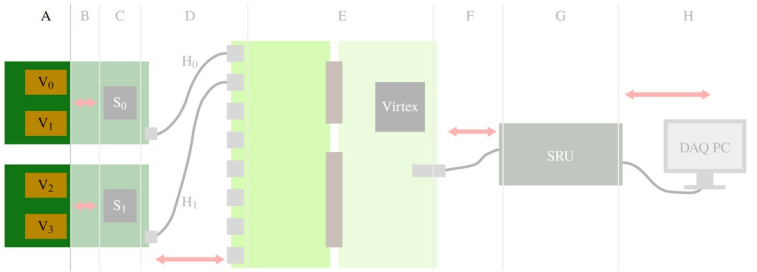


Study the digital data
→ output rate depending on input frequency and active channels

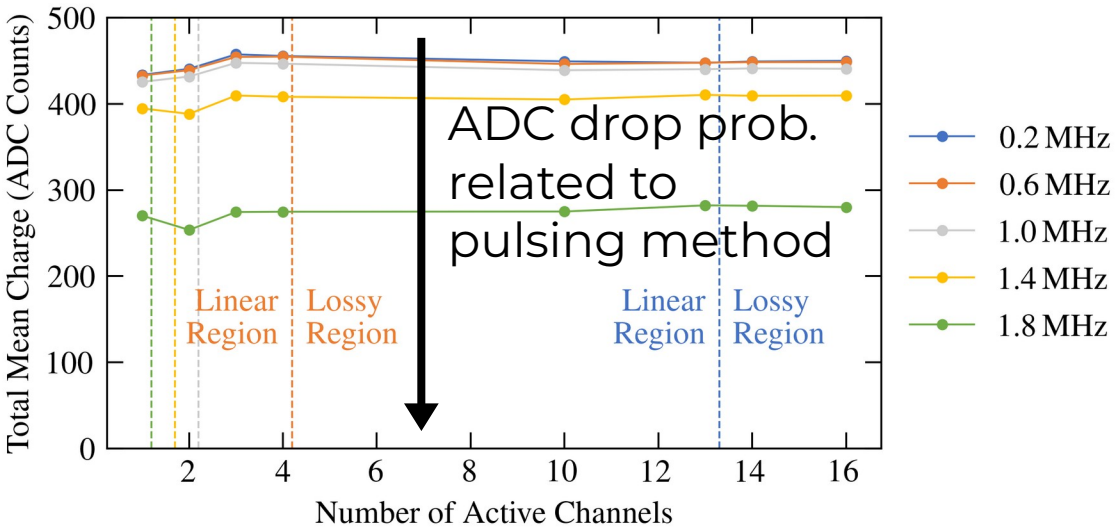


- All channels are pulsed with the same frequency
- Channels have always equal number of hits in linear region (left of dotted line) and in lossy region (right of the dotted lines)
- Losses are thus equally distributed over all channels

A: Multi Channel Stability

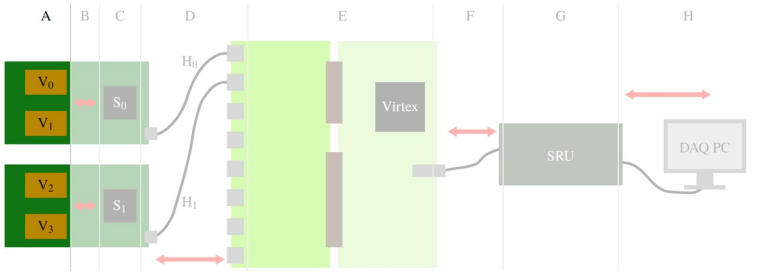


Study the digital data
→ ADC values depending on input frequency and active channels

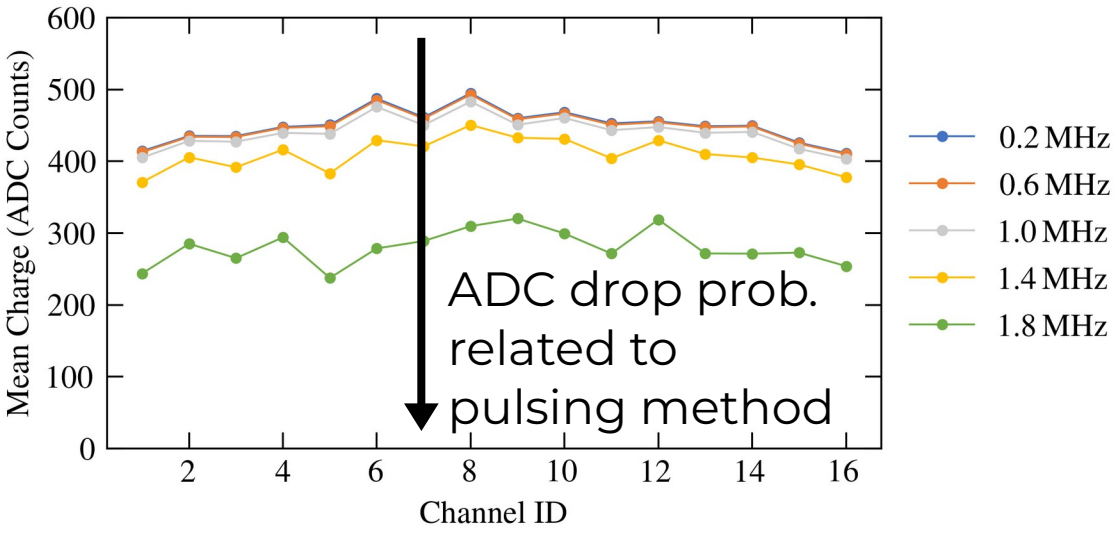


- For all data series, the linear region is left of the dotted line
- The lossy region is right of the dotted line
- Basically no relation between data losses and reduction of detected charge (detected charge stays stable from left to right)

A: Multi Channel Stability

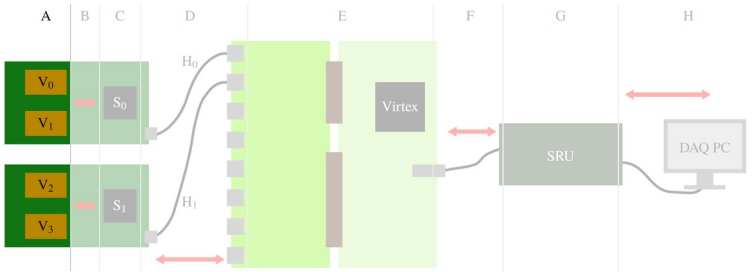


Study the digital data
→ Mean channel ADC values depending on input frequency and active channels

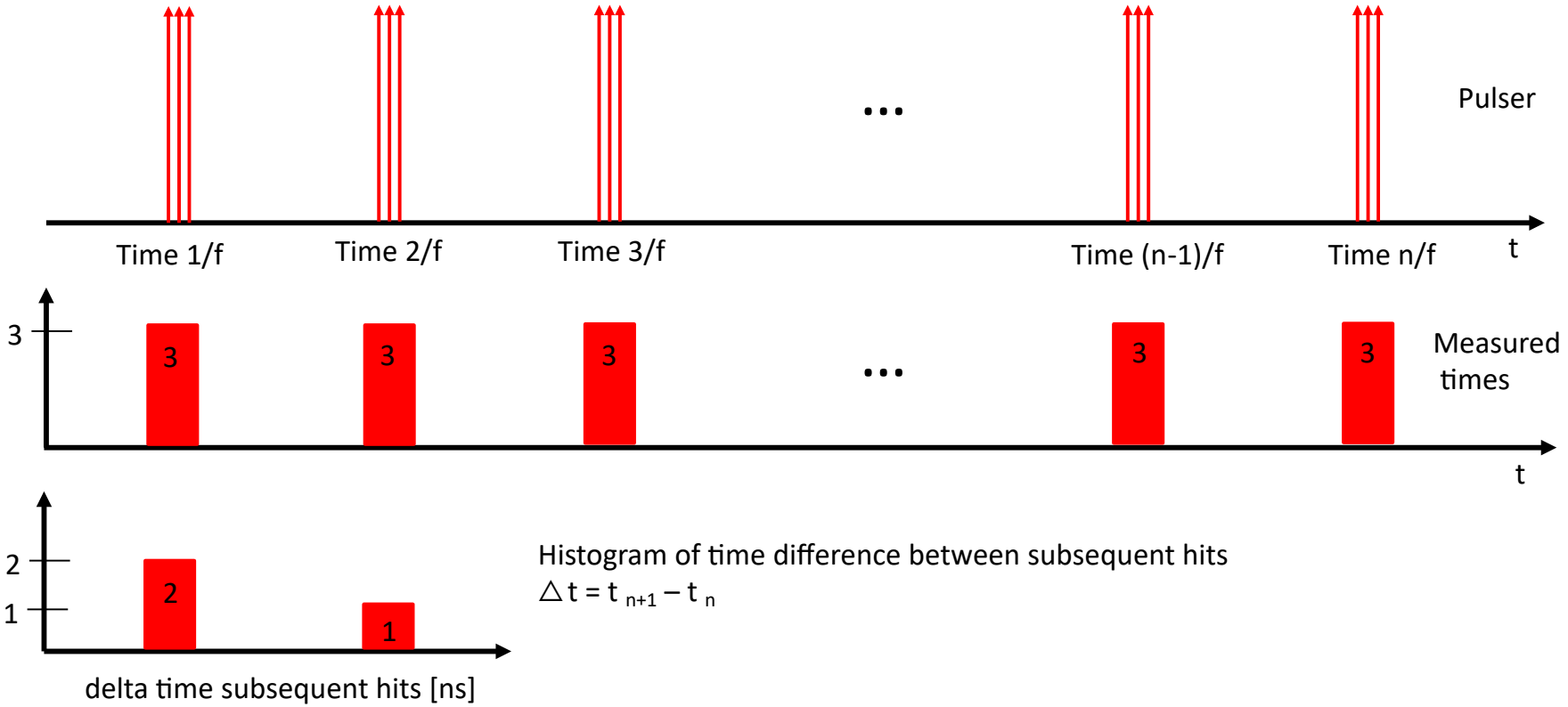


- 16 channels pulsed (equally spaced between channel 0 and 63)
- Typical inverse U-shape of charge distribution
- Shape is clearly preserved

A: Multi Channel Stability



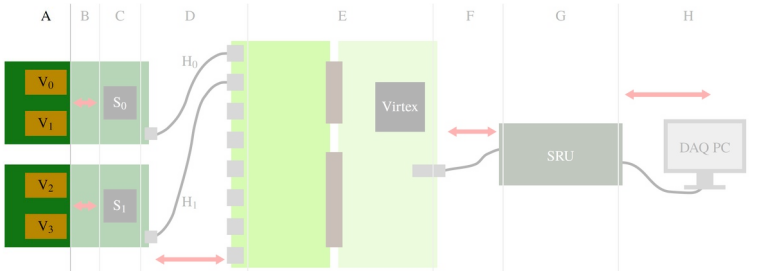
Pulsing scheme for multiple channels



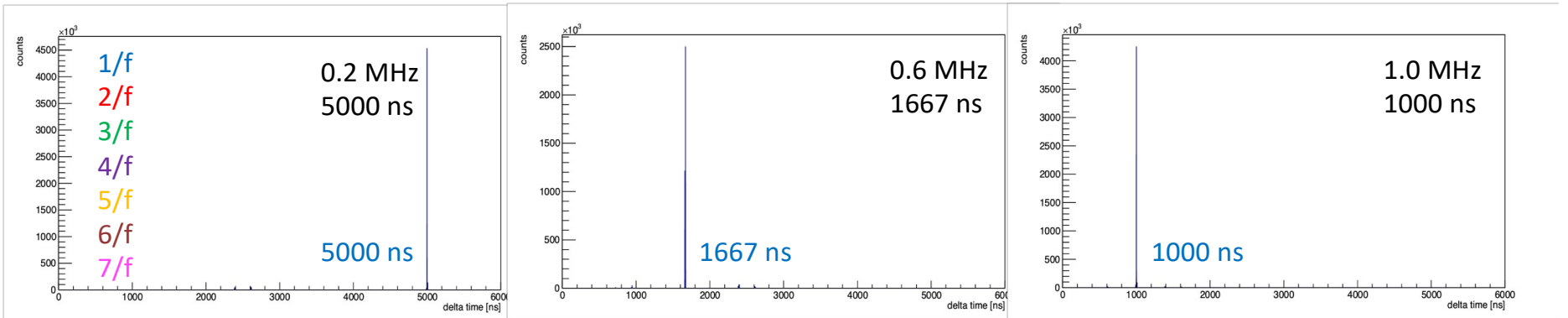
Histogram of time difference between subsequent hits

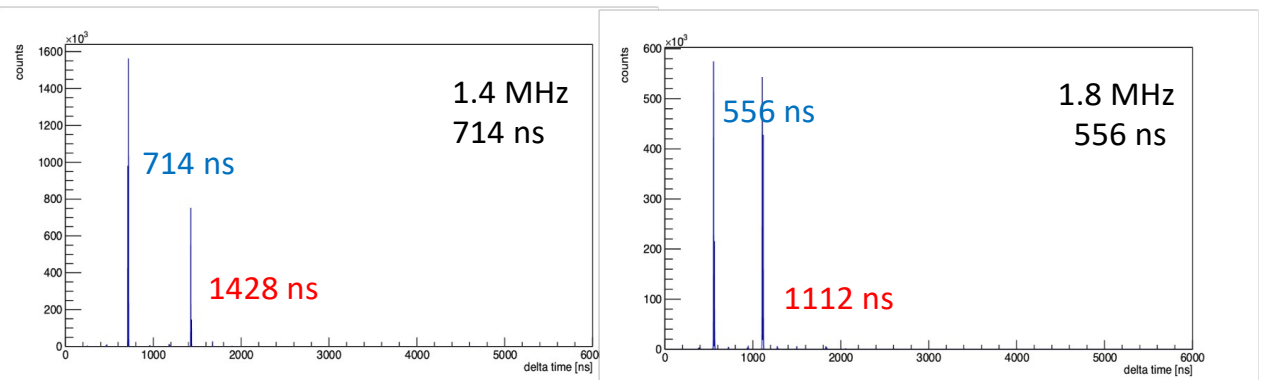
$\triangle t = t_{n+1} - t_n$

A: Multi Channel Stability

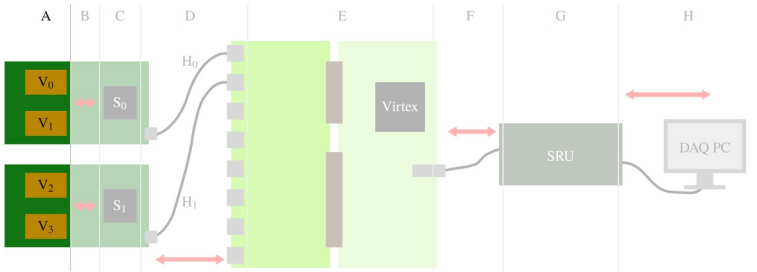


2 channels pulsed, channel 10, time difference

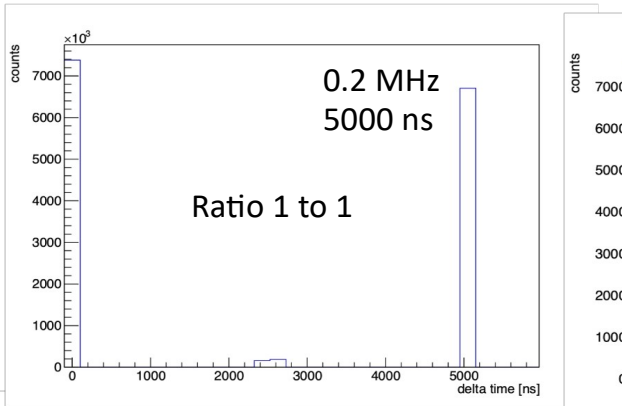


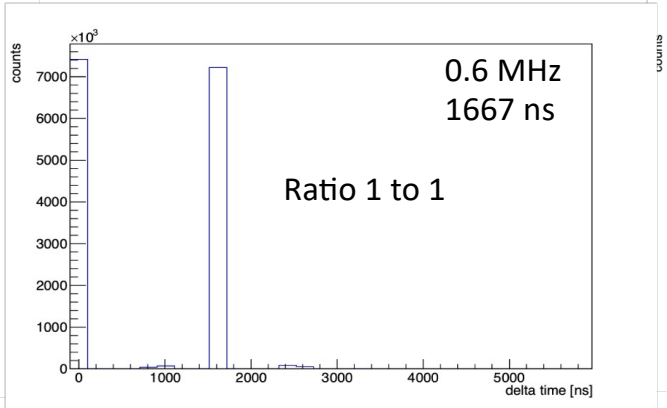


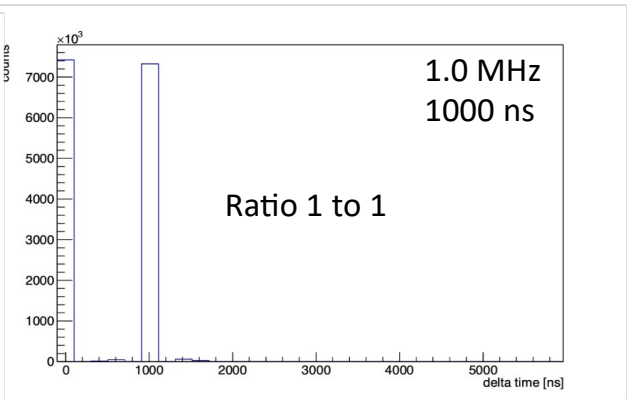
A: Multi Channel Stability

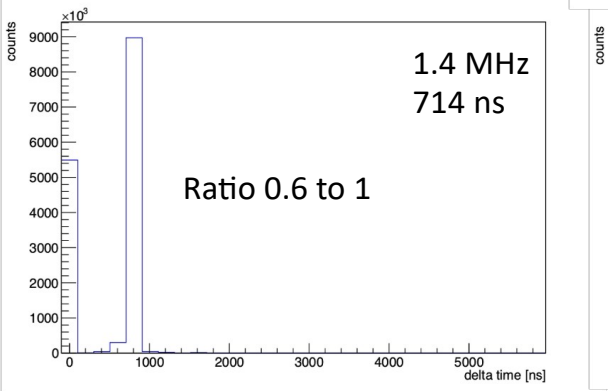


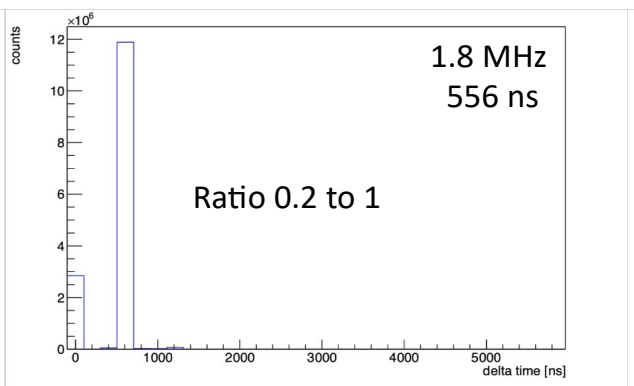
2 channels pulsed, time difference

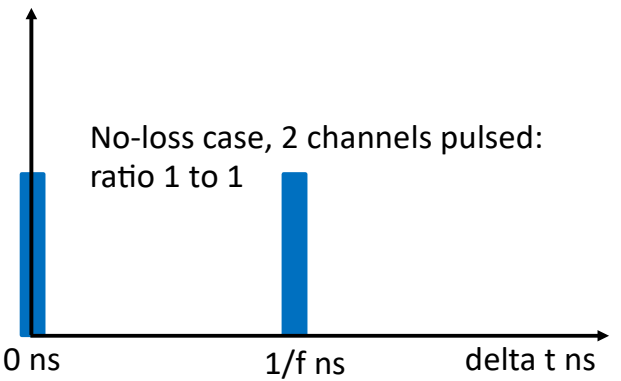




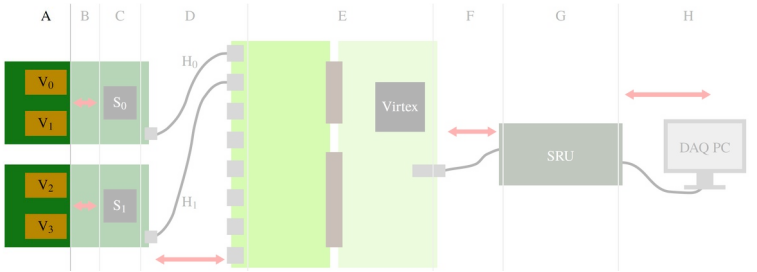




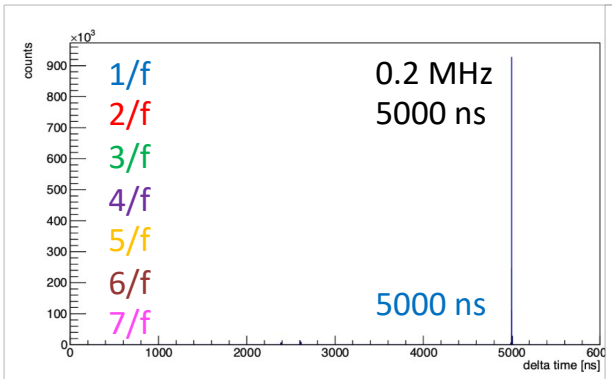


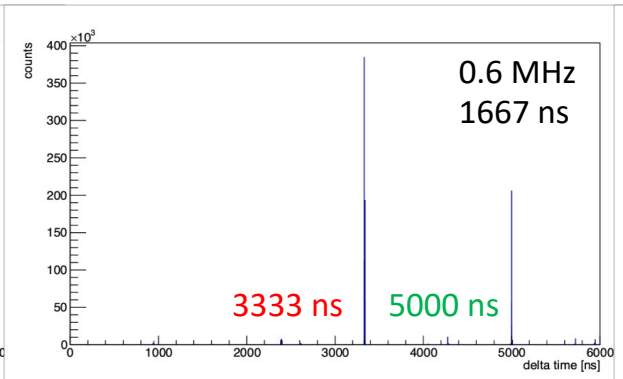


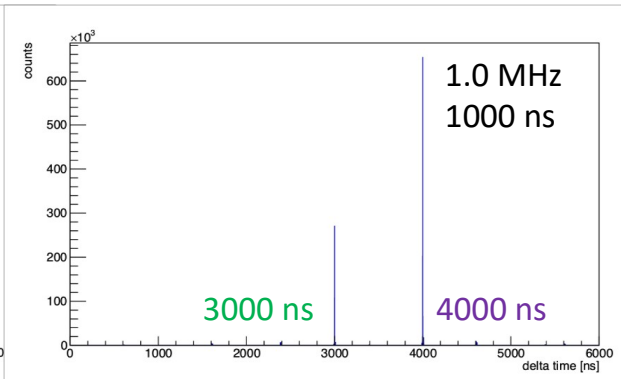
A: Multi Channel Stability

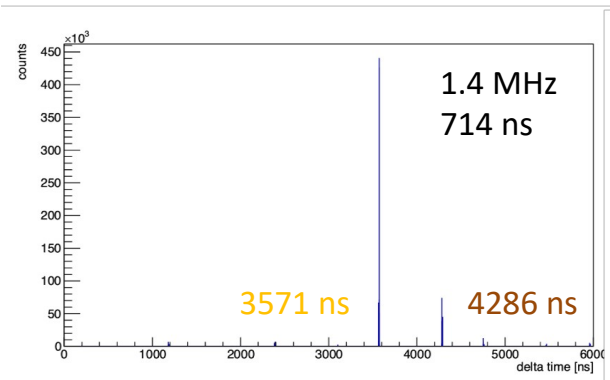


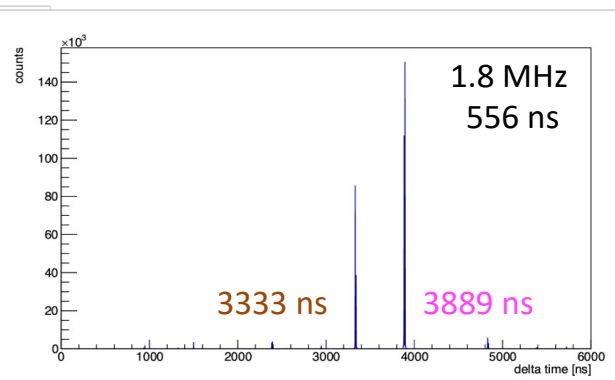
10 channels pulsed, channel 20, time difference



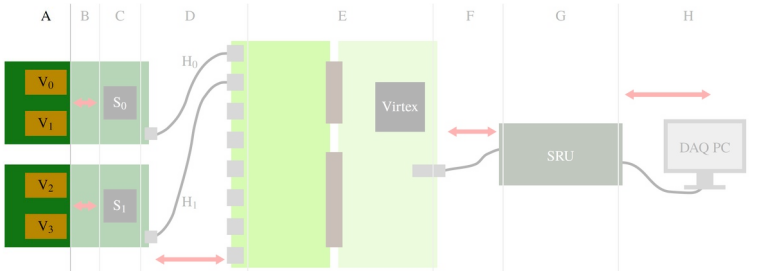




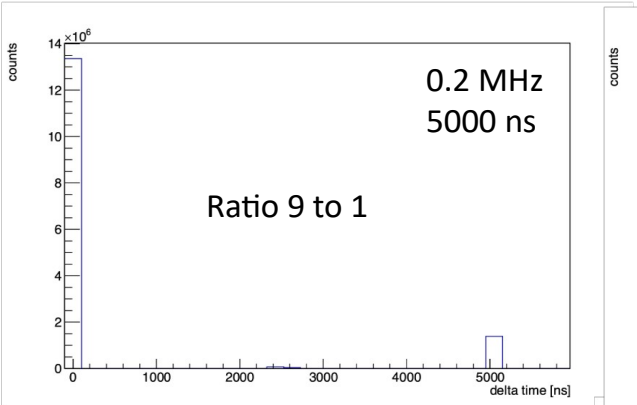


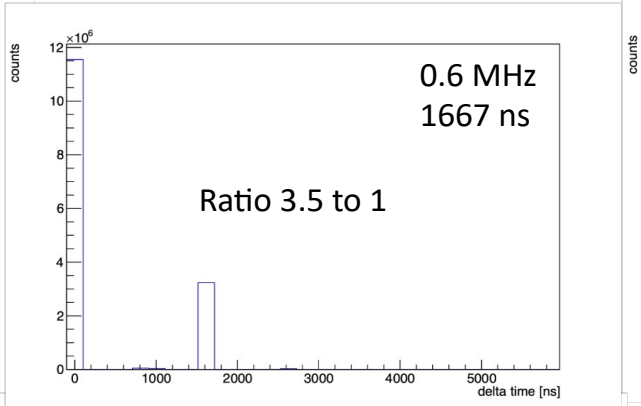


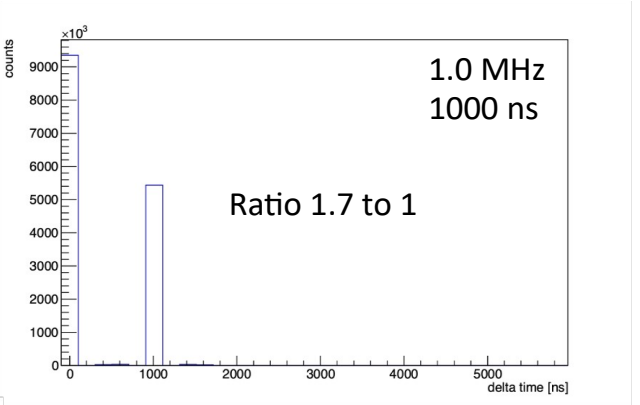
A: Multi Channel Stability

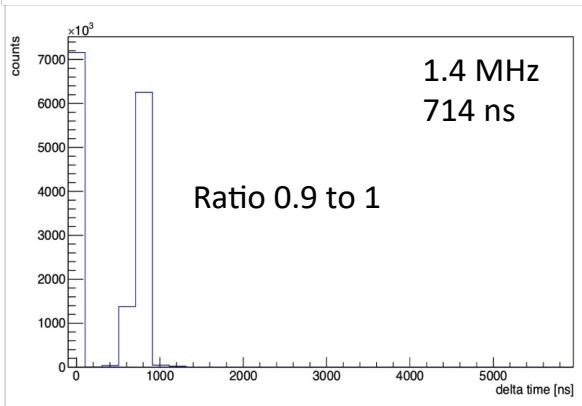


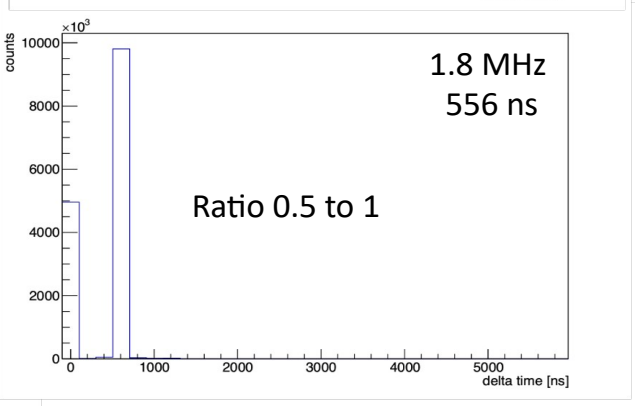
10 channels pulsed, time difference

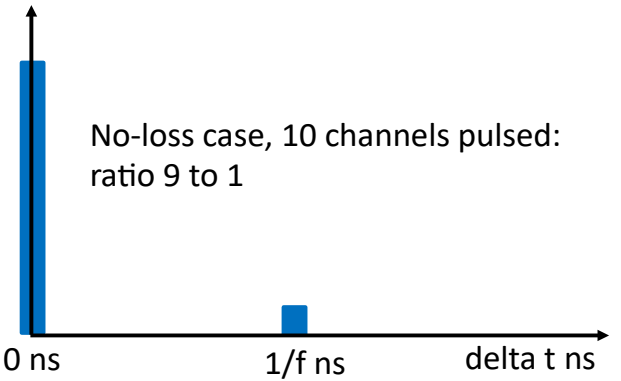




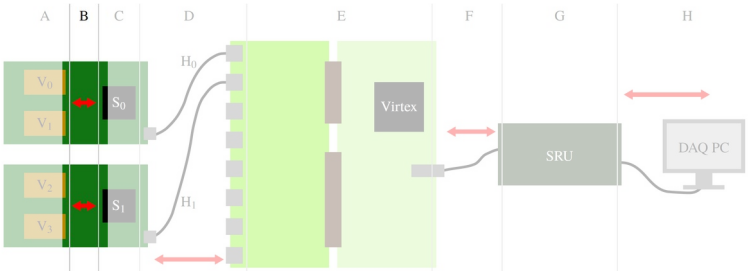








B: Readout Speed

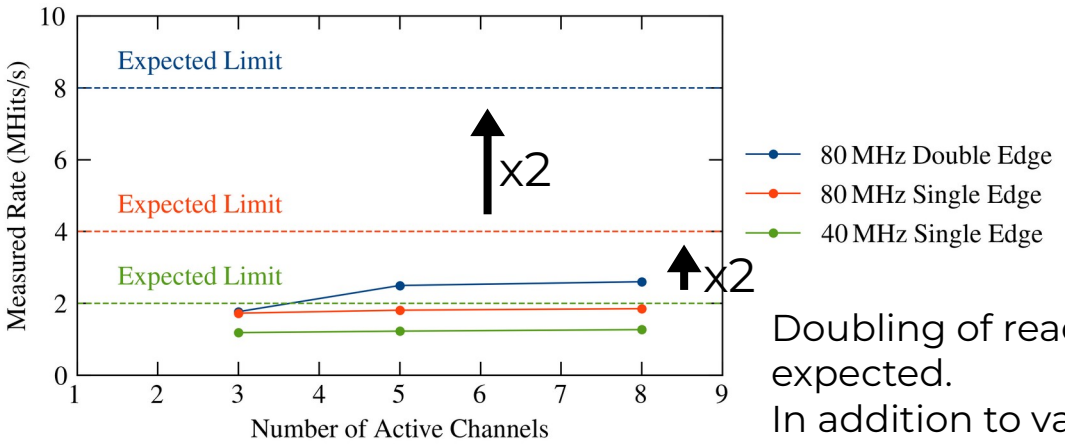


Expected:

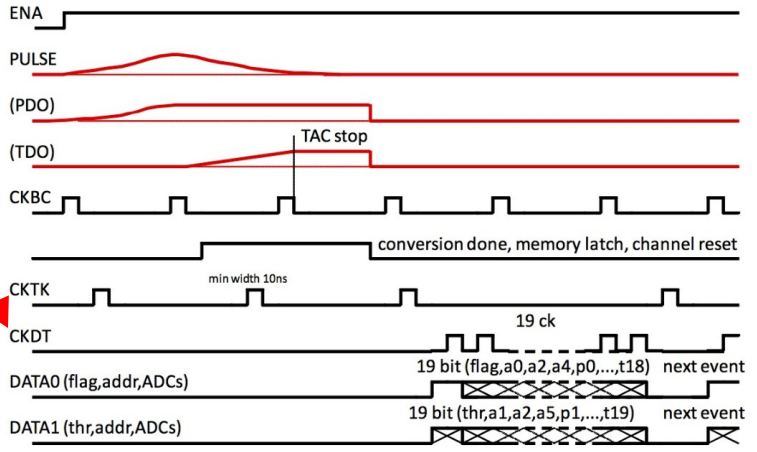
- Max. 160 MHz readout clock
- 2 Data lines per channel
- Dual edge readout
- **Max. 640 Mbps = 16 MHits/s output**

Measured:

- Stable operation only up to 80 MHz dual edge clock possible, so **max. 320 Mbps = 8 MHits/s output**
- **Team in Bonn is working on this**

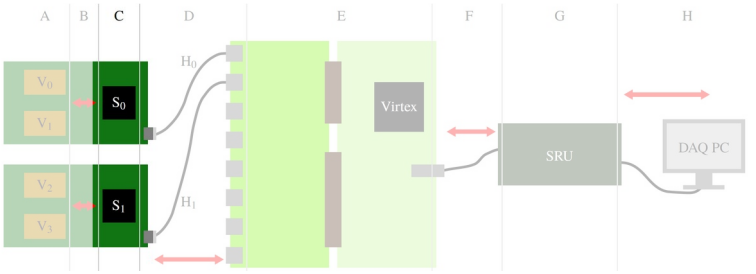


Doubling of readout rates expected.
In addition to variable CKDT fixed CKTK @ 40 MHz



[VMM3a Manual]

C: Spartan®-6 FPGA

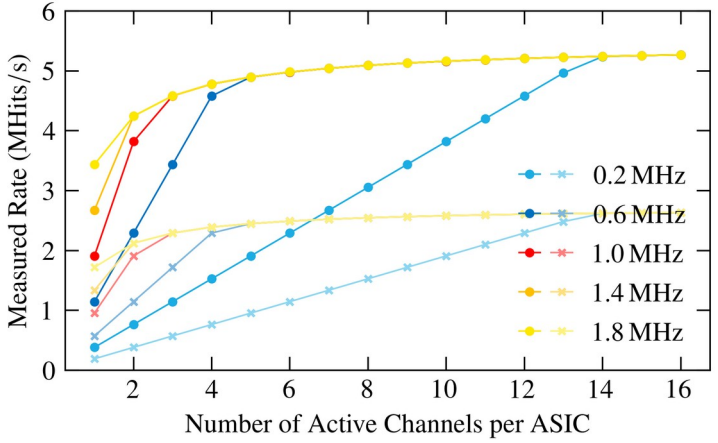


Expected:

- Max. output rate:
  950 Mbps = 23.75 MHits/s

Measured:

- Data rate from 1 to 2 VMMs doubles
- **216 Mpbs = 5.4 MHits/s**



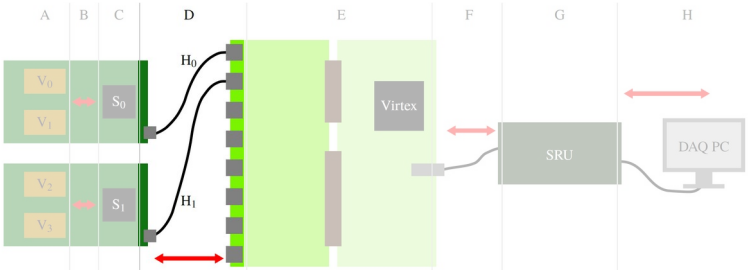
1 VMM

2 VMMs

Data rate scales by a factor of 2

Data losses are symmetrically distributed

D: HDMI Cable



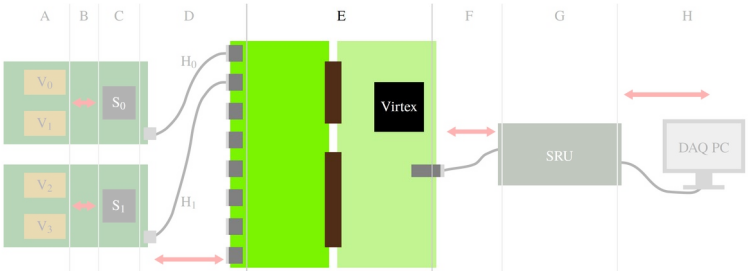
Expected:

- ~ 1 Gbps is no problem

Measured:

- Everything worked fine

E: D-Card/FEC, Virtex®-6

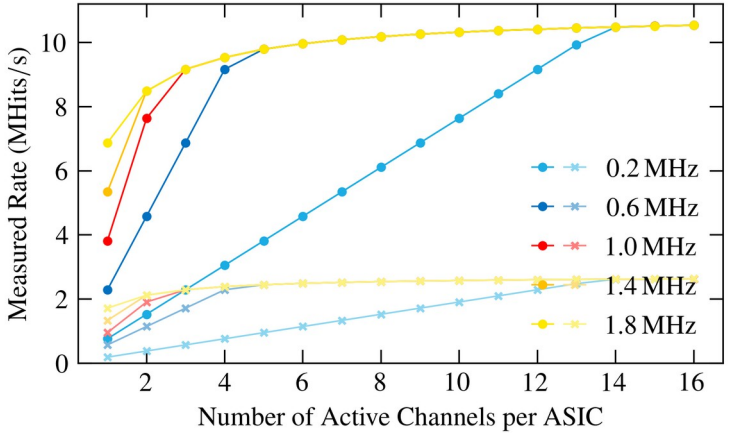


Expected:

- Virtex®-6 is powerful enough
- > 1 Gbps rates are no problem

Measured:

- Everything worked fine
- With 2 hybrids, so 4 VMMs:
  432 Mbps = 10.8 MHits/s



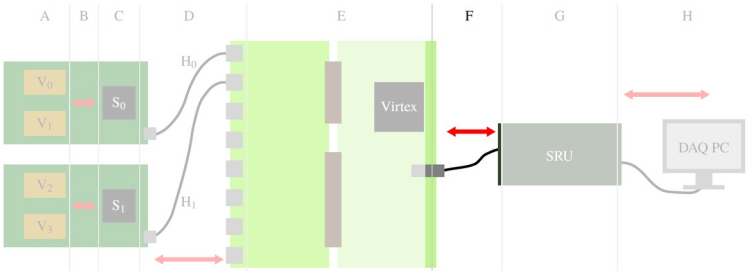
1 VMM

4 VMMs

Data rate scales by a factor of 4

Data losses are symmetrically distributed

F: Ethernet Cable



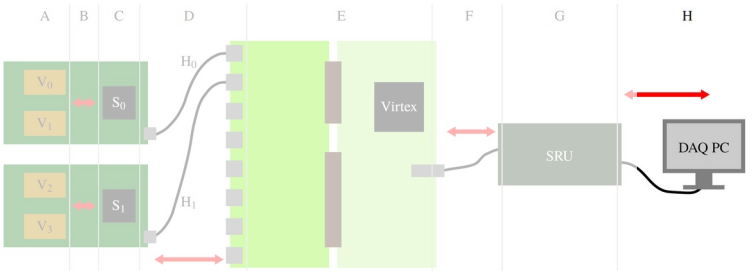
Expected:

- 1 Gbps

Measured:

- With 2 hybrids, so 4 VMMs: saturation at **432 Mbps = 10.8 Mhits/s**
- At FEC level: 40-bit hit → 48-bit hit → **518 Mbps**
- For 4 hybrids, so a 10 x 10 cm², so a COMPASS-like triple-GEM detector, this may be a problem!
  → **2 x 518 Mbps > 1 Gbps**

H: DAQ Computer



Expected:

- 10 Gbps network card

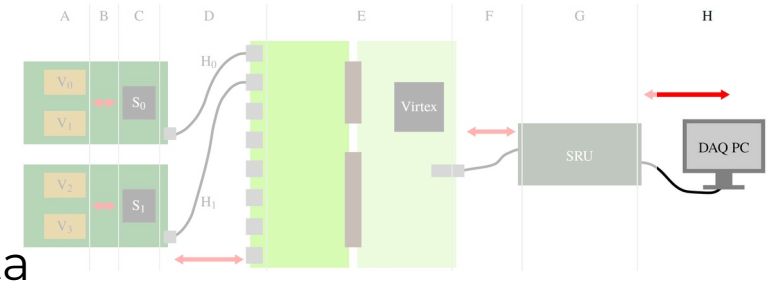
Measured:

- No problems with network card

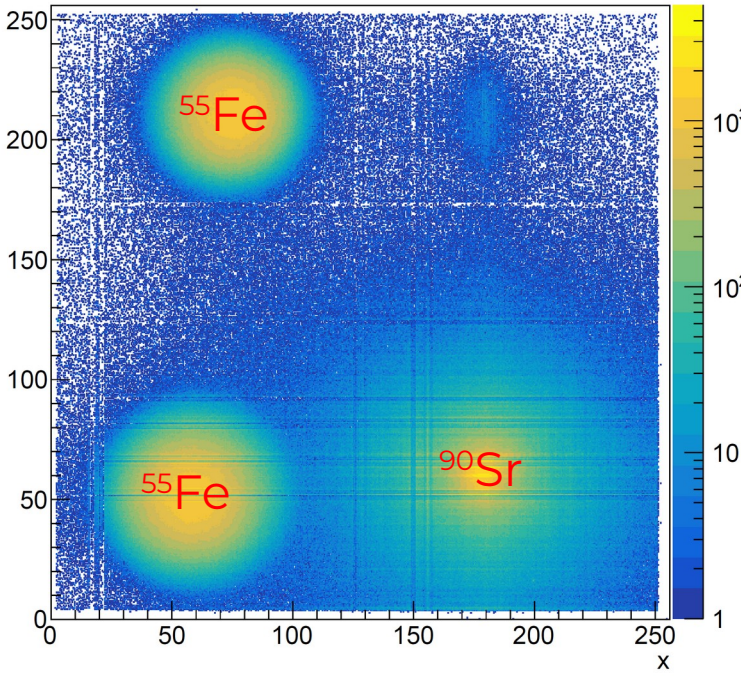
- Use ESS DAQ for monitoring
  (esp. Event Formation Unit & DAQuiri)
  → https://github.com/ess-dmsc/essdaq
- Use Wireshark/tcpdump for writing the data to disk

- We were able to take data at 110 kHz and we want to go higher

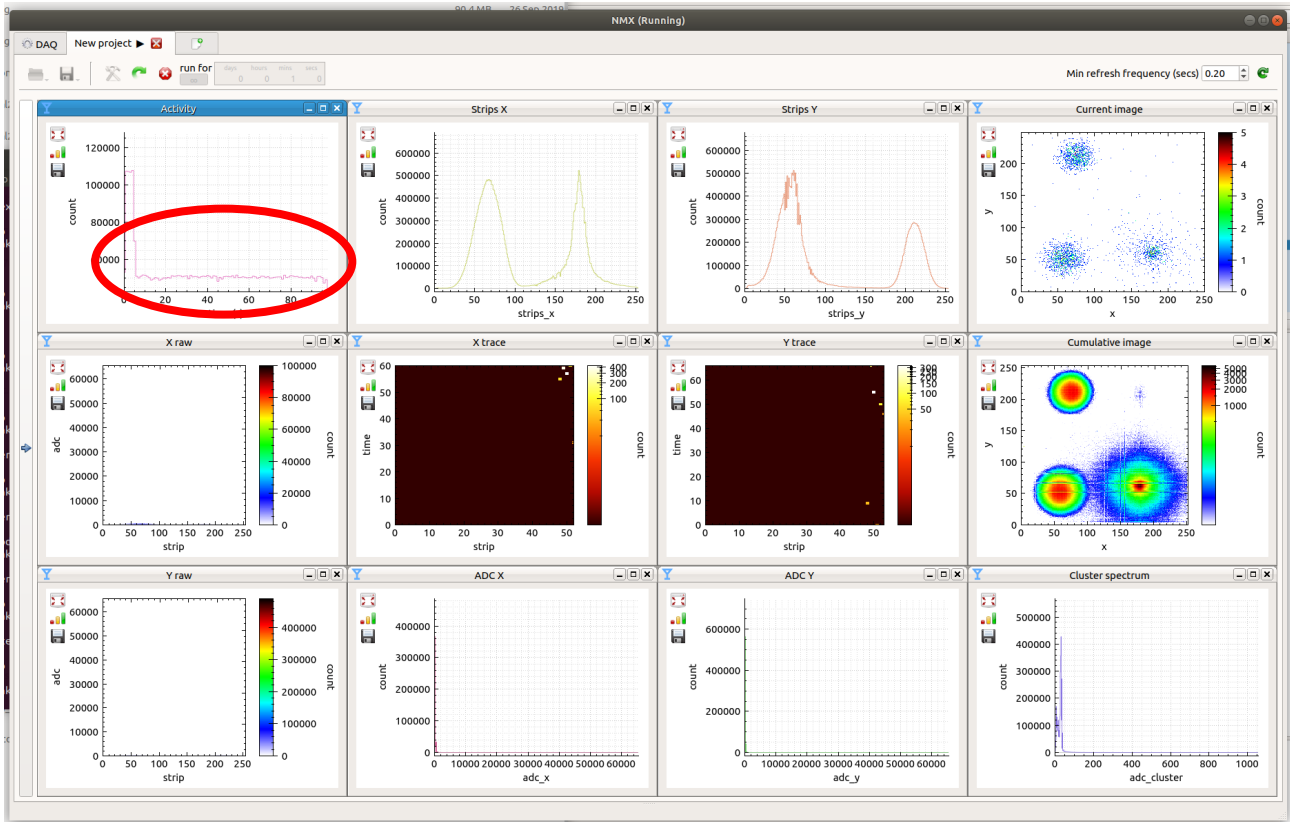
H: New DAQ Concept



Offline reconstructed data

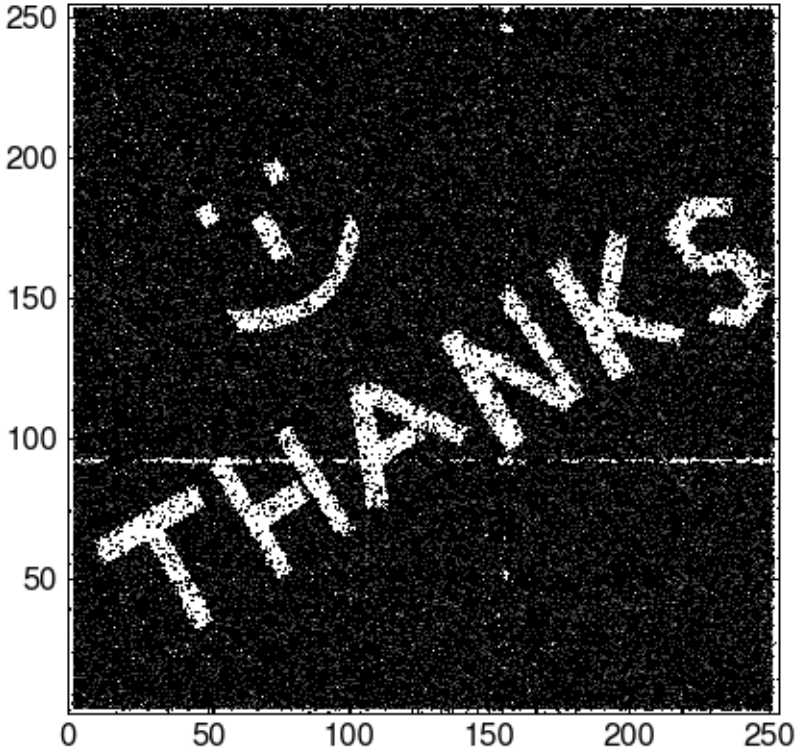


Online monitored data



Summary

- Readout clock for VMM seems to be the only bottleneck of the system in the current status
- Nevertheless, readout seems to be fair. Effects on the data rate are obseverd, but no effects on the data quality.
- Other SRS components work as they should and are well suited for high data rates (keep eye on 1 Gbps link from FEC to DAQ PC in the future)
- **Several options for improving the rate capability can be (easily) done:**
  - Usage of 160 MHz dual edge readout clock
  - Spartan®-6 speed grade 3 instead of 2 (faster FPGA, but no change of hybrid PCB needed)
  - For speed grade 3: use 2 instead of 1 HDMI lines



for your Attention