VMM hybrid firmware development

Marek Hracek
RD51 Mini-Week
About me

• Czech Republic

• Microelectronics at Brno University of Technology

• Part of GDD as associate member from Institute of Experimental and Applied Physics (Czech University of Technology)
VMM hybrid board

Note: translucent Globtop only on prototypes
VMM3a hybrid block diagram

From detector

64 channels

J1

64 channels

U2
VMM3a
VMM-1, ch0-63

U3
VMM3a
VMM-2, ch64-127

ADC
I2C

ADC
I2C

U1
Spartan FPGA

ADC
I2C

U9 (Flash)
AT45DB161E

ID chip EEprom

J10

J4

J3

J2

HDMI-D (micro)

DTCC link

M/S (J2=0)

M/S (J2=1)

1 x P1

2x P2

CLK

Data0

Data1

I2C

TRG/Config

R47

OR

R44

10k

12k

VAUX

Vaux=2V5

TMS(4)

VAUX(2)

TCK(6)

TDO(8)

TDI(10)

SDA(7)

SCL(9)

P1 (3V)

0.2A

P2 (1V8)

~ 1.6A

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Spartan firmware

“Light-DTCC” protocol with one particularity: Configuration and DAQ are mutually exclusive.
Larger system overview loop: FEC <-> DVM <-> HDMI<->VMM

K28.x symbols
Clk & Phase to VMM

Virtex 6
Xilinx code
FSM link phaser

FEC card

Link Status 1..4

VMM hybrid

Spartan 6
Xilinx code
FSM link phaser

HDMI cable Link

cable
5 or 2 m

LVDS transceiver

TX (Cfg)

Rx(data)

Data from VMM

Data lines to FEC

Data from VMM

LVDS transceiver

GND

HDMI-A

other channels

HDMI-D

VMM

1

VMM

2

Data lines to FEC

Data from VMM

Data from VMM

VMM 1

VMM 2

Cfg.to VMM

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DTCC protocol (Data trigger clock and controls)

- LVDS links (low voltage differential signaling)
- 8b10b encoding
- Trading overhead for:
  - Link control and word delimiting
  - Better electrical properties of transmission
### 8b/10b control words

#### VMM <-> FEC synchronization

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<td>010001 0111</td>
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</table>

- Link FEC to VMM
- IDLE VMM to FEC
- VMM DATA header
- FEC ACQ mode
- FEC Config header
- VMM ART header
FEC-VMM link status state machine

0. LOS
  any input
  Link code

1. SAP
  Link code

2. Align
  RX is aligned
  Link code

3. Link
  Idle code
  Link code

4. Idle
  cfg data or Idle code
  Acq enable

5. Acq
  Acq or Idle code

6. Acq
  VMM data

7. Acq
  Idle code

8. Acq
  Acq code

9. Acq
  VMM data

1. Init
  PHY sync
  Link codes

2. CheckLink
  Link code

3. Link
  not Link code
  Link code

4. CheckIdle
  Idle code

5. Idle
  Idde code
  Acq data or Idle code

6. Idle
  Acq or Idle code

7. Idle
  VMM data

8. Idle
  Acq code

9. Idle
  VMM data

10. Idle
    Acq or Idle code
Spartan Firmware enhancement list

- Clean up the code and document it
- Configuration readback
- EEPROM – ID number, default configuration for VMMs, also for testing
- HDMI connector selection on reset
- Utilization of Powerbox – Master-Slave mode, FastOR through ART
- Other schemes: e.g. Atlas-like mode, spill-buffer mode
- Improving and stabilizing readout speed from VMMs to Spartan

Patrick Schwäbig

10/02/2020
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VMM3a hybrid block diagram

Update V4.0 -> V4.1 in green

From detector

64 channels

J1

64 channels

J10

U2
VMM3a
VMM-1, ch0-63

ADC
I2C

U1
Spartan FPGA

U3
VMM3a
VMM-2, ch64-127

ADC
I2C

J4

ID chip
EEprom

DTCC link

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Testing, configuration

1.) Unique 128 bit ID for VMMhybrids
2.) Default VMM configuration at Power up
3.) ADC outputs

uPython board PYBv1 used as I2C master

3V power*
2.5V AUX
SCL, SDA 2.5V
GND

New small programming adapter PCB

ID chip

I^2^C-Compatible (2-wire) Serial EEPROM with a Unique, Factory Programmed 128-bit Serial Number
1-Kbit (128 x 8), 2-Kbit (256 x 8)
Thank you for your attention!

Questions?