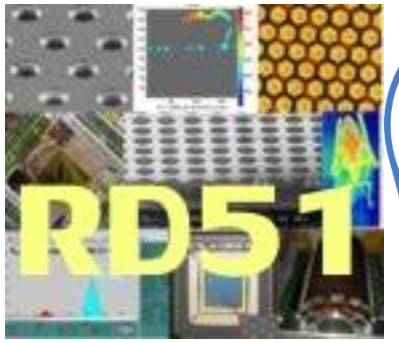




# VMM hybrid firmware development

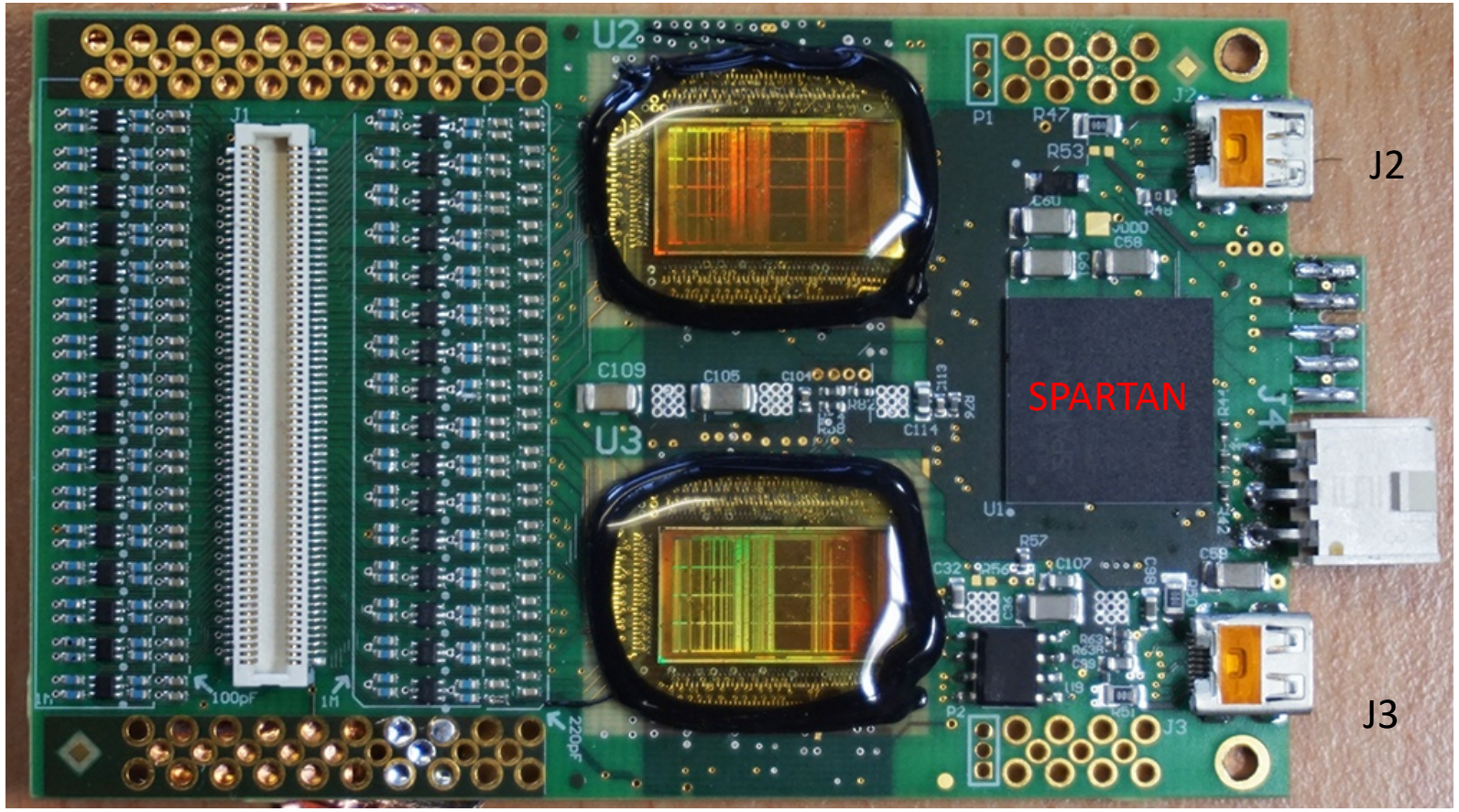
Marek Hracek

RD51 Mini-Week

# About me

- Czech Republic
- Microelectronics at Brno University of Technology
- Part of GDD as associate member from Institute of Experimental and Applied Physics (Czech University of Technology)

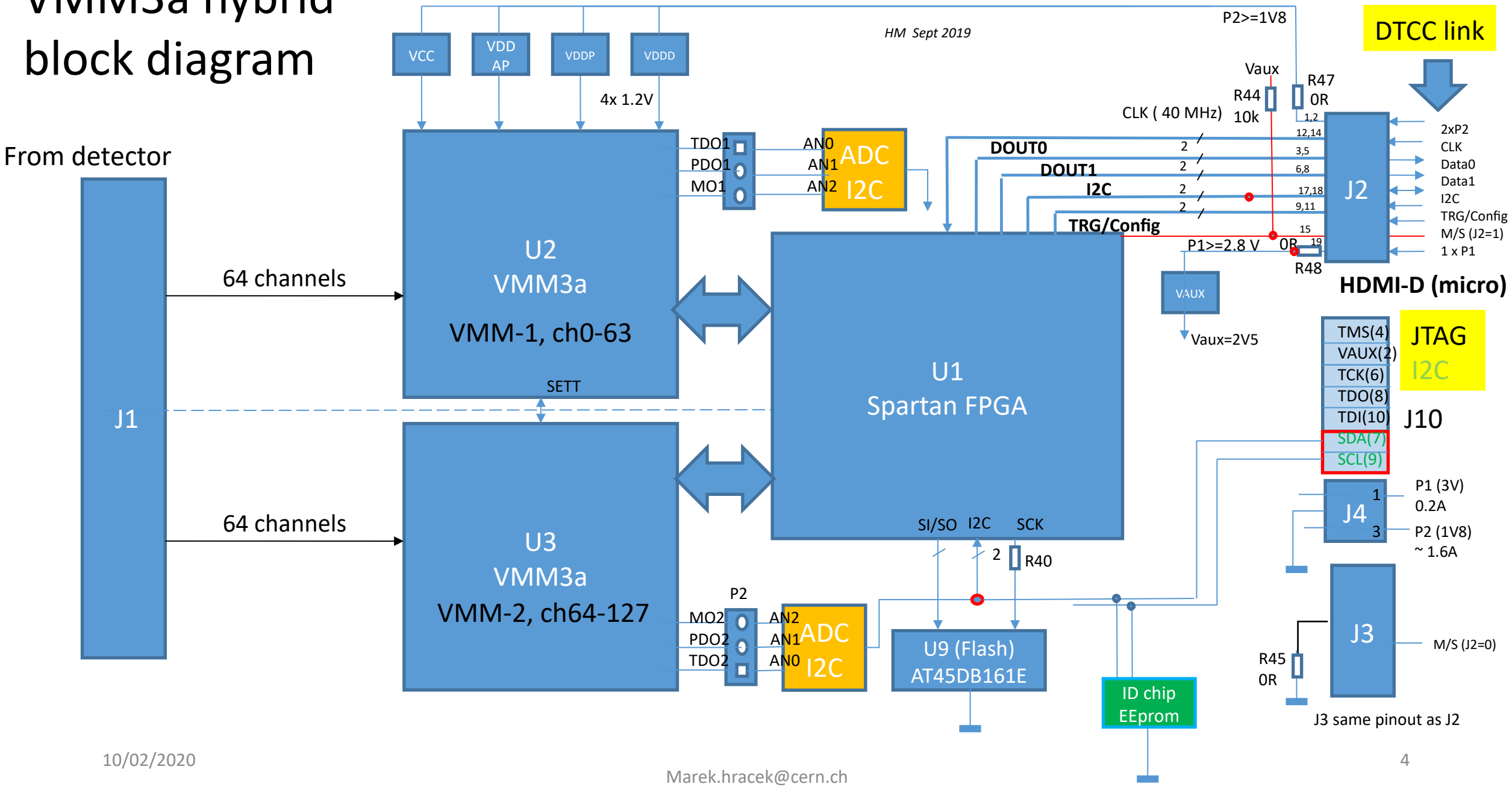
# VMM hybrid board




VMM3 prototype  hybrid 2017

Note: translucent Globtop only on prototypes

# VMM3a hybrid block diagram



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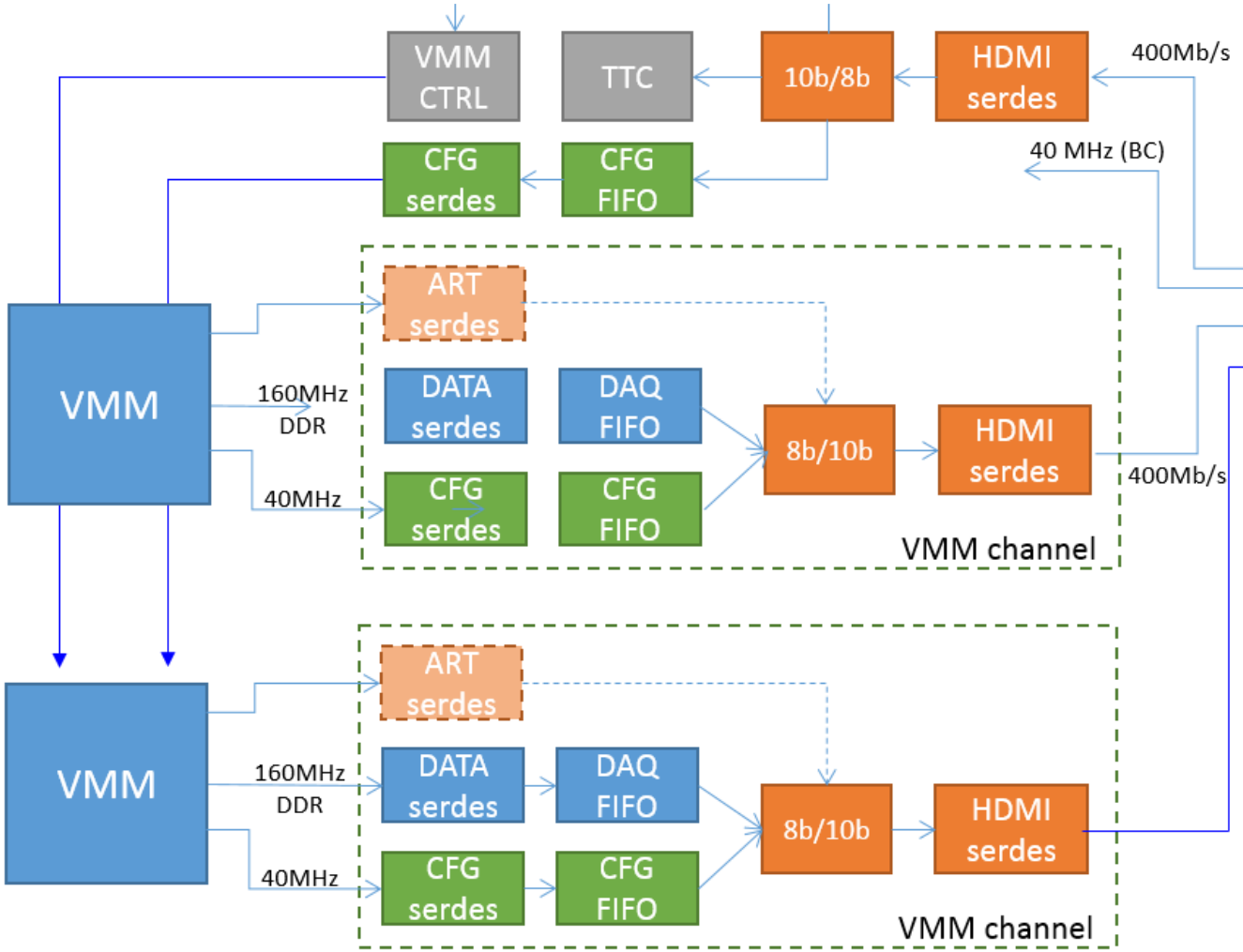
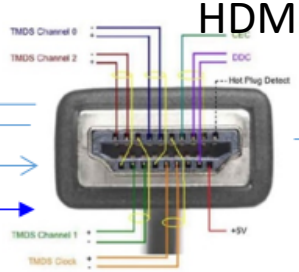
# Spartan firmware



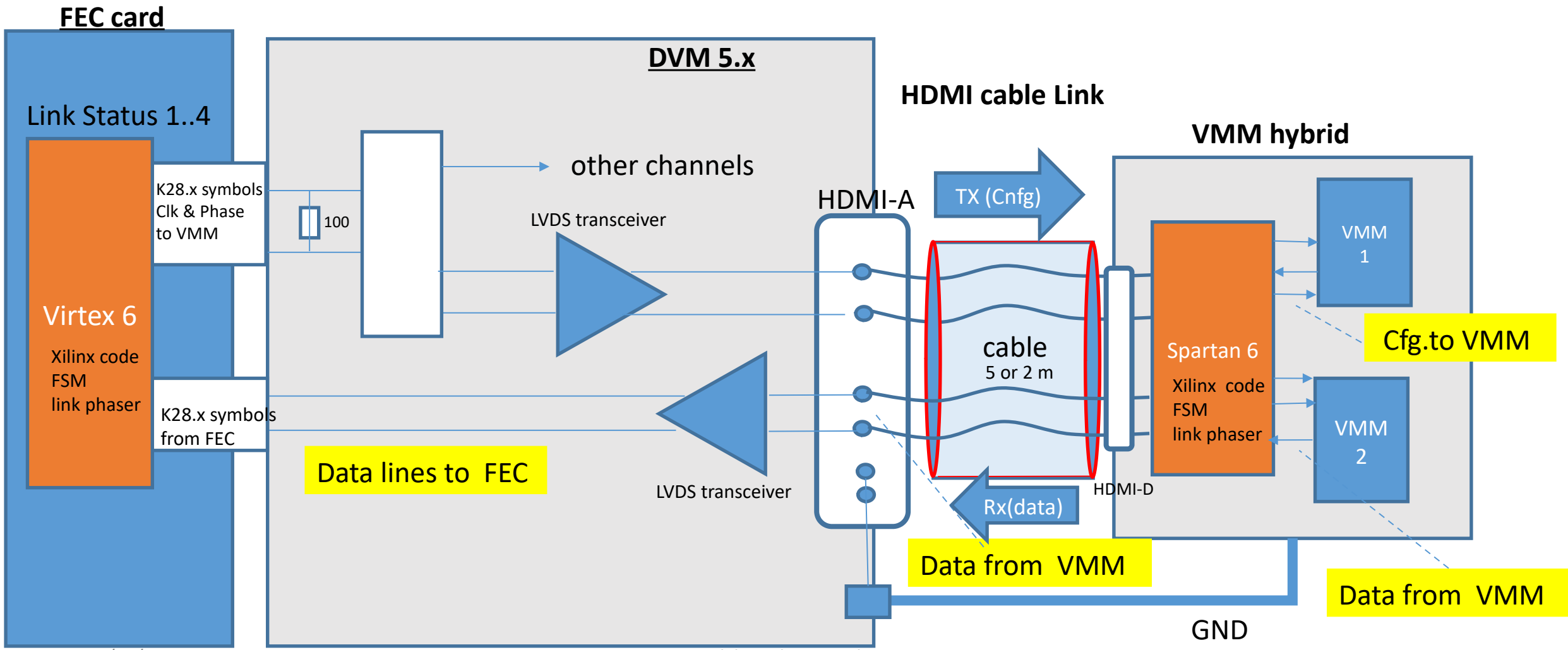

→ DAQ Data (Uplink)
→ ART Data (Uplink)
- "Fast-Or" with address

↔Configuration (Up/Downlink)
← TTC (Downlink)

← Power

*"Light-DTCC" protocol with one particularity: Configuration and DAQ are mutually exclusive.*

# Larger system overview
# loop: FEC <-> DVM <-> HDMI<->VMM



# DTCC protocol (Data trigger clock and controls)

- LVDS links (low voltage differential signaling)
- 8b10b encoding
- Trading overhead for:
  - Link control and word delimiting
  - Better electrical properties of transmission

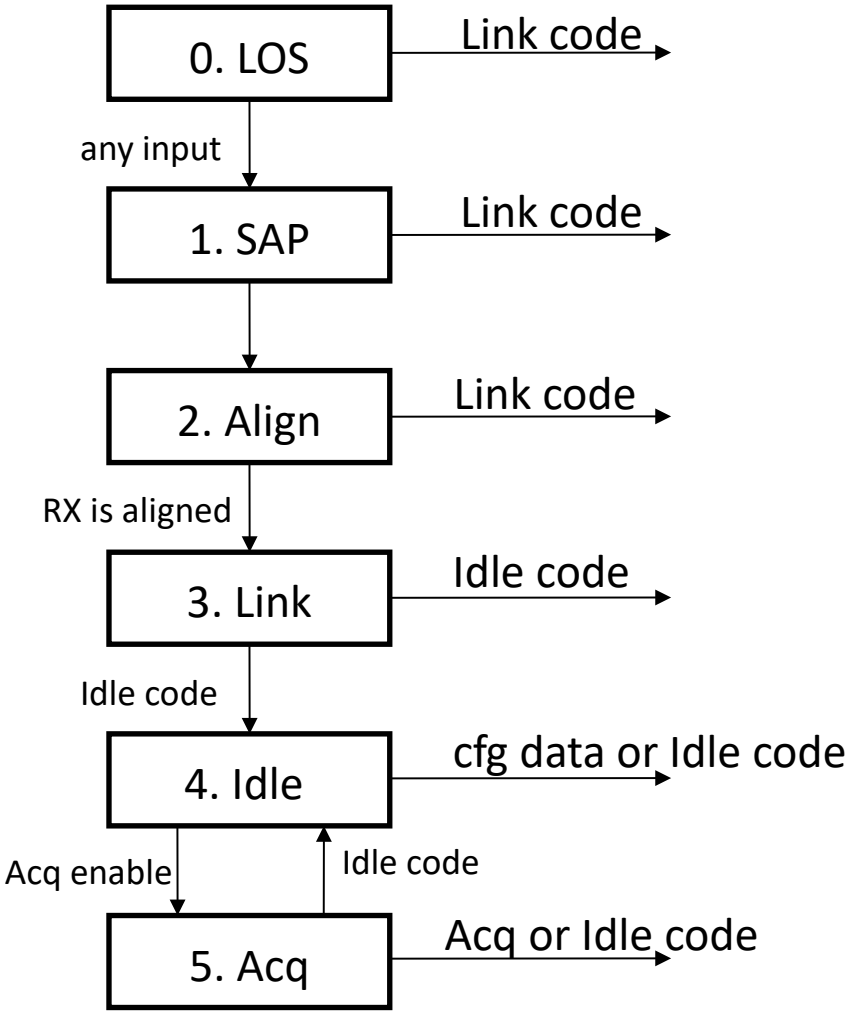
# 8b/10b control words

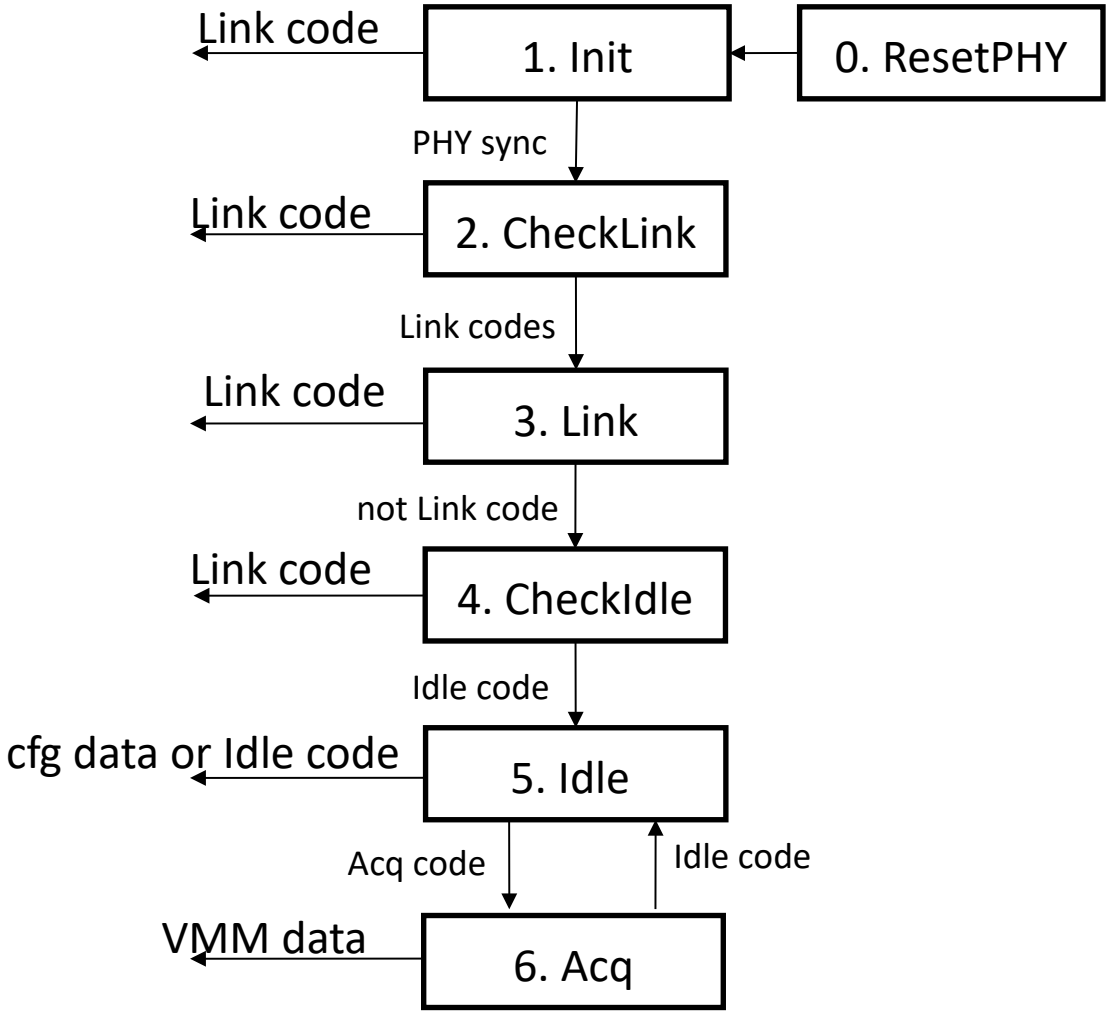
| | | | | |
|---|---|---|---|---|
| K28.0 | 1 | 000 11100 | 001111 0100 | 110000 1011 |
| K28.1 | 1 | 001 11100 | 001111 1001 | 110000 0110 |
| K28.2 | 1 | 010 11100 | 001111 0101 | 110000 1010 |
| K28.3 | 1 | 011 11100 | 001111 0011 | 110000 1100 |
| K28.4 | 1 | 100 11100 | 001111 0010 | 110000 1101 |
| K28.5 | 1 | 101 11100 | 001111 1010 | 110000 0101 |
| K28.6 | 1 | 110 11100 | 001111 0110 | 110000 1001 |
| K28.7 | 1 | 111 11100 | 001111 1000 | 110000 0111 |
| K23.7 | 1 | 111 10111 | 111010 1000 | 000101 0111 |
| K27.7 | 1 | 111 11011 | 110110 1000 | 001001 0111 |
| K29.7 | 1 | 111 11101 | 101110 1000 | 010001 0111 |
| K30.7 | 1 | 111 11110 | 011110 1000 | 100001 0111 |

VMM <-> FEC synchronization

- Link FEC to VMM
- IDLE VMM to FEC
- VMM DATA header
- FEC ACQ mode
- FEC Config header
- VMM ART header

# FEC-VMM link status state machine



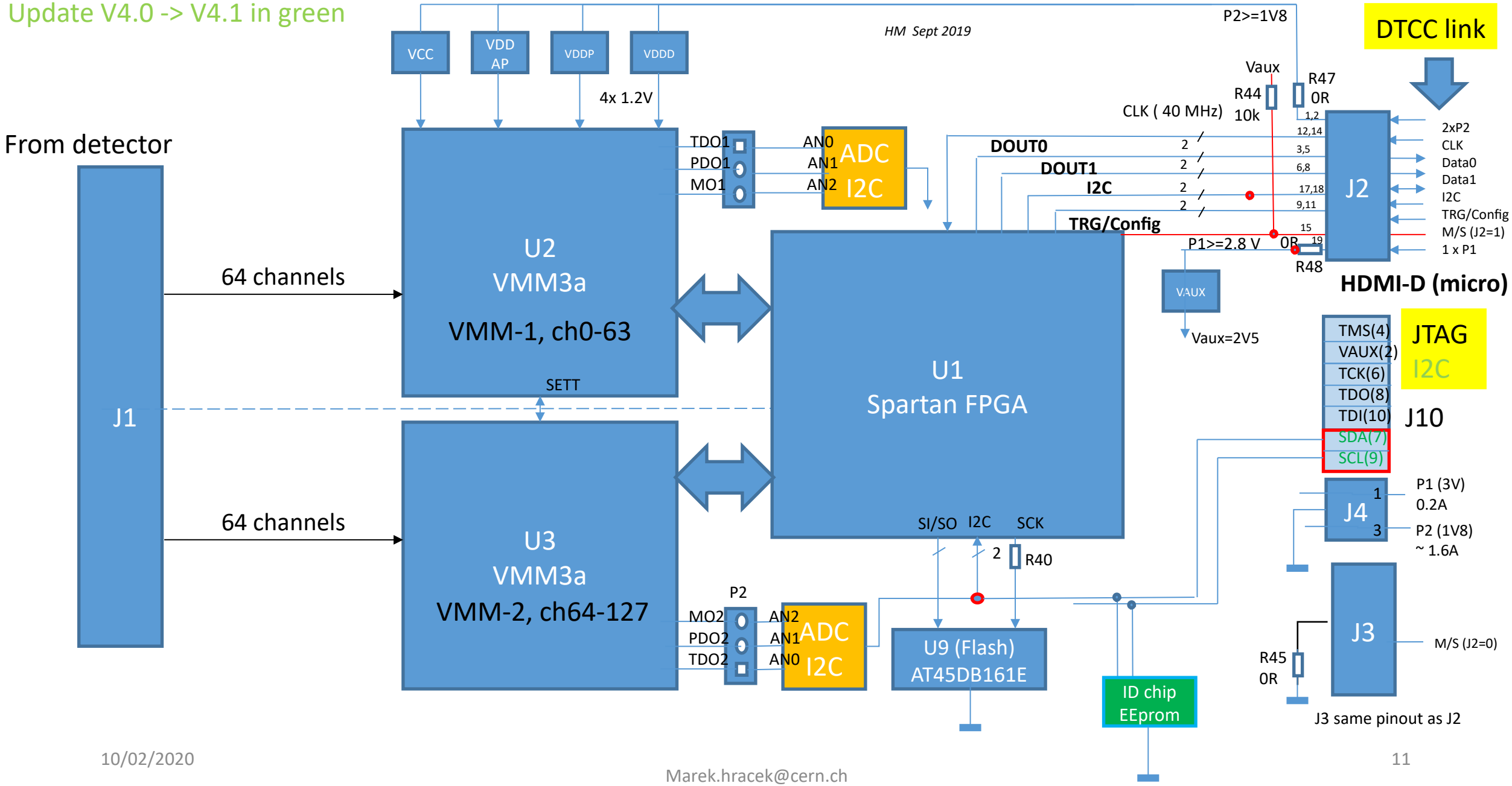



# Spartan Firmware enhancement list

- Clean up the code and document it
- Configuration readback
- EEPROM – ID number, default configuration for VMMs, also for testing
- HDMI connector selection on reset
- Utilization of Powerbox – Master-Slave mode,
  FastOR through ART
- Other schemes: e.g. Atlas-like mode, spill-buffer mode Patrick Schwäbig
- Improving and stabilizing readout speed from VMMs to Spartan

# VMM3a hybrid block diagram

Update V4.0 -> V4.1 in green



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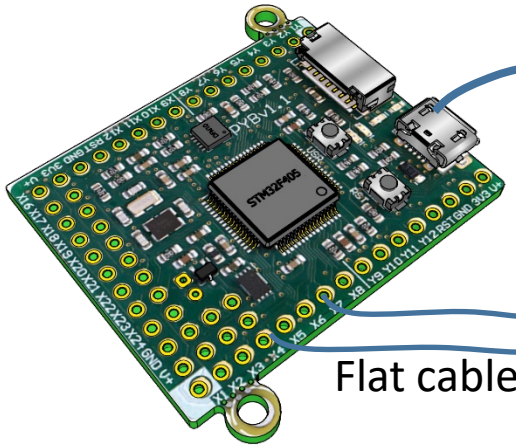
# Testing, configuration


1.) Unique 128 bit ID for VMMhybrids
2.) Default VMM configuration at Power up
3.) ADC outputs

uPython board PYBv1
used as I2C master

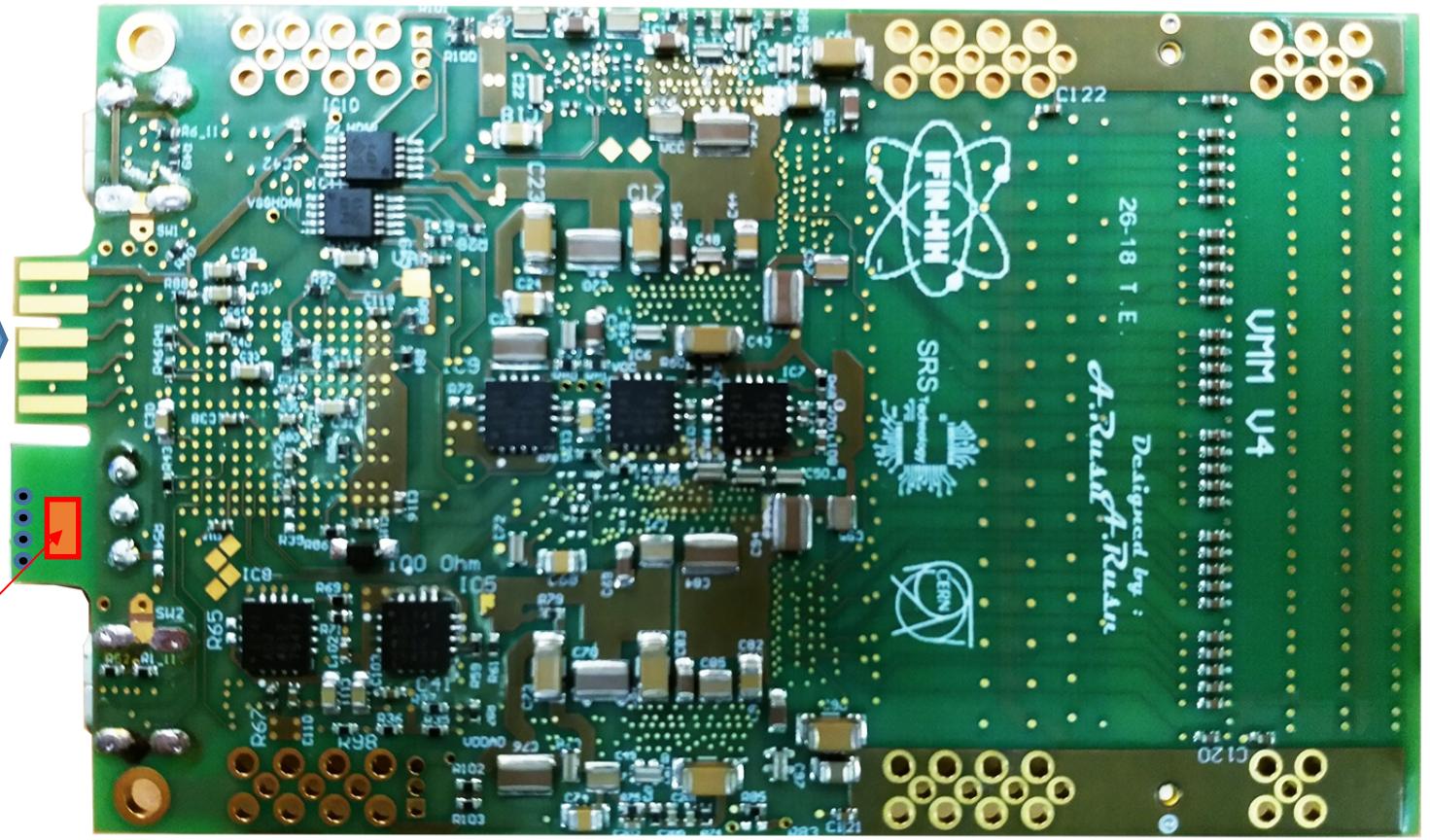
USB



3V power*
2.5V AUX
SCL,SDA 2.5V
GND

Flat cable

New small programming adapter PCB




## ID chip

**I²C-Compatible (2-wire) Serial EEPROM with a Unique, Factory Programmed 128-bit Serial Number**
**1-Kbit (128 x 8), 2-Kbit (256 x 8)**

# Thank you for you attention!

Questions?