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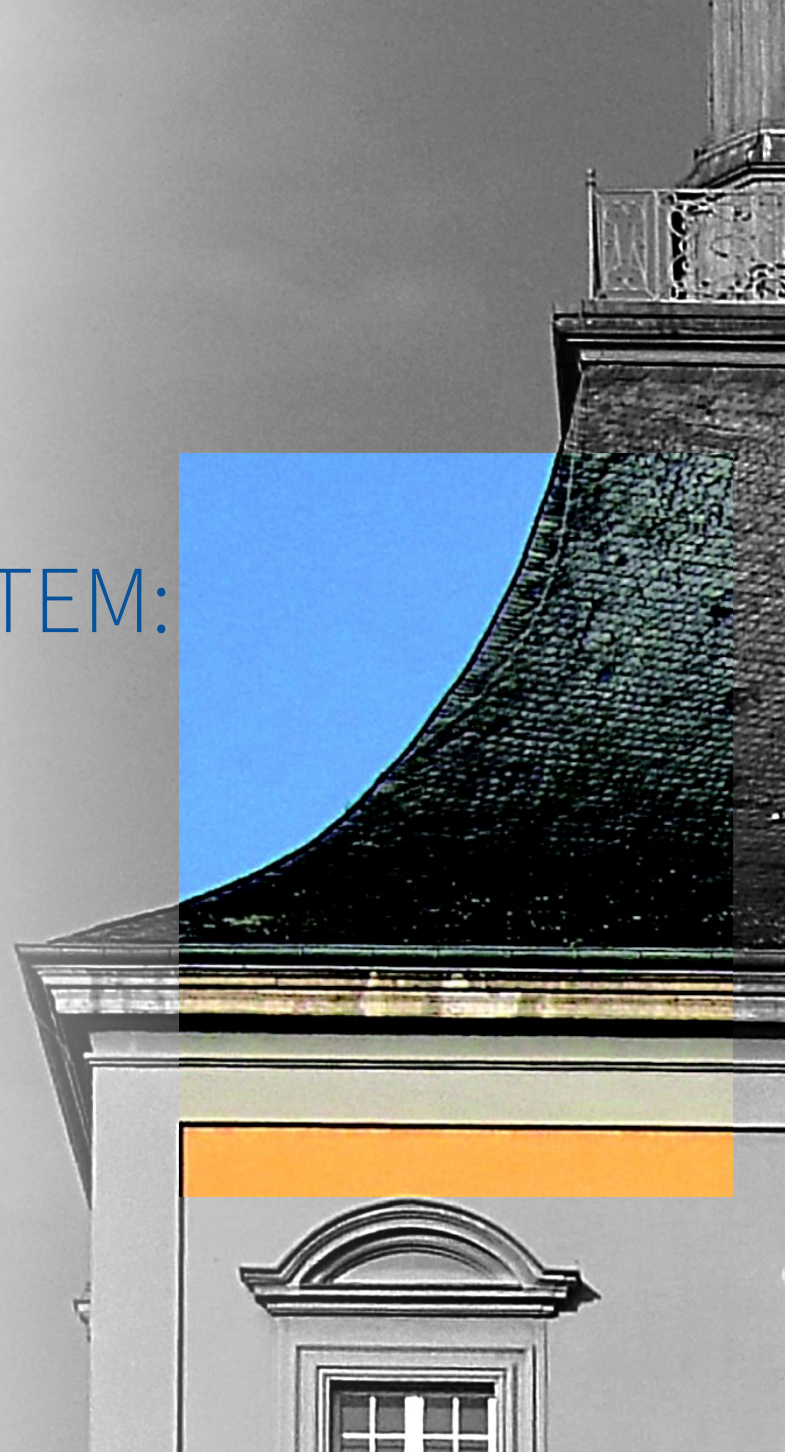
Physikalisches Institut

SCALABLE READOUT SYSTEM: UPDATES OF THE VMM HYBRID FIRMWARE

Patrick Schwäbig

RD51 Mini-Week, 2/10/2020



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OUTLINE

- The VMM
- The Scalable Readout System
- Speed-up of data transfer between VMM and FPGA
- Improved storage of VMM configuration on the FPGA
- Summary

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THE VMM

- Front-end ASIC for tracking detectors (DOI:10.1109/NSSMIC.2012.6551184)
- Current version: VMM3a (ATL-MUON-PROC-2019-010)
- Highly flexible, large range of configuration parameters
- 64 channels
- Continuous readout at high rates, low electronic noise
- Single channel: Can handle hit rate of up to 4 MHits/s
- Used for Micromegas and sTGC detectors of the ATLAS New Small Wheel (NSW)
- Will also be used at various other experiments e.g. for the NMX instrument at ESS in Lund, Sweden

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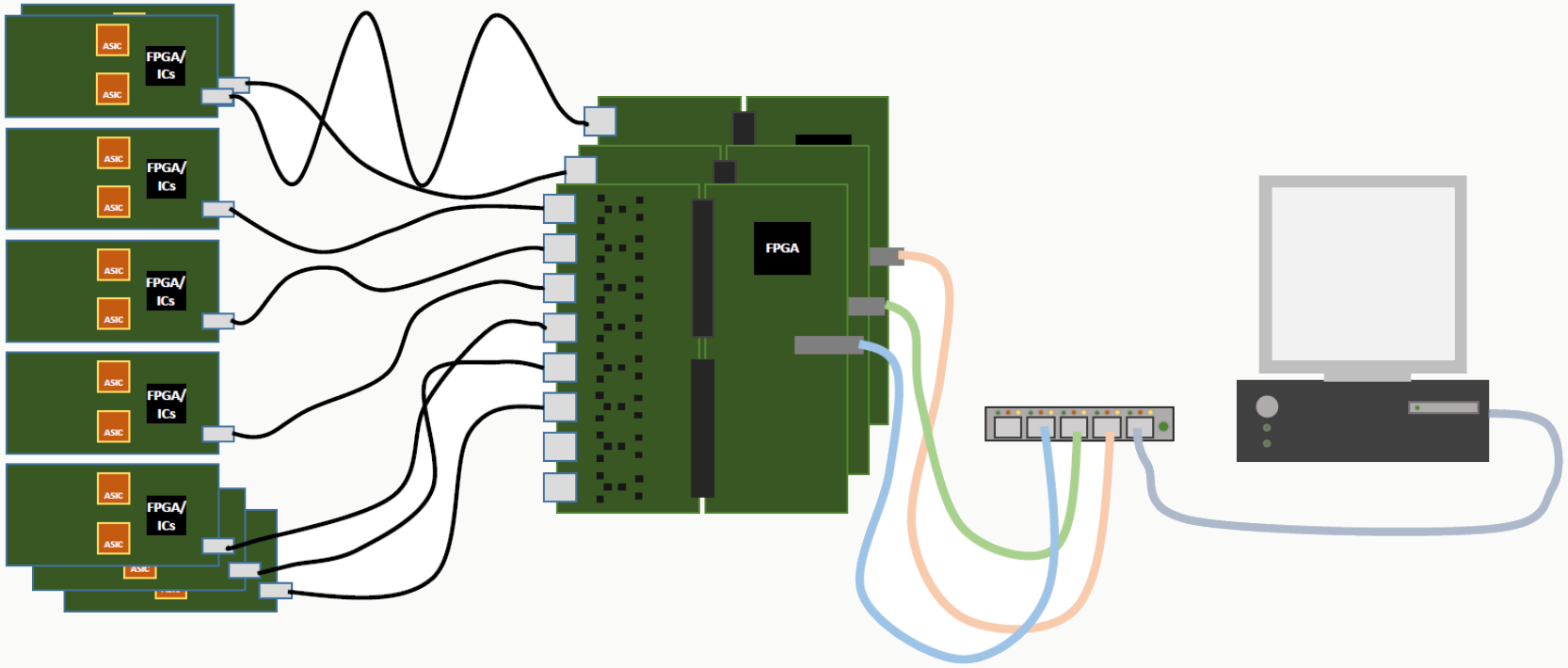
THE SCALABLE READOUT SYSTEM (SRS)

- Versatile read-out system
- Scalable from a few dozen to many thousand channels
- Compatible with different front-end ASICs
- Implemented: APV25 and VMM (since 2018, DOI: 10.1016/j.nima.2018.06.046)

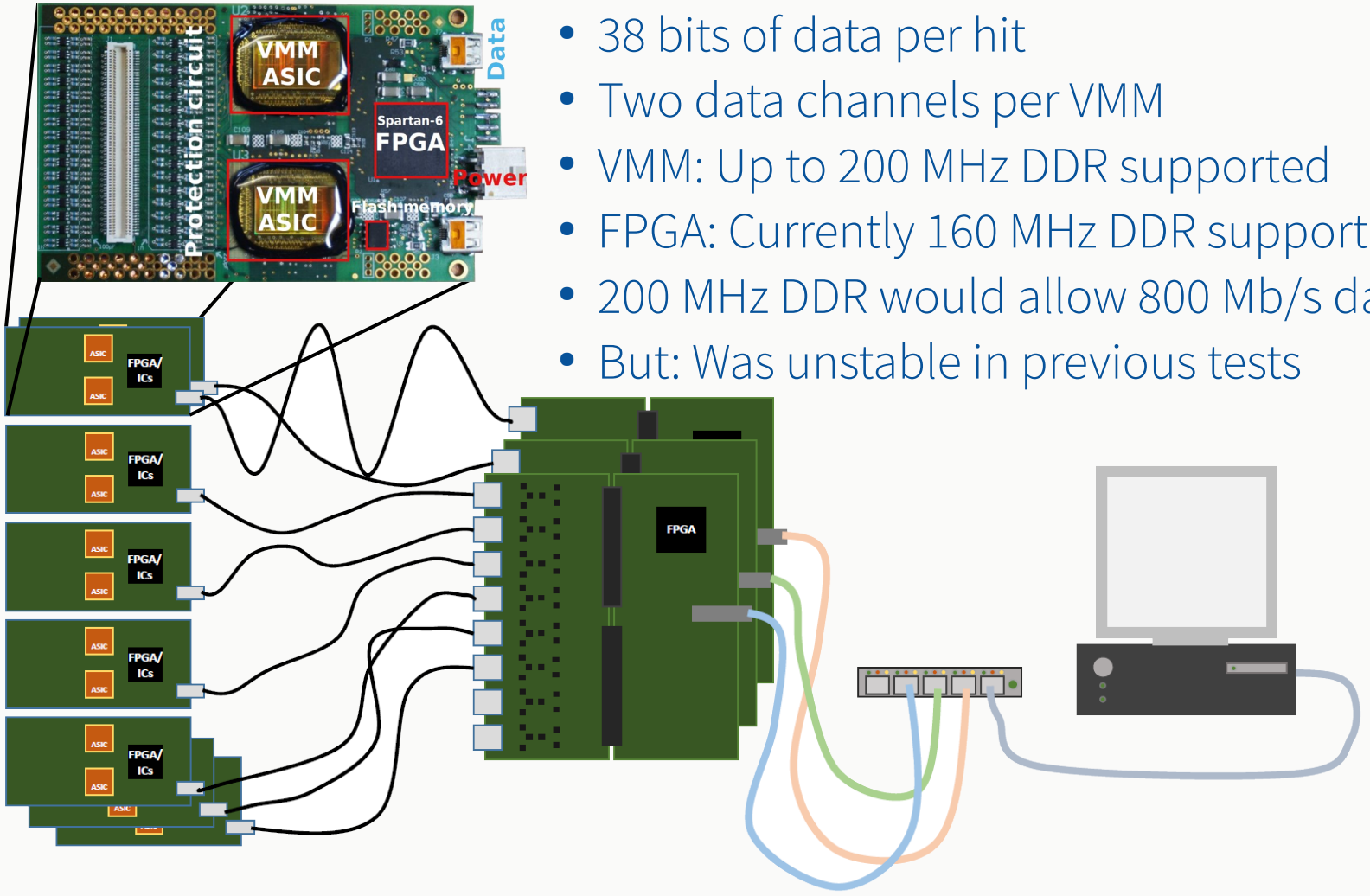


Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch →Ethernet → PC

THE SRS AND THE VMM

Data transfer between VMM and FPGA (Spartan-6):

- 38 bits of data per hit
- Two data channels per VMM
- VMM: Up to 200 MHz DDR supported
- FPGA: Currently 160 MHz DDR supported
- 200 MHz DDR would allow 800 Mb/s data transfer
- But: Was unstable in previous tests



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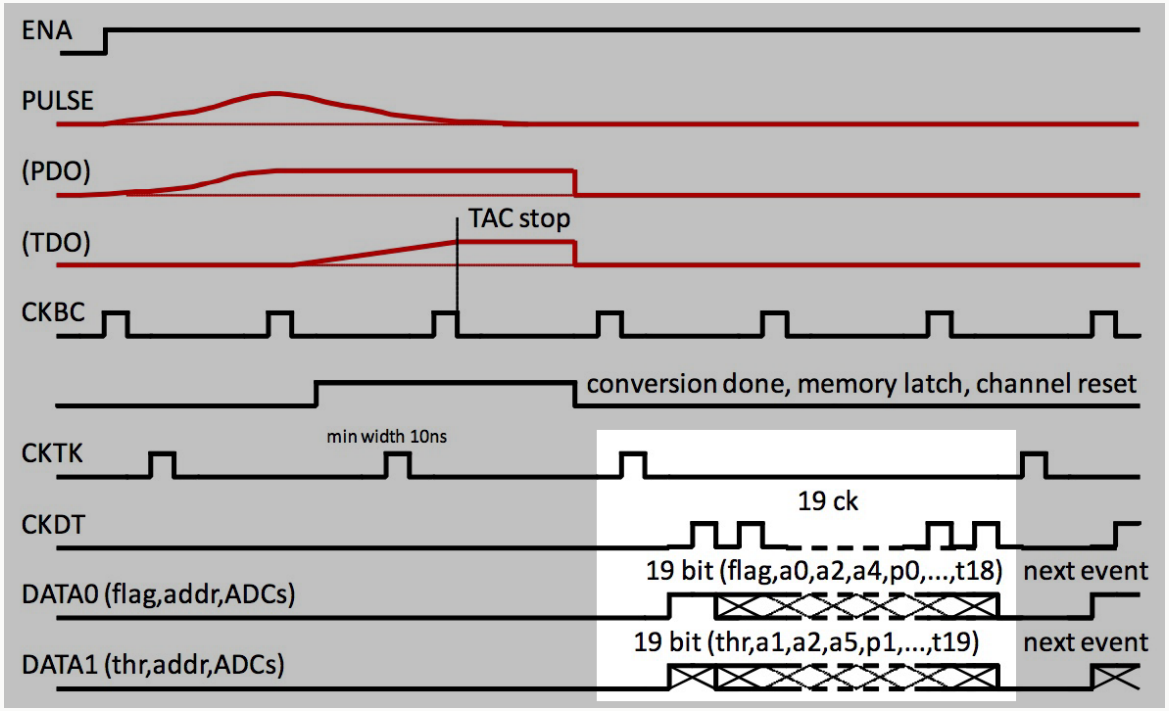
DATA TRANSFER BETWEEN VMM AND FPGA (CONTINUOUS MODE)



Data transfer:

- FPGA sends tokens on **CKTK**
- If VMM has data, raises flag after token on **DATA0**
- FPGA starts data clock on **CKDT**
- VMM sends data on **DATA0** and **DATA1**, 19 bits each

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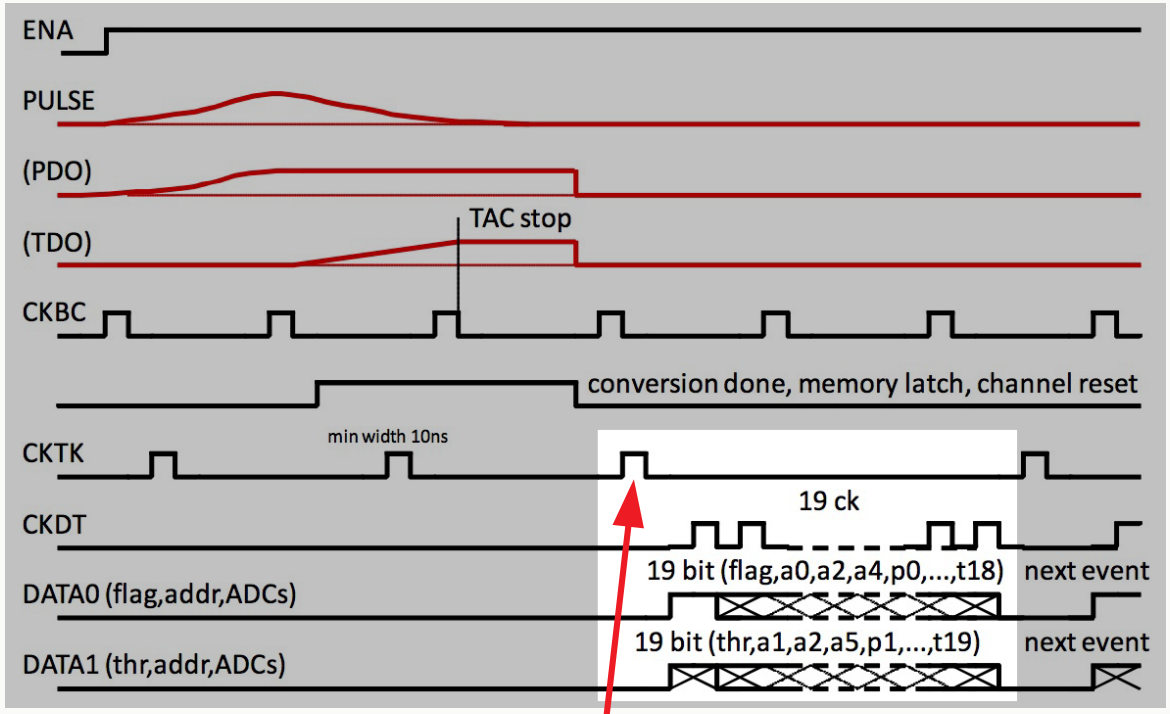

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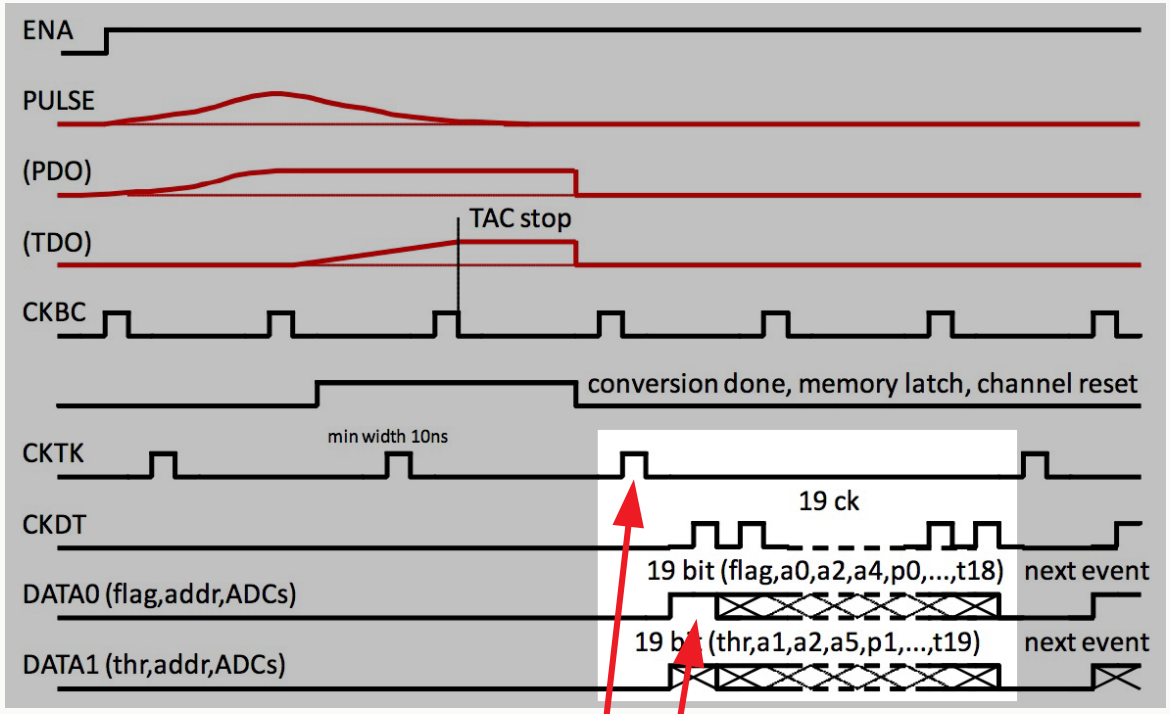

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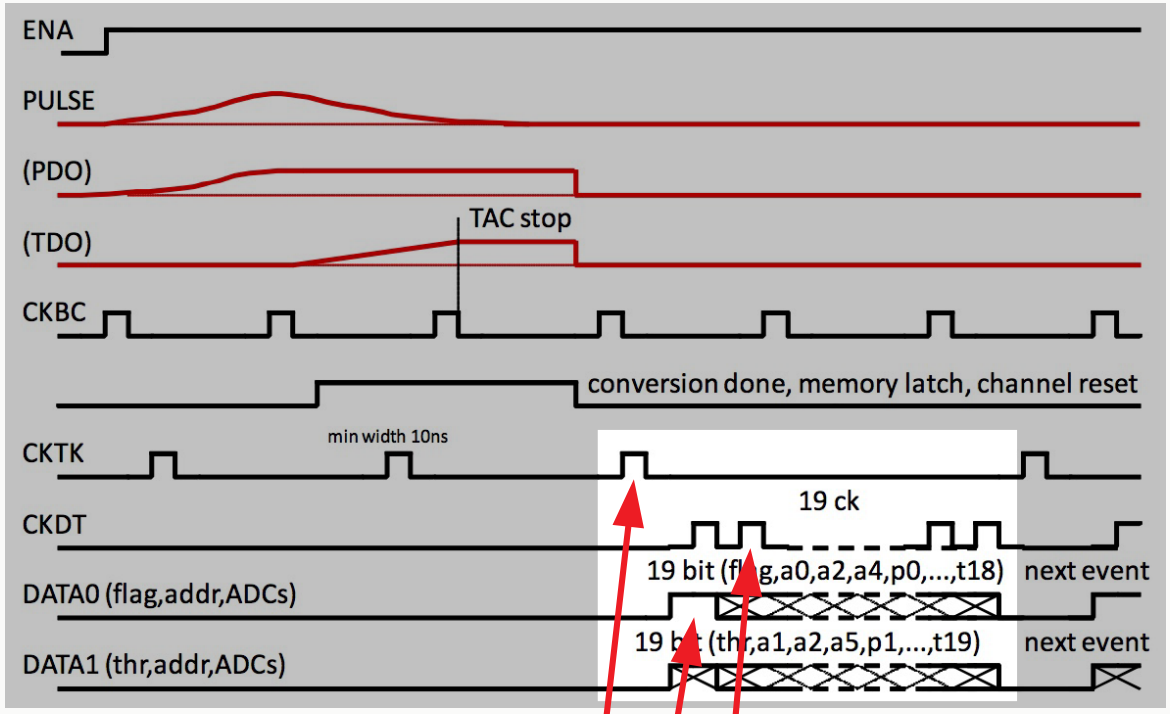

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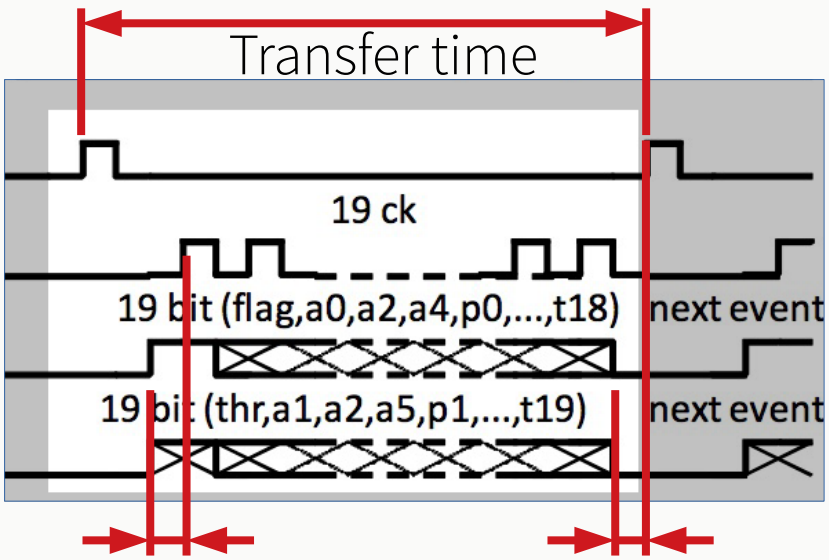
SPEEDING UP DATA TRANSFER BETWEEN VMM AND FPGA



CKDT frequency:

- VMM: up to 200 MHz DDR supported
- FPGA: Currently 160 MHz DDR supported
- Tests showed: VMM could not keep up with 200 MHz DDR
  (random bits sent twice)
- Problem verified (for our operating parameters) by VMM designer
- **But: 180 MHz DDR works!**

Aim: Reduce transfer time as far as possible

- Reduce time between flag and starting of CKDT
- Reduce time between end of CKDT and next token
- Shorter tokens

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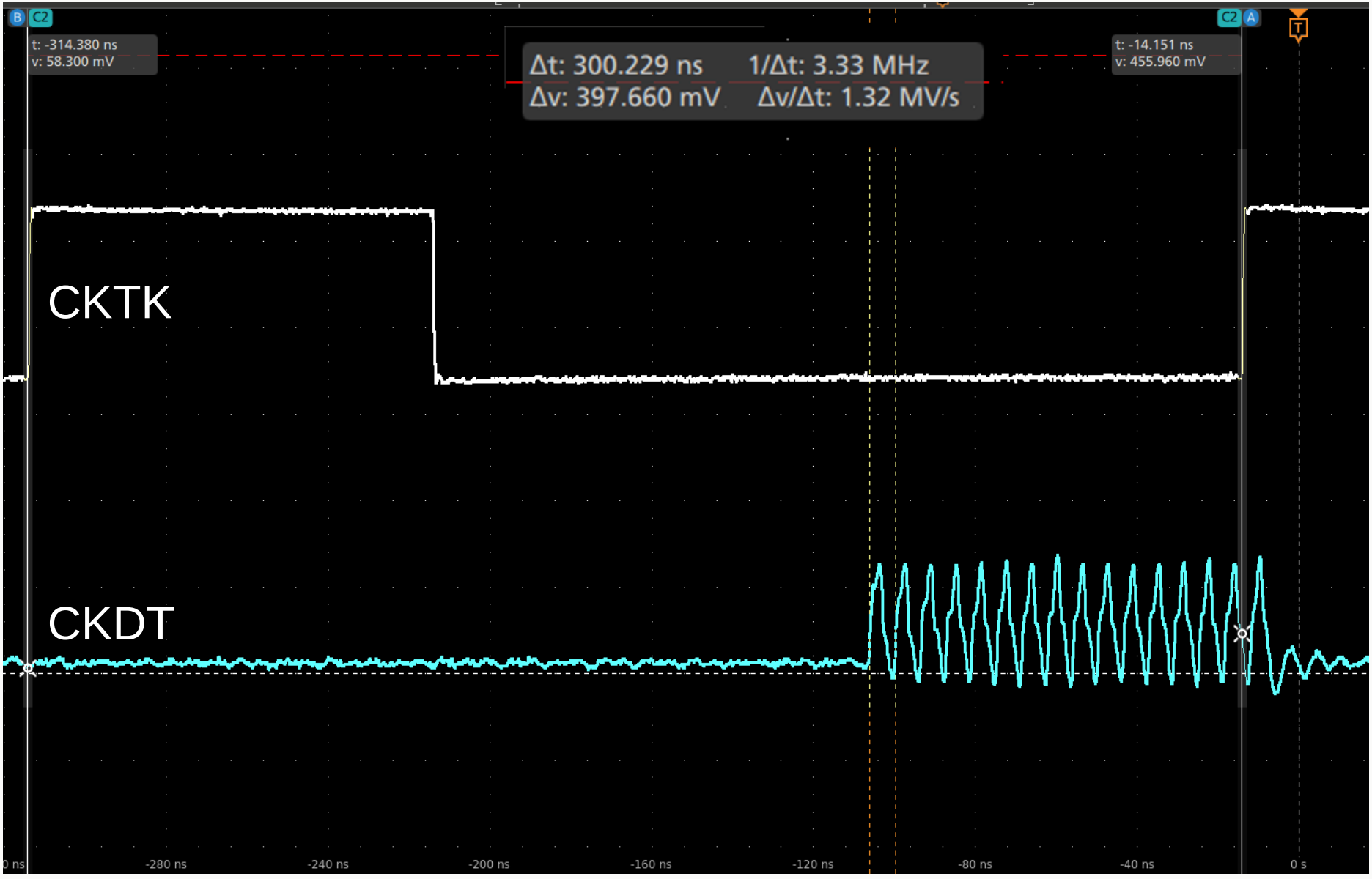
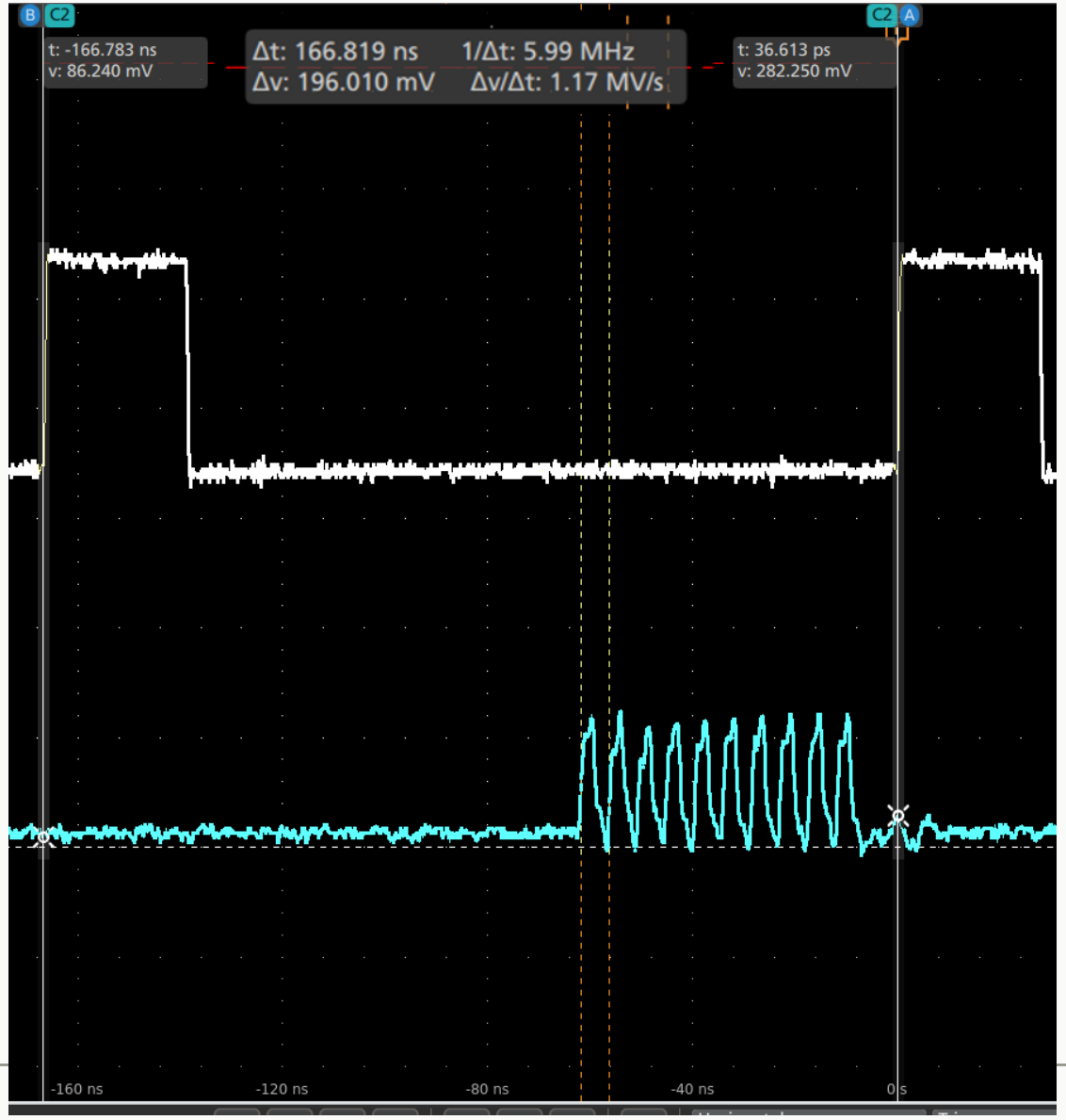
DATA TRANSFER – OLD FIRMWARE (160 MHZ DDR)



DATA TRANSFER – NEW FIRMWARE (180 MHZ DDR)

CKTK

CKDT



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DATA TRANSFER BETWEEN VMM AND FPGA

160 MHz DDR, old firmware: about 300 ns
180 MHz DDR, new firmware: about 167 ns

→ Nearly halved transfer time

Other features:

- CKDT can be changed (using PLL DRP feature of Spartan-6)
  180 MHz, 90 MHz, 45 MHz, 22.5 MHz (SDR and DDR)
- Compensation for data shifts
  e.g. due to process variations, CKDT change etc.:
  auto-calibration using test pulses (work in progress)

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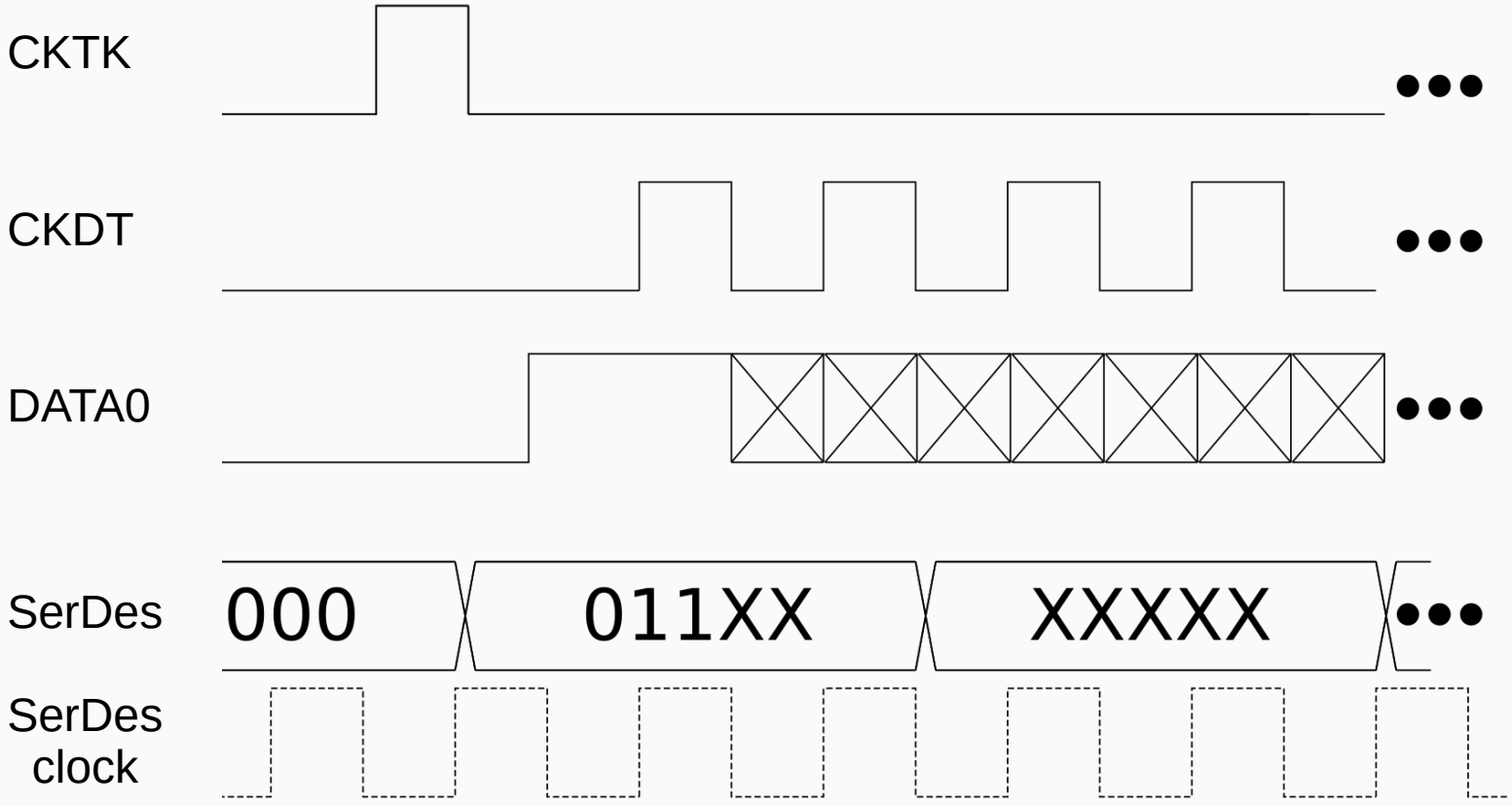
AUTO-CALIBRATION



Multiple leading ‘1’, shifted depending on phase between SerDes and data

- affected by delay between token and flag
- time between recognizing flag and start of CKDT

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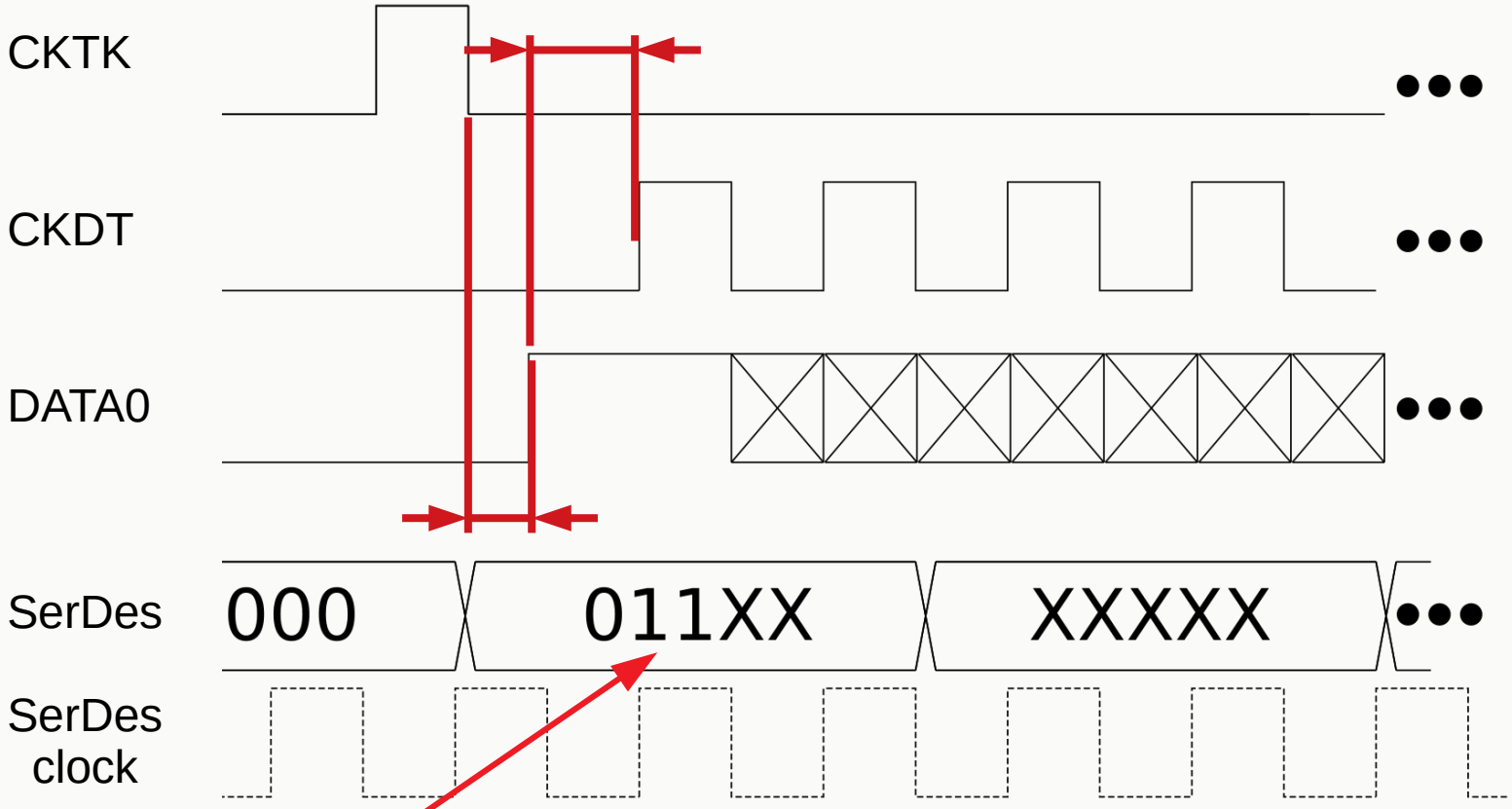

Multiple leading ‘1’, shifted depending on phase between SerDes and data

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AUTO-CALIBRATION (WORK IN PROGRESS)

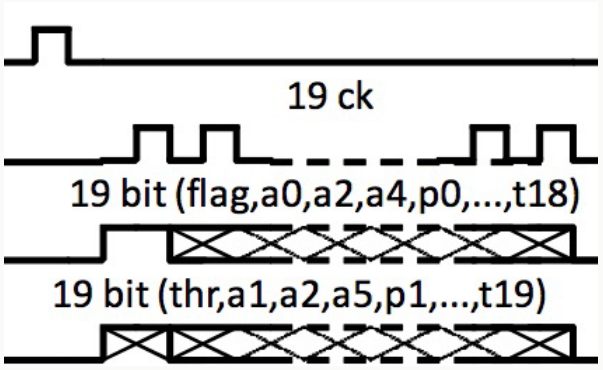
Where does the data really start?

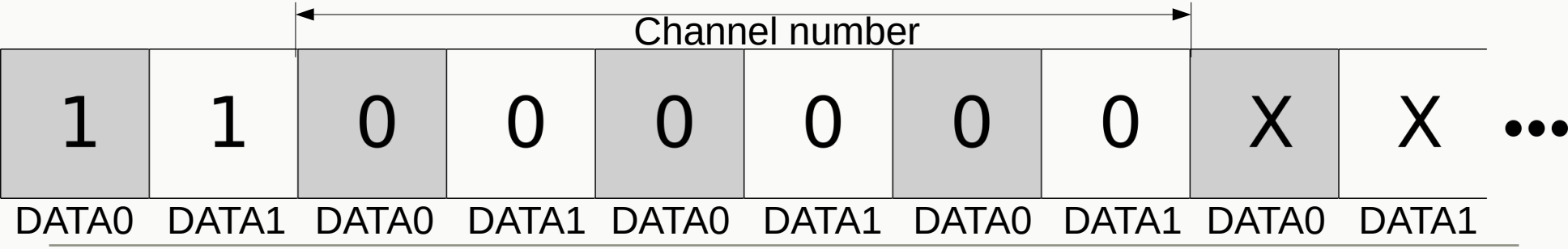
Old firmware:

- counters with different frequencies
- for each CKDT frequency setting a set of conditions
  which counter must have which value

New firmware:

- send test pulse on a single channel, e.g. channel 0
- where does the first '0' occur?
- infer data shift from this information
- apply this shift to all incoming data





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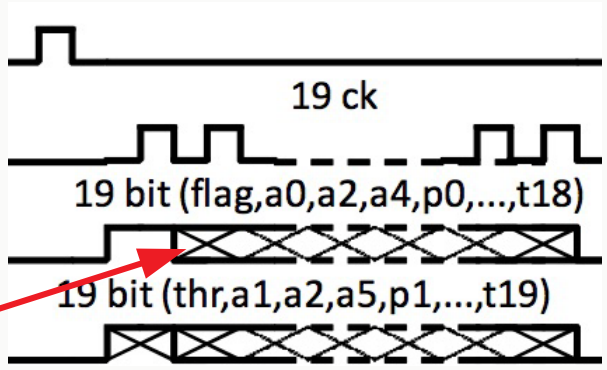

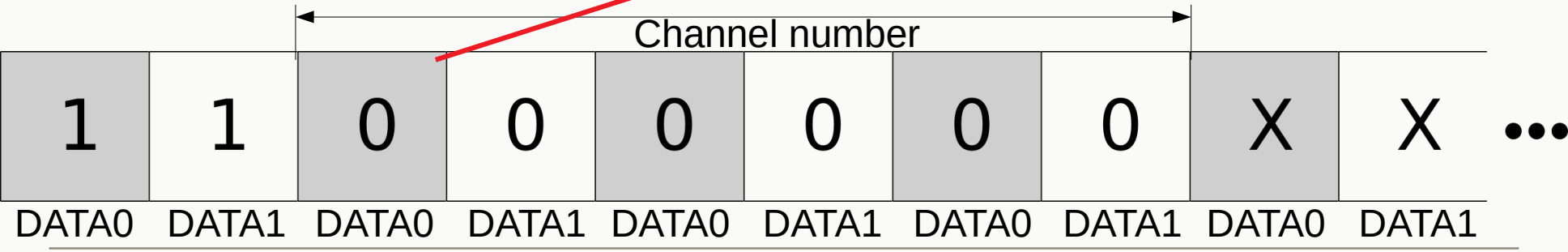

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STORING VMM CONFIGURATION IN BRAM

- Configuration bits for the VMM (about 1.7K each) sent from FEC to FPGA
- FPGA forwards configuration to VMM
- Old firmware: stores configuration in FPGA logic (2 vectors, 1.7Kbit each)
- New firmware: stores configuration in Block RAM

	Old firmware	New firmware
Number of used Slice Registers	4,547 (24%)	1,205 (6%)
Number of used Slice LUTs	9,112 (42%)	1,574 (17%)

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SUMMARY

→ Implemented updates for the VMM Hybrid firmware

For this: tested supported VMM data rates
180 MHz at double data rate seems to be maximum

- Rewrote the code responsible for receiving data
- Reduced data transfer time per hit from 300 ns to 167 ns
- CKDT frequency can be changed using the PLL DRP
- Possible shifts in data avoided by auto-calibrating with test pulse
- Storing VMM configuration in Block RAM, saving a large fraction of resources

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Thanks for your attention!

Questions?