EMCI / EMP / ELMB2 monthly meeting
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EP-ESE-FE
EMCI features

- VTRX+ optical link to FMC connector through IpGBT
- Up to 28 TX and CLK e-links and 16 RX e-links
- FMC footprint (HPC) on both sides (only one at a time)
- Possibility to connect to FMC (LPC), losing some features
- Possibility to attach different connector (e.g. SMA) to VTRX+ connector
- ADC (8 ch, 10 bit)
- DAC (1 ch, 12 bit)
EMCI features

- Phase shifter CLK (4 ch.)
- GPIO (16 ch.)
- I2C (2 ch.) (there is a 3\textsuperscript{rd} ch. for VTRX+)
- Extra SCA e-link (lower speed)
- Extra connector for IpGBT configuration
- DIP switches for extra IpGBT configuration (MODE, ADR, SC\_I2C)
- E-fuse through extra connector or pushbutton
Power

5-12V coming from FMC connector

- FEASTMP $\rightarrow$ 2.5V, 10W (flat version limits the power)
  - It may be possible to fit between PCBs
- bPOL2V5 $\rightarrow$ 1.2V, 3.6W
Not included lpGBT features

• External VREF for ADC/DAC
• External reference CLK (only needed when used as simplex TX)
• TSTOUT pins (used for lpGBT debugging)
• Other lpGBT debug lines (STATEOVRD, PORDIS, VCOBYPASS…)}
FMC standard

User-defined pins:
- LA[00..33]_P/N (LPC) (34 d) – User defined
- HA[00..23]_P/N (HPC) (24 d) – User defined
- HB[00..21]_P/N (HPC) (22 d) – User defined (not debuggable using FPGA eval. board)
- DP[0..9]_M2C_P/N (10 d) – Gigabit transceiver (not debuggable using FPGA eval. board)
- DP[0..9]_C2M_P/N (10 d) – Gigabit transceiver (not debuggable using FPGA eval. board)

Example pinout:
- E-links (16+28+28 d):
  - LA[00..24]_P/N (7 OUT, 9 IN, 9 CLK)
  - HA[00..13]_P/N (3 OUT, 6 IN, 6 CLK)
  - HB[00..21]_P/N (6 OUT, 8 IN, 8 CLK)
  - DP0_M2C_P/N and DP0_C2M_P/N (1 IN, 1 CLK)
  - DP[1..9]_M2C_P/N and DP[1..9]_C2M_P/N (2 OUT, 6 IN, 6 CLK)
- ADC x8 (8 se, can be used in diff.)
  - LA[25..26]_P/N (4 ch)
  - HA[14..15]_P/N (4 ch)
- GPIO x16 (16 se)
  - LA[27..30]_P/N (8 ch)
  - HA[16..19]_P/N (8 ch)
- E-link for SCA (3 d)
  - HA[20..22]_P/N
- DAC (1 se)
  - LA33_P
- I²C x2 (4 se) (there is extra one for VTRX+)
  - LA[31..32]_P/N
- Phase shifter CLK x4 (4 d)
  - HA23_P/N (1 ch)
  - DP[1..3]_C2M_P/N (3 ch)
- RSTOUTB (1 se)
  - LA33_N

If the FMC connector is soldered in the bottom side of the PCB all the connections will be mirrored and this standard will not be met.
E-links

28 TX, 28 CLK, 16 RX

DC coupling $\rightarrow$ 0R resistor
AC coupling $\rightarrow$ Capacitor

TX lines: terminator resistor
RX lines: balance resistors

Total footprints: 280
(if sharing footprint between C and R)
Debug

Need to purchase:

- VLDB+ 2000 CHF
- VTRX+ 450 CHF
- Raspberry Pi kit for IpGBT 300 CHF
- Virtex-7 ev. board ~3500 USD
Next steps

- First prototype?
- EMP?
Thank you for your attention!